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Using 3.3V I/O Guidelines in a Virtex-II Pro Design

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Summary

This application note describes guidelines on interfacing 3.3V I/O in a Virtex-II Pro™ system design. Topics include overshoot/undershoot design considerations, Peripheral Component Interface (PCI) bus interface solutions, device configuration, and other board level design techniques.

Introduction

New system I/O standards continue the trend of lowering supply voltage to gain higher throughput performance. Still, many 3.3V I/O standards, including LVTTL and PCI, are prevalent to accommodate legacy requirements. To support all popular design requirements, Virtex-II Pro devices offer a range of 3.3V to 1.5V I/O standards. Despite internal device power of 1.5V, the I/Os are designed to meet every system design challenge.

To achieve maximum performance and get the best the Virtex-II Pro devices have to offer, several 3.3V I/O designs and techniques are highlighted in this application note. This includes managing overshoot/undershoot with termination techniques, PCI design guidelines, configuration rules, and other design considerations.

I/O Standard Design Rules

Supported 3.3V I/O Standards

The Virtex-II Pro family supports the following 3.3V I/O standards: LVTTL, LVCMOS_33, PCI_33, PCI_66, PCI_X, and LVDCI_33.

Overshoot / Undershoot

For 3.3V I/O operations, overshoot and undershoot voltage should not exceed the absolute maximum ratings of –0.3V to 3.75V. The I/O drivers should match the board trace impedance to within ± 10% to minimize over/undershoot. To verify overshoot and undershoot does not exceed the I/O absolute maximum specifications, perform an IBIS simulation.

Source termination is often used to manage overshoot/undershoot. The Virtex-II XCITE™ digitially controlled impedance (DCI) feature has built-in source termination on all user output pins. It compensates for impedance changes due to voltage and/or temperature fluctuations, and can match the reference resistor values. Assuming the reference resistor values are the same as the board trace impedance, the output impedance of the driver will closely match with the board trace.

Using LVDCI_33

The LVDCI_33 standard is used to enable the DCI features for 3.3V I/O operations. As shown in Figure 1, the OBUF_LVDCI_33 primitive is used to implement the source termination function in Virtex-II Pro output drivers. The pullup resistor connected to VRN and the pulldown resistor connected to VRP determine the output impedance of all the output drivers in the same bank.

The LVDCI_33 standard does not offer input termination. Figure 1 also shows the recommended external source termination resistors to be incorporated on the driver side.

The total impedance of the LVTTL/LVCMOS driver added to the series termination resistor R_0 must match the board trace impedance ±10 percent to minimize overshoot and undershoot. An IBIS simulation is advised for calculating the exact value needed for R_0.

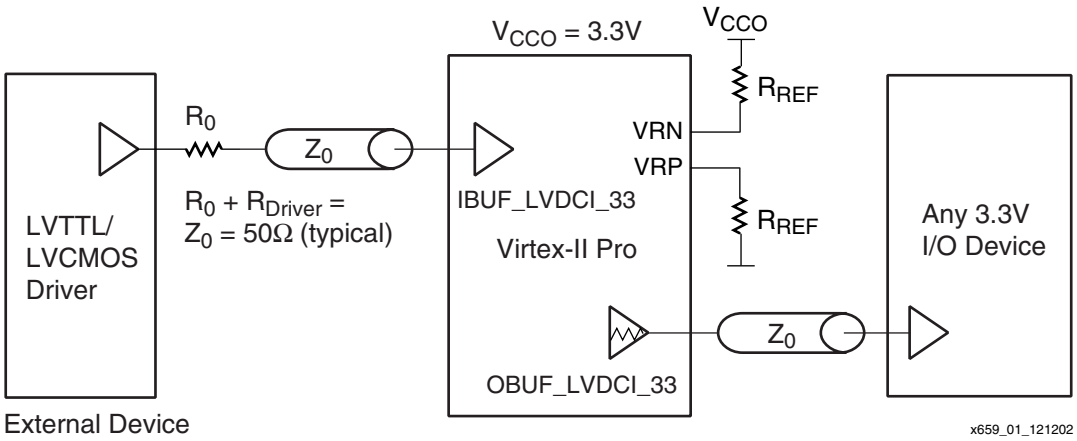

Figure 1: **Connecting LVTTL or LVCMOS Using the LVDCI_33 Standard**

The connection scheme shown in Figure 2 is for a bi-directional bus scenario. The signal performance may be degraded by R_0. Therefore, it is also recommended to verify the R_0 value and performance with an IBIS simulation.

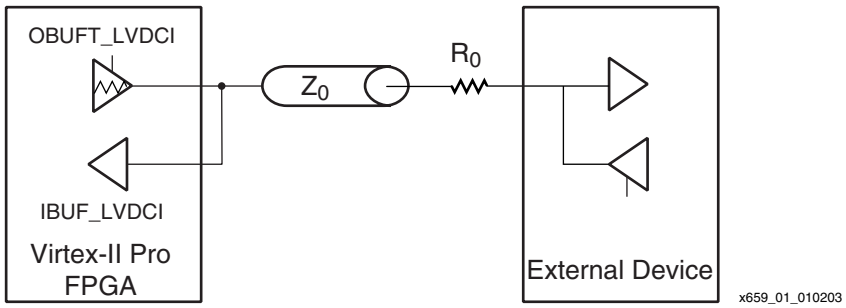

Figure 2: **3.3V I/O Configuration**

The following list contains helpful information for designing with the LVDCI_33 standard:

- The output drive strength and slew rates are not programmable. The output impedance references the VRP and VRN resistors, and the output current is determined by the output impedance.
- If only LVDCI_33 inputs are used, it is not necessary to connect VRP and VRN to external reference resistors. The implementation pad report does not record VRP and VRN being used. External reference resistors are required only if LVDCI_33 outputs are present in a bank.
- LVDCI_33 is compatible with LVTTL and LVCMOS standards only.
- Refer to the Virtex-II Pro user guide on using DCI. It shows an HDL example as well as other DCI design considerations.

The Xilinx **Signal Integrity Central** web site contains additional design information to assist PCB designers and signal integrity engineers.

If the system architecture does not allow termination resistors, as in the case of PCI, different approaches to address overshoot/undershoot are needed. The following section discusses these alternatives.

PCI Bus Solutions

PCI system architecture does not allow termination resistors on a bus. Therefore, the LVDCI_33 method does not support PCI33/66 applications. Two fully verified application notes are available to address the maximum PCI signal overshoot and undershoot specifications related to PCI applications:

- **XAPP653**: Virtex-II Pro 3.3V PCI Reference Design
- **XAPP646**: Connecting Virtex-II Devices to a 3.3V/5V PCI Bus

Table 1 lists application notes to consult for guidance, based on the PCI signaling environment.

Table 1: **Reference Application Notes**

Signaling Environment	Virtex-II Devices	Virtex-II Pro Devices
PCI 3.3V	Not Required	**XAPP653** or **XAPP646**
PCI 5.0V	**XAPP646**	**XAPP646**

Notes:
1. Xilinx recommends **XAPP653** for designing Virtex-II Pro systems in a PCI 3.3V environment, as it is PCI compliant and provides a lower cost solution than **XAPP646**.

Summaries of these two application notes are described in this section. For full details, refer to the specific application notes.

XAPP653: Using a Linear Technology Voltage Regulator Solution

The approach is to lower the V_{CCO} voltage of the Virtex-II Pro device to 3.0V allowing both the clamp diodes D_1 and D_2 to clamp before the signals reach the absolute maximum rating. Since PCI specifications allow the device supply voltage to be as low as 3.0V, it is still PCI compliant.

By lowering the I/O bank voltage V_{CCO} to 3.0V, PCI signals greater than 3.6V are clamped by the internal protection diode in the I/Os. This permits the signal to stay within the absolute maximum upper limit of 3.75V (see Figure 3).

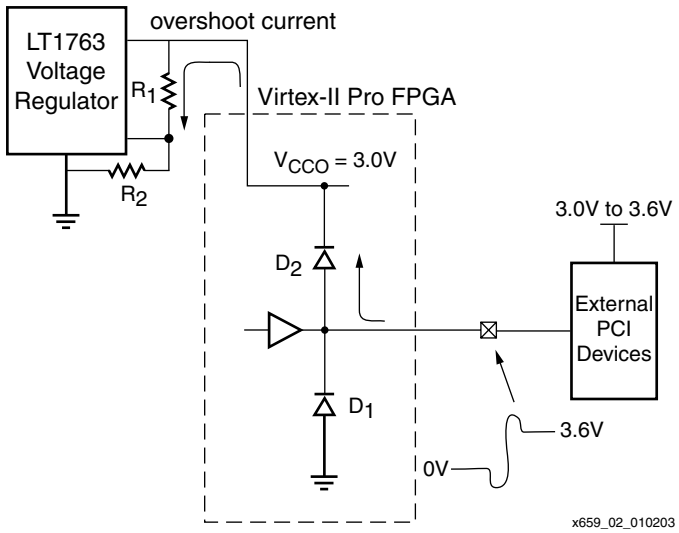

Figure 3: **Clamping PCI Signals**

The PCI bus specification for minimum input voltage is –0.5V. The absolute maximum specification for Virtex-II Pro input (V_{IN}) is –0.3V when V_{CCO} is at 3.45V. When V_{CCO} is lowered to 3.0V, as described in **XAPP653**, this lower limit is changed from –0.3V to –0.5V. Undershoot below –0.5V is clamped by the intrinsic diode in the I/O. Figure 4 shows the **XAPP653** regulator implementation.

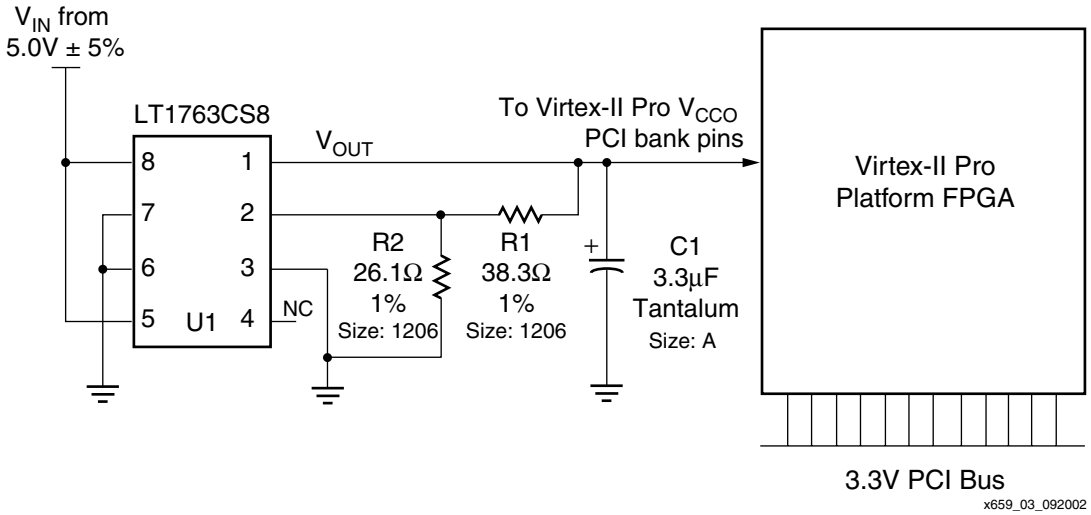

Figure 4: **XAPP653: Regulator Reference Design**

A Texas Instruments voltage regulator can be used as a compatible, alternative solution. Figure 5 shows an example of the TPS7301 low drop-out regulator circuit example.

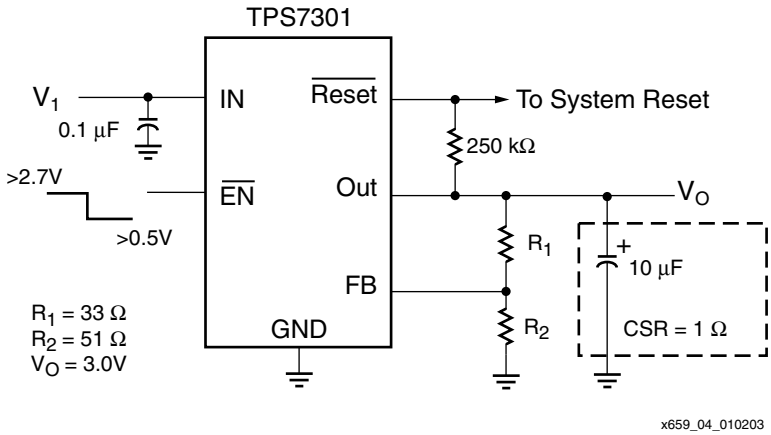

Figure 5: **Texas Instruments TPS7301 Voltage Regulator Example**

For more details, refer to the TI website: **http://www-s.ti.com/sc/ds/tps7301.pdf**

XAPP646: Using the IDT QuickSwitch Solution

The IDT QuickSwitch device is a high-speed bus switch. It allows Virtex-II Pro FPGAs and Virtex-II FPGAs to interface with PCI in 3.3V and 5V environments. In its simplest form, a QuickSwitch device contains a series of NMOS pass transistors with 250 ps delay and less than 5 pF loading. Figure 6 shows the basic QuickSwitch structure.

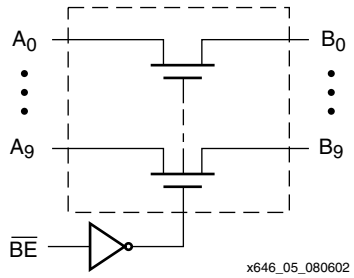

Figure 6: **QuickSwitch Structure**

In Figure 7, the B-side of the QuickSwitch device limits the positive overshoot voltage from the A-side to less than ~3.0V, as the NMOS pass transistor cuts off when the A-side voltage is greater than V_{CC} less the device threshold. It also limits the negative undershoot excursions (undershoot) to no more than –0.1V, due to the intrinsic device diodes.

The 0.1 µF bypass capacitor from V_{CC} to ground (one each per QuickSwitch device) and the 0.1 µF bypass capacitor from the ground pin bias point to the system ground are both required to absorb the transients and provide good clamping and cutoff action. The 390 µF capacitor (values from 220 µF to 470 µF are suitable) is required to keep the negative clamp-level bias voltage stable.

For more implementation details, refer to **XAPP646**.

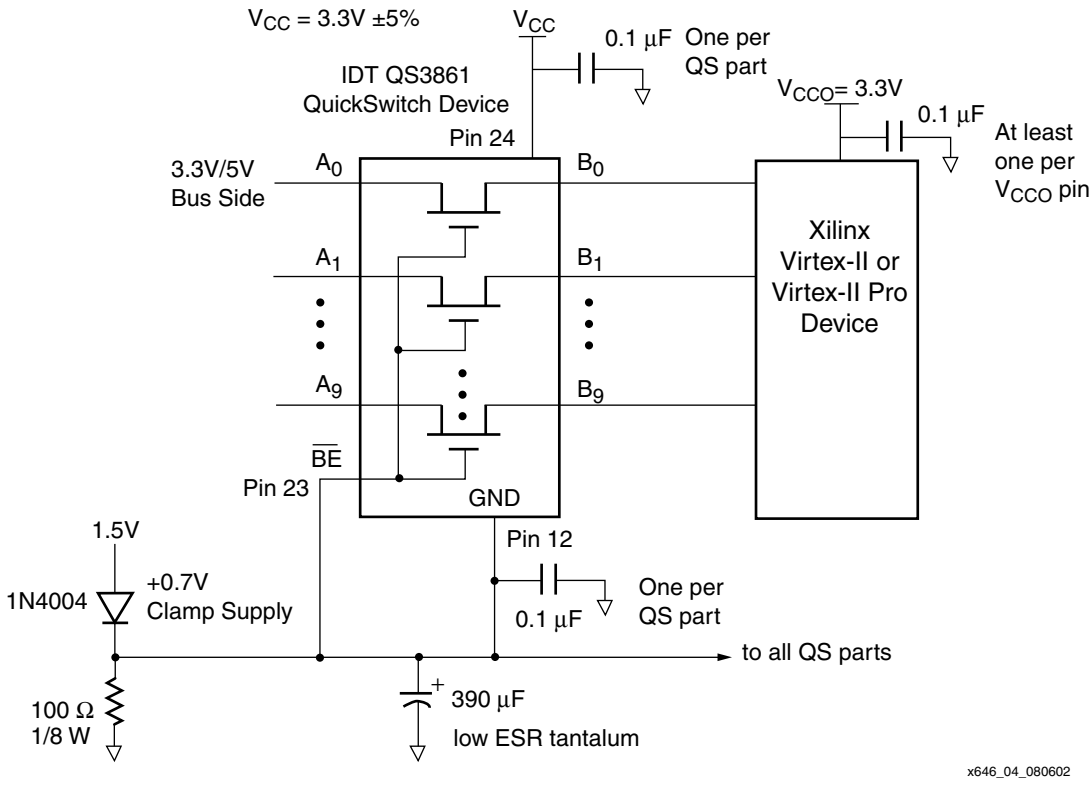

Figure 7: **QuickSwitch-to-FPGA Connection**

Device Configuration

Virtex-II Pro devices can be configured through a JTAG interface port, a serial PROM, or by a System ACE controller.

Dedicated configuration pins such as CCLK, PROG_B, DONE, M2, M1, and M0 are powered by V_{CCAUX} at 2.5V while dual purpose configuration pins such as DIN, D1:D7, CS_B, RDWR_B, BUSY/DOUT and INIT_B can be either 2.5V or 3.3V.

This section describes design information for each method. For further information on configuration, refer to the ***Virtex-II Pro Platform FPGA User Guide***.

JTAG Configuration

Although JTAG pins are powered by V_{CCAUX} (2.5V), all JTAG input pins are 3.3V compatible and operate between 2.5V and 3.3V TTL levels. The JTAG output pin, TDO, is an open drain output. It does not have an internal pull-up resistor and must be pulled up with an external resistor on the PCB. The maximum pull-up voltage is 3.3V. It is recommended to use an external pull-up resistor in the range of 200 Ω. Different resistor values yield different JTAG performance. Perform IBIS simulation to verify the speed.

Serial PROM Configuration

Xilinx recommends using the XC18V00 series of In-System Programmable Configuration PROMs. This family provides 3.3V or 2.5V output capability. When interfacing to the Virtex-II Pro FPGA in both master serial and slave serial mode, the V_{CCO} of the 18V00 PROM should connect to 2.5V. If desired, the V_{CCO} of the Virtex-II Pro bank 4 can connect to 3.3V. The DO pin of the PROM is at LVCMOS25 levels and the DIN pin of the Virtex-II Pro is at LVTTL levels. Therefore, they are compatible. Figure 8 shows the Virtex-II Pro FPGA and the XC18V00 PROM in master serial configuration.

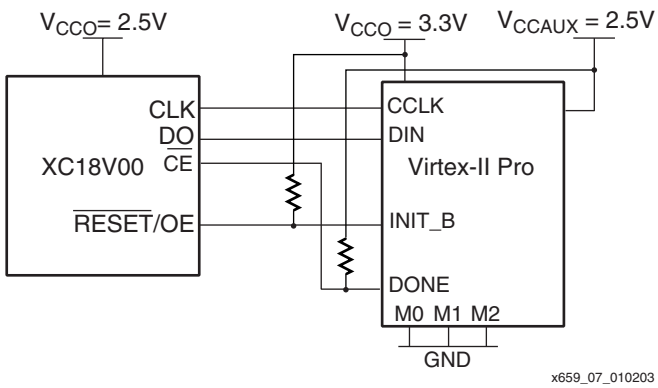

Figure 8: **Virtex-II Pro and XC18V00 PROM in Master Serial Configuration**

Although the noise margin of LVCMOS driving LVTTL is 100mV, the LVCMOS25 driver will most likely run between rail to rail giving more real world margin. For more information about Xilinx PROM solutions, refer to **DS026**.

System ACE Configuration

When interfacing a System ACE controller to a Virtex-II Pro FPGA, set the V_{CCO} of the System ACE controller to either 1.8V or 2.5V, depending upon system DC power availability. For more information, see the **System ACE** web site.

Other System Design Considerations

DC Power Distribution System

Designers need to consider power distribution in their system designs. Many systems have 5V, 3.3V, 2.5V, 1.8V, 1.5V and other DC power requirements. Use **XAPP623** "Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors" as a guide to determine board level decoupling requirements for a successful system design

Package Thermal Management

The absolute maximum junction temperature (T_J) is lowered from 125°C to 100°C for 3.3V I/O operation for the Virtex-II Pro FPGA. Use Xilinx application note **XAPP415** "Packaging Thermal Management" as a design resource for thermal measurement techniques, package thermal characteristics, and options for power management in a system environment. The document also contains some references for heat-sink and interface material suppliers.

LVDS

Although the Virtex-II Pro Platform FPGA does not support LVDS_33, its input and output specifications are compatible with LVDS_25. It is acceptable to use LVDS_25 in place of LVDS_33.

Implementation Support

Xilinx ISE5.1i implementation tools support LVDCI_33, PCI33_3, and PCI66_3 standards. But LVTTL, LVCMOS_33, and PCI-X standards are not supported until the ISE5.2i release. The current tools perform design rule checks to verify that only supported standards are placed in designated 3.3V I/O banks of the target device. To temporary remove the 3.3V I/O banking restriction before the ISE5.2i release, refer to Xilinx solution record 14965.

Conclusion

Virtex-II Pro devices support 3.3V I/O standards (LVTTL, LVCMOS33, LVDCI33, PCI33/66, and PCIX) when the following guidelines are met:

1. Keep signal overshoot and undershoot within the absolute maximum FPGA device specifications.
2. For PCI bus solutions use either **XAPP653** or **XAPP646**.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/25/02	1.0	Initial Xilinx release.
01/06/03	1.1	Add PCIX, LVTTL_33 and LVCMOS_33 support. Removed 3.3V banking restrictions
01/07/03	1.2	Added new sub-section on supported 3.3V I/O standards.