This year ISQED offers a single full-day tutorial track focusing on a range of critical issues in circuit design at sub-100nm CMOS. We are pleased to have five noted experts in their respective fields (Manufacturability, Variability/Uncertainty, Advanced Devices, Low-Power Design, and Interconnect Modeling/Analysis) to present the latest research in these compelling areas.
ISQED Tutorials
Compact Modeling and Analysis for Nanometer-scale CMOS Design

Part 1
Nanometer-Scale CMOS Devices
Presenter: Kerry Bernstein, IBM T.J. Watson Research Center

This part of the tutorial will examine the operation and idiosyncrasies of emerging deep submicron CMOS devices and materials appearing in future high speed logic products. These novel structures include ultra-thin and fully depleted silicon-on-insulator devices, double-gated transistors, strained silicon, and crystal re-oriented MOSFETs. Molecular computing technologies, such as carbon nano-tubes, and new materials which extend scaling, such as high-k dielectrics, will also be explored. Circuit design issues, soft error vulnerabilities, defect mechanisms and required device model accommodations will also be discussed.

Part 2
Interconnect Modeling
Presenter: Professor Jeff Davis, Georgia Tech

This tutorial will review compact VLSI interconnect models for both parameter extraction (e.g. R, L, and C) and key transient waveform characteristics (e.g. time delay, crosstalk, and overshoot). The tradeoff between model simplicity and accuracy will be explored by comparing the results of these compact models to more detailed interconnect simulations. The impact of the variability of interconnect layout geometries on the accuracy of these compact models will also be discussed. In addition, these compact models will be used to analyze a variety of VLSI interconnect circuits and structures. This analysis will include an overview of the impact of embedded low-k dielectrics on time delay and crosstalk, time delay optimizations with non-ideal repeater placements, interconnect device optimization with coplanar shield lines, and the impact of repeater insertion on inductive crosstalk.
Part 3
Manufacturability

Presenter: Professor Andrew B. Kahng, University of California, San Diego

This portion of the tutorial reviews physical design complications and methodology changes – for example, in the detailed routing arena - that arise from sub-wavelength lithography and deep submicron manufacturing (antennas, metal planarization and mask-wafer mismatch). In addition, yield-constrained optimizations in PD are covered, especially “beyond corners” approaches that escape today’s pessimistic or even incorrect corner-based approaches. We also discuss current and near-term prospects for the overall design-to-manufacturing PD methodology. Key aspects include better integrations with analysis and manufacturing interfaces, as well as cost-benefit tradeoffs for “regular” layout structures that are likely beyond 90nm, cost optimizations for low volume production, and the role of robust and/or stochastic optimization in PD.

Part 4
Low-Power Design

Presenter: Professor Kaushik Roy, Purdue University

This section of the tutorial will present technology scaling and its impacts on dynamic and static power dissipation. Both leakage and dynamic power estimation and design techniques to reduce power dissipation in scaled technologies will be described.

Part 5
Coping with Uncertainty

Presenter: Nagib Hakim, Intel Corporation

Uncertainties from process variations, tool and model inaccuracies, as well as operating environment limit the designers ability to accurately predict product performance and power consumption. Understanding and modeling these effects would enable the development of strategies to better optimize these circuits and perform the desired power-performance tradeoff. The presentation will discuss various sources of uncertainty, their modeling, their impact on various types of circuits, and their use in product development and optimization.