Today’s SoC’s combine an increasingly wide range of heterogenous processing elements, consisting of general purpose RISC’s, DSP’s, application-specific processors, and fixed or configurable hardware. Five to ten processors on an SoC is now common. A bottom-up assembly of these heterogeneous components using an ad-hoc interconnect topology, different instruction sets and embedded S/W development tools leads to unmanageable complexity and low quality. This talk will present an approach to effectively integrate heterogenous parallel components – H/W or S/W – into a homogeneous programming environment. This leads to higher quality designs through encapsulation and abstraction. This approach, supported by ST’s MultiFlex multi-processing SoC tools, allows for the combination of a range of heterogeneous processing elements, supported by high-level programming models. Two programming models are supported: a distributed system object component (DSOC) message passing model, and a symmetrical multi-processing (SMP) model using shared memory. We present the results of mapping an Internet traffic management application, running at 2.5Gb/s. We demonstrate the combined use of the MultiFlex multi-processor compilation tools, supported by high-speed hardware-assisted messaging, context-switching and dynamic task allocation in the StepNP platform.

About Pierre G. Paulin

Pierre Paulin is director of System-on-Chip Platform Automation at STMicroelectronics, Ottawa, Canada. Previously, he was director of Embedded Systems Technologies for ST in Grenoble, France. Before this, he managed embedded software tools and high-level synthesis R&D with Nortel Networks research labs. His interests are in design automation technologies for multi-processor systems, embedded systems and system-level design. He obtained a Ph.D. from Carleton University, Ottawa in 1988, and B.Sc. and M.Sc. degrees from Laval University, Quebec in 1982 and 1984 respectively. He is a member of the IEEE.