Full-Chip Analysis Method of ESD Protection Network

Sachio Hayashi, Fumihiro Minami, Masaaki Yamada†
Toshiba Corporation Semiconductor Company, †Toshiba Microelectronics Corporation
{sachio.hayashi, fumihiro.minami, mm.yamada}@toshiba.co.jp

Abstract

With the advance of process technology, electrostatic discharge (ESD) problem becomes more and more serious. To prevent design iterations caused by ESD failures, it is necessary to verify ESD protection network at design stage. In this paper, we present a full-chip analysis method of ESD protection network, which can analyze pad voltages for every pair of pads. Since the proposed method combines the merits of shortest path search and circuit simulation, it can analyze pad voltages more accurately than shortest path search with a little overhead of run time. The experimental results show that the proposed method can predict the reduction effect of pad voltage by ESD remedy. And it is shown that for a chip with 858 pads, the proposed method can analyze pad voltages of every pair of pads within 2 hours.

1. Introduction

With the advance of process technology, electrostatic discharge (ESD) problem becomes more and more serious. Although gate oxide thickness of MOS transistor becomes thinner with scaling down of integrated circuits (ICs), ESD surge level is not scaled down. As a result, gate oxide becomes more fragile for ESD. On the other hand, many circuit blocks are integrated on a chip with increased integrity of ICs, which requires many power domains to prevent noise coupling between circuit blocks. Increase of power domains makes ESD protection network design difficult. With such situations, it becomes difficult to achieve necessary ESD performance by traditional ESD protection approach. Therefore, it is urgently needed to establish chip-level quantitative ESD design method and ESD verification method.

The principle to protect an IC chip from ESD damage is to design on-chip ESD protection network to meet the following two conditions: to provide low impedance path between any two pads to discharge large ESD current safely, and to clamp pad voltage between any two pads to a sufficiently low level to avoid gate oxide breakdown [1]. Since high pad voltage means large risk of ESD damage and low pad voltage means low risk of ESD damage, pad voltage becomes a metric of ESD robustness. To prevent ESD failure, it is important to verify at design stage whether ESD current path exists for any two pads, and whether pad voltage between any two pads is sufficiently low level. But such a verification tool is not available commercially at present. Insufficient verification of ESD protection network at design stage causes many ESD failures and many design iterations which lead to large loss of cost. Therefore, the needs for ESD verification tools are increasing recently.

Some previous works exist regarding to ESD verification methods. Ref. [2] presents the first practical ESD verification tool which can check various ESD design rules including bus resistance related rules. Ref. [3] presents a schematic-based ESD verification tool, which is a SPICE pre/post processor and extracts only a critical ESD current path netlist. Ref. [4] presents a chip-level verification method for charged device failures using hierarchical modeling approach. Since it relies on transient circuit simulation, it can only be applied to a limited number of pad pairs. The analysis methods of pad voltage are presented in [5], [6]. In these methods, ESD protection network is extracted from layout, which is represented as a graph, and pad voltage is analyzed using this graph. In [5], I-V characteristic of pad voltage is obtained by recursively reducing I-V tables of devices on the ESD current paths. But, it is not efficient for analyzing all pad pairs. In [6], Dijkstra's shortest path search algorithm [7] is used to obtain the least impedance path between two pads and the pad voltage between them. Since Dijkstra's algorithm is very fast, all pad pairs can be analyzed. But, it has a problem that pad voltage is overestimated since it takes into account only one current path to calculate pad voltage.

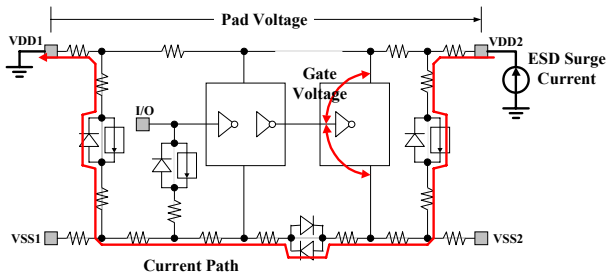

Fig. 1. Functionality of the proposed method

In this paper, we propose a full-chip analysis method of ESD protection network. The functionality of the proposed method is illustrated in Fig. 1. The proposed method searches the minimum impedance current path between two pads, and calculates the pad voltage between them. What is obtained is the static pad voltage in the state where constant ESD surge current is applied. Although ESD is a transient phenomenon actually, such a time-varying behavior is ignored. But, for the purpose of detecting the weak portion of ESD protection network at design stage, such static analysis would be useful.

The proposed method adopts a shortest path search approach such as presented in [6] as basis, but some improvements have been done to increase accuracy of pad voltage. Accuracy is improved by calculating node-to-node voltages of resistance networks on the ESD current path using circuit simulation. We propose an efficient method to calculate node-to-node voltages of resistance networks, which is efficient especially when many pad pairs are analyzed. Since some accuracy problem is remained, we present a practical method for pad voltage analysis by hybrid use of the proposed method and circuit simulation.

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Although pad voltage can be used as a metric of ESD robustness, pad voltage is not necessary applied to gate oxide directly. Even if pad voltage is high, when gate voltage is low, it is considered that the risk of ESD damage is low. Therefore, gate voltage is more useful than pad voltage to detect the risk of gate oxide breakdown, which is a significant ESD failure in recent ICs. Therefore, we present a method to estimate maximum gate voltage from the pad voltage analysis result.

The remainder of this paper is organized as follows. In Section 2, the analysis flow of the proposed method is presented. In Section 3, the details of pad voltage analysis method are described. In Section 4, gate voltage analysis method is presented. In Section 5, experimental results are shown, followed by conclusions in Section 6.

2. Analysis Flow

The analysis flow of the proposed method is shown in Fig. 2. In Step1, an ESD protection network consisting of nets connected to pads and protection devices connected between these nets is extracted from layout. In Step2, for each net connected to the pads, parasitic resistances are extracted. Since pad voltage is determined by sum of clamp voltages of protection devices and voltage drops of parasitic resistances, it is necessary to extract parasitic resistances as accurately as possible. Therefore, parasitic resistances are extracted including power supply wirings in the core area. In Step3, resistance network reduction is performed. In Step4, pad voltage analysis is performed to the extracted ESD protection network. The pad voltage analysis method is described in detail in Section 3.

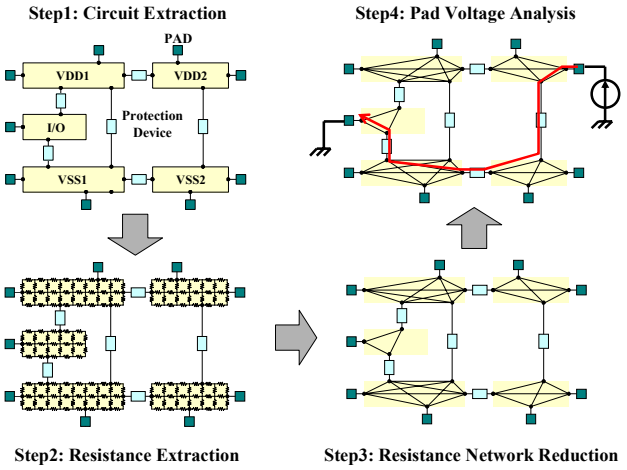

Fig. 2. Analysis flow

3. Pad Voltage Analysis

3.1. Circuit Simulation Method and Shortest Path Search Method

At first, two basic methods to analyze pad voltage are explained. One method is circuit simulation method and the other is shortest path search method.

The circuit simulation method is explained with Fig. 3. For the ESD protection network extracted from layout as in Fig. 3(a), a current source representing ESD surge current is connected to a stressed pad, and a grounded pad is connected to the ground, as shown in Fig. 3(b). For the circuit as in Fig. 3(b), DC analysis is performed with a circuit simulator. The voltage at the stressed pad corresponds to the pad voltage. Since the circuit simulation method can take into account all current conducting paths, accurate pad voltage can be obtained. But, as it takes about 10 minutes to analyze one pad pair for a chip of typical size, only a very small number of pad pairs can be analyzed.

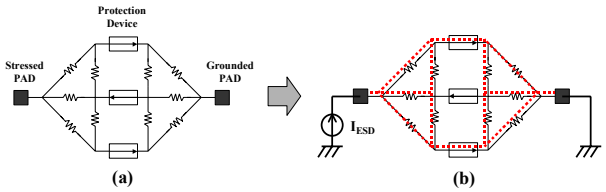

Fig. 3. Circuit simulation method

The shortest path search method is explained with Fig. 4. From the ESD protection network extracted from layout as in Fig. 4(a), a directed graph as in Fig. 4(b) is created. For protection devices, edges whose direction is the same as the current direction of the protection device are created, and for resistances, edges are created for both directions. For each edge, weight whose value is the same as the terminal voltage is given. For this graph, shortest path search by Dijkstra's algorithm is performed, and the path giving minimum voltage between the stressed pad and the grounded pad is searched. As a result, the least impedance current path between the pads and the pad voltage when ESD current flows on that current path are obtained. Since Dijkstra's algorithm is very fast, all pad pairs can be analyzed. But, only one current path can be taken into account, the shortest path search method has a problem that pad voltage is overestimated. To solve this overestimation problem, convex minimum cost maximum flow algorithm is applied in [6]. Although this algorithm seems to be faster than the circuit simulation method, it is still too time consuming to analyze all pad pairs.

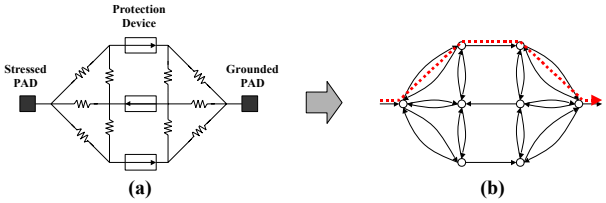

Fig. 4. Shortest path search method

3.2. Proposed Method

The circuit simulation method is accurate, but it is too time consuming to analyze all pad pairs. On the other hand, the shortest path search method is fast enough to analyze all pad pairs, but its accuracy is not good. Therefore, we propose a method which combines the merits of both methods. The proposed method is based on the shortest path search method basically, but it uses circuit simulation for partial resistance networks which do not contain protection devices, and it calculates the whole voltage difference between two pads using the voltage analysis results of partial resistance networks. Since circuit simulation is applied to only partial resistance networks,

the proposed method can perform analysis fast enough without losing accuracy.

The proposed method is explained with Fig. 5. At first, the shortest path search method is performed for all pad pairs, and the current path information between any two pads is obtained. One of the obtained current paths is shown in Fig. 5 as an example. For resistance networks (A)(B)(C)(D) which the current path P passes, current sources are connected to the input and output nodes of current as shown in (a)(b)(c)(d), and the circuit simulation is performed for each circuit (a)(b)(c)(d). A voltage drop of a resistance network taking into account all current paths can be obtained by calculating the voltage difference between the input and output nodes of current. Then, by summing the obtained voltages of resistance networks and the clamp voltages of protection devices on the current path, an accurate pad voltage which takes into account all current paths in the resistance networks can be obtained.

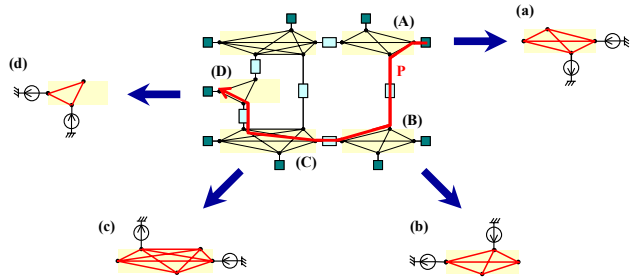

Fig. 5. Overview of the proposed method

Since it is inefficient to run a circuit simulator many times to analyze node-to-node voltages of resistance networks, we adopt the following method. At first, for each resistance network, all node pairs whose node-to-node voltage must be calculated are listed up in a node pair table. For example, when there are three current paths P, Q, R as shown in Fig. 6(a), a node pair table shown in Fig. 6(b) is created. Then, for each resistance network, node-to-node voltages of all node pairs listed in the node pair table are calculated using a modified circuit simulator.

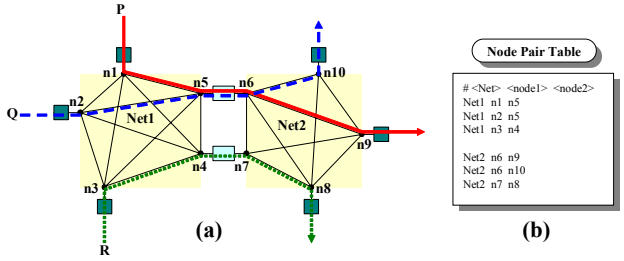

Fig. 6. Node pair table

Here, the method to calculate the node-to-node voltage between the nodes n_i and n_j of the circuit shown in Fig. 7(a) is explained in the following. The analysis flow of a conventional circuit simulator is shown in Fig. 8(a). At first, a netlist is inputted, and the nodal equation GV=I as shown in Fig. 7(b) is constructed. G represents conductance matrix for resistance network, V represents node voltage vector for each node voltage, and I represents current source vector for current sources connected to each node. The current source (P) in Fig. 7(a) corresponds to the element (p) in the vector I, and the current source (Q) in Fig. 7(a) corresponds to the element (q) in the vector I. Next, LU factorization of coefficient matrix G and forward substitution and backward substitution is performed. After that, node voltages of each node in V are obtained. The node-to-node voltage between the nodes n_i and n_j can be obtained by calculating the voltage difference between the nodes n_i and n_j.

By the way, for calculating the node-to-node voltage between the nodes n_k and n_l of the same resistance network, as coefficient matrix G becomes the same, the LU factorization of coefficient matrix G can be reused. By changing the only right-hand side vector I as shown in Fig. 7(c) and performing forward substitution and backward substitution using the same LU factorization of G, the node-to-node voltage between the nodes n_k and n_l can be obtained. As the steps from Step1 to Step3 in Fig. 8(a) can be skipped, execution time can be reduced.

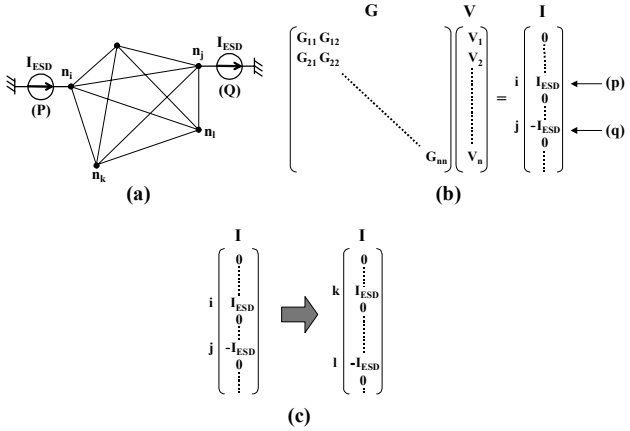

Fig. 7. Analysis method of node-to-node voltage

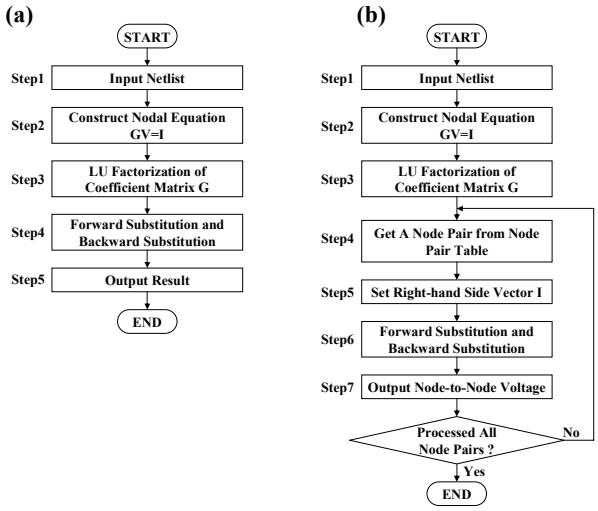

Fig. 8. Analysis flow of circuit simulator

Therefore, in the proposed method, a modified circuit simulator whose analysis flow is shown in Fig. 8(b) is used to calculate node-to-node voltages of node pairs listed in the node pair table for each resistance network. The execution of steps from Step1 to Step3 is necessary only one time for each resistance network, the execution time is reduced compared to

executing a conventional circuit simulator many times for every pad pair.

For a resistance network having 41212 nodes, CPU time necessary for analyzing node-to-node voltages is shown in Table 1. Compared to running a conventional circuit simulator many times, using a modified circuit simulator can reduce CPU time significantly.

Table 1. Execution time of node-to-node voltage analysis

	Node pair count		
	100	1000	10000
Using conventional circuit simulator	313	3147	31465
Using modified circuit simulator	33	44	154

(unit:sec)

Fig. 9 shows the comparison of pad voltages of randomly selected 500 pad pairs, which are obtained by the circuit simulation method, the shortest path search method and the proposed method. The proposed method can obtain closer pad voltages to the circuit simulation method than the shortest path search method. Table 2 shows the comparison of execution times of the shortest path search method and the proposed method for three chips used in the experiment shown in Section 5. It is found that large overhead of execution time does not occur in the proposed method.

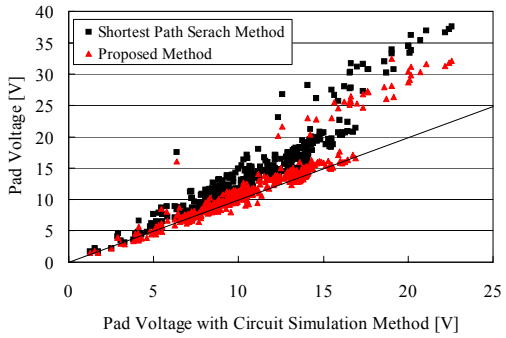

Fig. 9. Comparison of pad voltage

Table 2. Execution time of pad voltage analysis

	Chip1	Chip2	Chip3
Shortest path search method	256	3397	5635
Proposed method	294	4506	6751

(unit:sec)

3.3. Hybrid Use of Proposed Method and Circuit Simulation Method

Our present implementation of the proposed method uses the predefined default sizes to calculate clamp voltages of protection devices. In Fig. 9, some discrepancies between the proposed method and the circuit simulation method are observed. The reason may be that there are some protection devices whose effective size deviates largely from the predefined default size. Since such an accuracy problem still exists in the proposed method, we present a method to analyze pad voltage by hybrid use of the proposed method and the circuit simulation method in the following.

At first, pad voltage analysis by the proposed method is performed for all pad pairs. Next, pads are divided into groups according to their net or I/O type. Then, for each pair of stressed pad group and grounded pad group, a pad pair giving maximum pad voltage and a pad pair giving minimum pad voltage are searched, and the circuit simulation method is performed for these pad pairs. It is considered that if pad pairs are ones between the same type of stressed pad and the same type of grounded pad, relative order of pad voltage is almost coincide between the proposed method and the circuit simulation method. Thus, it is expected that the pad voltages obtained by the circuit simulation method in the above would become the maximum and minimum values obtained by the circuit simulation method.

One example is shown in Fig. 10. In this example, stressed pads are ones of power supply nets, and grounded pads are ones of VSS net. The horizontal axis represents stressed pad groups. The hashed lines represent maximum and minimum values of pad voltages obtained by the proposed method. The straight lines represent pad voltages which are obtained by performing the circuit simulation method for the pad pairs giving maximum and minimum values of the proposed method. It is expected that pad voltages obtained by the circuit simulation method for other pad pairs would exist between the two straight lines. In such a way, accurate minimum and maximum values of pad voltage can be obtained for each pair of stressed pad group and grounded pad group, by hybrid use of the proposed method and the circuit simulation method.

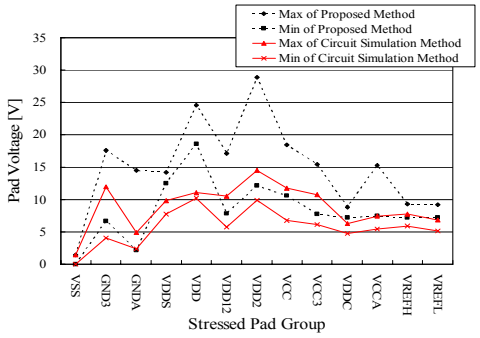

Fig. 10. Maximum and minimum of pad voltage

4. Gate Voltage Analysis

To detect the risk of gate oxide breakdown, it is more useful to analyze gate voltage. From the pad voltage analysis result by the proposed method, maximum gate voltage can be obtained for each pad pair. Here, maximum gate voltage means the upper bound of voltage difference which may be applied to gate oxide of MOS transistor.

The gate voltage analysis method is explained with Fig. 11. In this figure, a current path between PAD_i and PAD_j is shown with potential values from PAD_j. At first, for each pair of nets, it is checked whether a MOS transistor, for which voltage difference is applied to gate oxide, exists or not by searching the netlist. Next, for each pair of nets which has such transistor, maximum voltage difference between the nets, ΔV_{max}, is calculated using potential values from PAD_j. For example, in the case of Net2 and Net3 in Fig. 11, ΔV_{max} is V5-V2, since V5 is maximum potential of Net3 and V2 is minimum potential of Net2. After that, maximum of ΔV_{max} is calculated. This value corresponds to the maximum gate voltage for the pad pair of PAD_i and PAD_j. In such a way, maximum gate voltage can be obtained for all pad pairs.

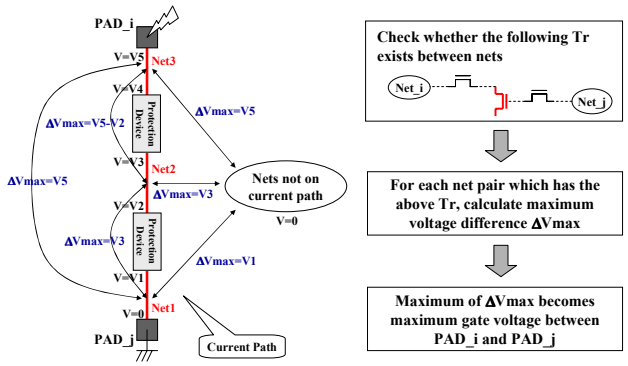

Fig. 11. Gate voltage analysis method

5. Experimental Results

The proposed ESD protection network analysis method was applied to three chips. This section shows the analysis results.

5.1. Test Data

Chip size and pad count of three chips used in the experiment are summarized in Table 3. Regarding to Chip1, there are two chips, one is a chip before ESD remedy, and the other is a chip after ESD remedy. In the chip after ESD remedy, silicon-controlled rectifiers (SCRs) are used instead of grounded gate NMOSs (ggNMOSs), and power bus resistance is lowered.

Table 3. Test Data

	Chip Size	Pad Count
Chip1	5.9mm x 5.9mm	210
Chip2	9.3mm x 9.3mm	568
Chip3	13.9mm x 13.9mm	858

5.2. Pad Voltage Analysis Result

Pad voltage analysis has been done using ESD current value 1.3A, which corresponds to peak current of HBM (Human Body Model) 2kV ESD test method. Pad voltage plots obtained from the analysis result are shown in Fig. 12. In each plot, the horizontal axis represents stressed pads and the vertical axis represents grounded pads. At the coordinate (PAD_i, PAD_j), pad voltage between PAD_i and PAD_j is plotted according to the level of pad voltage. Therefore, pad voltages of all pad pairs are shown in this plot. In the case of Chip1 in Fig. 12, scales of pad voltage are the same between before ESD remedy and after ESD remedy. From comparison between before ESD remedy and after ESD remedy, it is found that the area of high pad voltage level is reduced, which means pad voltages are reduced significantly by ESD remedy. In such a way, it is possible to capture the effect of ESD remedy visually with the pad voltage plot. In the case of Chip2 in Fig. 12, there are some white lines, which represent that there is no current path between pads. So, existence of current path between any two pads can also be checked visually with this plot.

Pad voltage distributions of each chip are shown in Fig. 13. In the case of Chip1 in Fig. 13, pad voltage distributions of before ESD remedy and after ESD remedy are overlaid in the same plot. It is found that pad voltage distribution is significantly improved by ESD remedy.

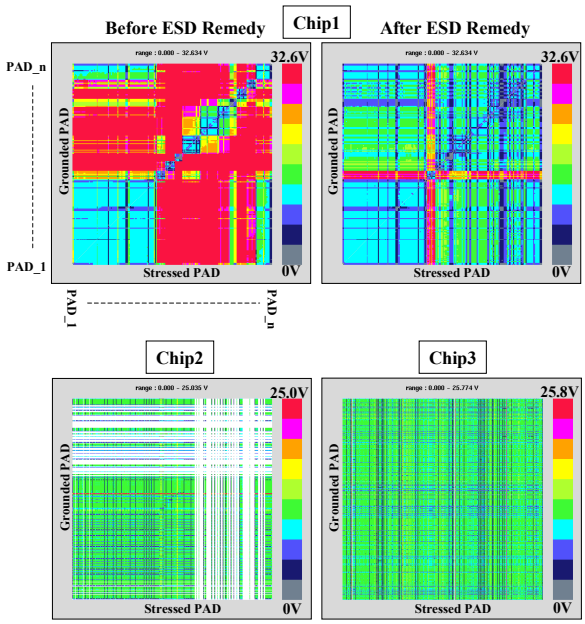

Fig. 12. Pad voltage plot

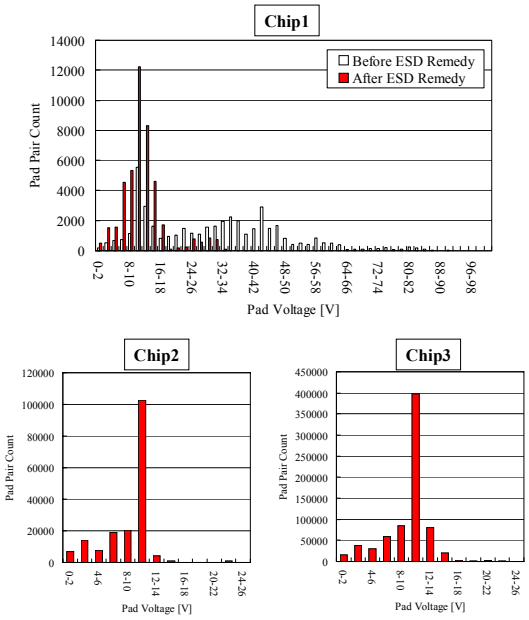

Fig. 13. Pad voltage distribution

5.3. Example of Current Path

Current path information between any two pads can be obtained from the pad voltage analysis result by the proposed method. Therefore, current paths can be displayed graphically, and can be overlaid on the layout. The example of current path of Chip1 is shown in Fig. 14. In the case of before ESD remedy, the current path passes on the large area and the number of protection devises which the current path passes is six. On the other hand, in the case of after ESD remedy, the current path is

improved and the number of protection devices which the current path passes is reduced to two. As a result, pad voltage is reduced from 101V to 13V.

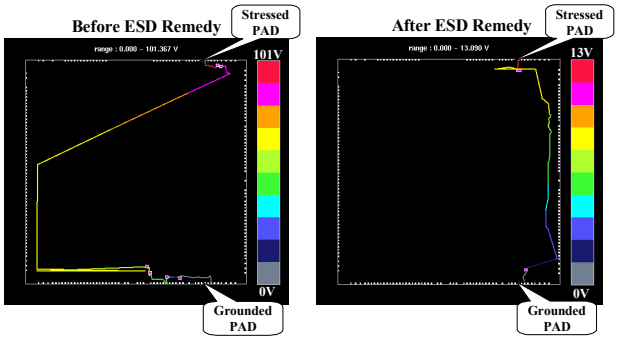

Fig. 14. Example of current path

5.4. Comparison with Tester Result

For Chip3, ESD test result with a tester as shown in Table 4 has been obtained. This tester result is for the case that the stressed pad is one of each power supply net or I/O type, and the grounded pad is one of VSS net. The weak result is obtained in the case that the stressed pad is one of VCC or LVDS-TX (LVDS driver).

Table 4. Tester result

Stressed Pad	GND3	GNDA	VDDS	VDD	VDD12	VDD2	VCC
Tester Result	±2000V PASS	±2000V PASS	±2000V PASS	±2000V PASS	±2000V PASS	±2000V PASS	±2000V FAIL

VCC3	VDDC	VCCA	VREFH	VREFL	LVDS-TX	LVDS-RX	CMOS I/O
±2000V PASS	±2000V PASS	±2000V PASS	±2000V PASS	±2000V PASS	±2000V FAIL	±2000V PASS	±2000V PASS

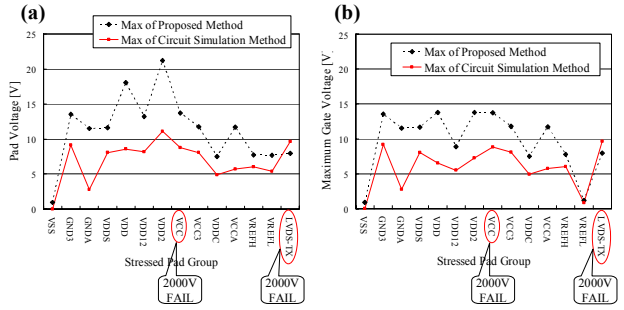

Fig. 15. Comparison with tester result

This tester result is compared with the pad voltage analysis result, which is obtained by hybrid use of the proposed method and the circuit simulation method. The analysis result is shown in Fig. 15(a), in which only maximum pad voltages for each stressed pad group are shown. In this figure, the stressed pad groups which give weak tester result are designated with circles. When maximum pad voltage of the circuit simulation method is compared, a certain amount of correlation to the tester result is observed, since pad voltage is relatively high at the stressed pad group which gives weak tester result.

Next, maximum gate voltage, which is obtained by the gate voltage analysis method described in Section 4, is compared. Since maximum gate voltage is calculated from the pad voltage analysis result by the proposed method, maximum gate voltage of the circuit simulation method was calculated by the following equation.

> maximum gate voltage of the circuit simulation method = maximum gate voltage of the proposed method * (pad voltage of the circuit simulation method / pad voltage of the proposed method)

The obtained maximum gate voltages are shown in Fig. 15(b). When maximum gate voltage of the circuit simulation method is compared, more clear correlation to the tester result is observed compared to Fig. 15(a).

5.5. Run Time

Run times are summarized in Table 5. "Extraction" row represents the run time required for extracting ESD protection network from layout. "Pad voltage analysis" row represents the run time to analyze pad voltages for all pad pairs. The analysis can be accomplished within the reasonable run time even for a large chip with 858 pads.

Table 5. Run time

	Chip1	Chip2	Chip3
Extraction	1:43:10	12:05:21	11:12:54
Pad Voltage Analysis	0:04:54	1:15:06	1:52:31

(hour:minute:second)

6. Conclusion

In this paper, full-chip analysis method for ESD protection network, which can analyze pad voltage and maximum gate voltage for all pad pairs, is presented. Since the proposed method combines the merits of the shortest path search method and the circuit simulation method, it can analyze pad voltage more accurately with a little overhead of run time compared to the shortest path search method. From the experimental results, it is shown that the proposed method can predict the reduction effect of pad voltage by ESD remedy. Also, it is shown that more clear correlation to the tester result can be obtained by maximum gate voltage compared to pad voltage. Furthermore, it is shown that the proposed method can analyze all pad voltages between every pair of pads within reasonable run time.

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