Circuit Level Reliability Analysis of Cu Interconnects

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Abstract

Copper (Cu) based interconnect technology is expected to meet some of the challenges of technology scaling in the pursuit of higher performance. However, Cu interconnects are still susceptible to electromigration-induced failure over time. We describe a new hierarchical approach for predicting the reliability of Cu-based interconnects in circuit layouts, and present an RCAD tool, SysRel, for such an analysis. We propose a (jL) product filtering algorithm with a classification of separate via-above and via-below treatments in Cu interconnect trees. After the filtering of immortal trees, a default model is applied to the remaining trees to compute reliability figures for individual units. SysRel utilizes joint stochastic reliability metrics based on the desired lifetime of a chip and combines reliability figures from individual fundamental reliability units. Simulation results with a 32-bit comparator circuit layout demonstrate the significance of our methodology in selectively identifying critical nets and their impacts on overall reliability.

1. Introduction

Copper (Cu) has been replacing aluminum (Al) as the material of choice for interconnects due to its lower sheet resistance. While the electromigration behavior of Al interconnects is quite well understood [1], the reliability of Cu is still under active study. According to the International Technology Roadmap for Semiconductors [2], more than 5 kilometers of active metal wiring per centimeter square are required to construct a high-performance IC in 2003. In addition, a more stringent operating condition of the metal interconnects is expected, with a service temperature of 105°C and a maximum current density $1.3\times10^7$ A/cm². Although Cu interconnects are able to meet these technological requirements, they are still susceptible to electromigration-induced failure over time, just like Al-based interconnects.

Models and techniques have been developed to make realistic reliability assessments of interconnects in ICs during the design and layout process (Reliability Computer Aided Design, RCAD), so that the reliability data can be fed back, and changes can be made promptly before the fabrication process to achieve optimum reliability and performance. BERT (BErkeley Reliability Tool) [3], iTEM [4], ERNI (Electromigration Reliability of Networked Interconnects), and ERNI-3D [5, 6] are examples of performance and reliability analysis tools for Al-based interconnect technology that have been developed previously. BERT and iTEM calculate the overall reliability of a given layout based on reliability estimations for individual straight line segments. However, the reliability of segments depends strongly on the activities in linked segments in both Al and Cu [7]. ERNI and ERNI-3D are based on a hierarchical methodology based on filtering of immortal interconnect trees, which are more fundamental reliability units.

In this paper, we present a new hierarchical approach, suitable for design-time analysis, in predicting the reliability of Cu-based interconnects in circuit layouts. Immortality filters based on the critical (jL) product, followed by a conservative default model based on the analysis of the time for void nucleation or void growth at vias, are applied to assess the reliability of each failure unit. The approach is implemented in a new RCAD tool, SysRel (System-level IC Reliability).

2. Electromigration Experiments

Detailed experimental work is a prerequisite to understanding electromigration trends in Cu technology. Figure 1 shows a sample of test structures: straight via-to-via interconnects (‘I’), straight via-to-via lines with an additional via at the center (‘dotted-I’), straight via-to-via lines with an additional metal limb at the center (‘T’), straight via-to-via lines with two additional metal limbs at the center (‘+’), straight via-to-via lines with a transition in width along the interconnect (‘width-transition’) and wider straight via-to-via lines with extra metal limbs nearer to one side of the lines (‘asymmetrical T transition’). The test lines are either in the first (M1) or second (M2) level of metallization.
Test samples were fabricated using a Cu dual-damascene process in IME and SEMATECH. Sixteen samples of each test were stressed in a package-level electromigration test system with a temperature range between 50°C and 400°C. To reduce the possibility of temperature-induced failures and variations in diffusivity due to joule heating, current densities were chosen to limit joule heating below 10°C. The range of current densities was between 0.5 to 5.0 MA/cm².

In addition to recording median-time-to-failure ($t_{50}$) (defined as time to 30% increase in resistance) and standard deviation ($\sigma$), resistance trends were observed for different structures. All the failures detected were due to open-circuit failure from the formation of voids. Experimental results and failure characteristics are presented in detail in [7-10]. Voids nucleate easily at the Cu/Si₃N₄ interface in Cu interconnects. Therefore, M2 structures have a higher lifetime than that of identical M1 structures [8]. Moreover, M2 dual-damascene interconnects have a larger critical current-density linewidth product than M1 lines [7]. This phenomenon applies to all metal layers. If the electron current is flowing into the line from a via on top, a shorter lifetime applies to all metal layers. If the electron current is length product than M1 lines [7]. This phenomenon interconnects have a larger critical current-density line-structures have a higher lifetime than that of identical M1

3. Hierarchical Reliability Methodology for Cu Interconnects

It is impossible to fabricate all the possible interconnect trees found in an IC and experimentally test all of them to determine their reliabilities. However, a set of rules and specifications can be developed to make realistic reliability assessments of complex interconnect networks. From the experimental results of various Cu interconnect trees, we have developed a hierarchical reliability analysis approach. Following are the steps of the hierarchical method.

i) Extract interconnect trees from a layout.

An interconnect tree is a unit of continuously connected high-conductivity metal lying within one layer of metallization. In addition to geometric properties, the locations of the vias/contacts are also identified on each interconnect tree. Given an interconnect tree, every via is classified as “via-above” or “via-below” depending on whether it is located above or below the interconnect line, respectively.

ii) Determine the maximum of the smallest distances between two junctions, $L_{\text{max}}$.

To find the longest distance between two vias in an extracted tree, an interconnected graph needs to be created. The shortest distances between all connected vias are calculated and then $L_{\text{max}}$ is determined by using the Minimum Spanning Tree algorithm.

iii) Filter interconnect trees using “M1” ($jL_{\text{crit,nuc}}$) failure criterion.

The first step of the filtering algorithm assumes the worst case scenario. The maximum current density allowed by the design rule, $j_{\text{max}}$, can be obtained from the International Technology Roadmap for Semiconductors [2]. Assuming the worst case condition of $(jL)_{\text{crit,nuc}} = 1500 \, \text{A/cm}$ [11] (i.e. the via is above the line at the cathode end as in a M1 test structure), the program checks whether $(jL)_{\text{crit,nuc}}/j_{\text{max}} > L_{\text{max}}$ for every interconnect tree. If so, the tree is considered immortal and can be ignored in further analysis.

iv) Filter mortal interconnect trees using “M2” ($jL_{\text{crit,sat}}$) failure criterion.

Determine if either of the vias contributing to $L_{\text{max}}$ is a via-above. If at least one of the vias happens to be via-above, the interconnect tree may fail with a M1 $(jL)_{\text{crit,nuc}}$ failure criterion as determined in the previous step and the hierarchical flow proceeds directly to step (v). However, if both of the vias are via-below, the M2 $(jL)_{\text{crit,sat}}$ failure criterion of $(jL)_{\text{crit,sat}} = 3700 \, \text{A/cm}$ [12] is applied. The condition $(jL)_{\text{crit,sat}}/j_{\text{max}} > L_{\text{max}}$ is checked for such interconnect trees. However, even if a tree passes this test, all the other vias in the tree must be considered before classifying it as immortal. This is because via-above nodes have a much smaller immortality value and thus shorter lengths may fail. The longest distance in the graph from any via-above node to all other vias, $L_{\text{max, via}}$, is determined. We again apply the test $(jL)_{\text{crit,sat}}/j_{\text{max}} > L_{\text{max, via}}$ to determine whether the tree might fail.

v) Estimate the current density, $j_{i}$, in each segment.

The $\text{Vdd}$ and $\text{Gnd}$ lines need to be identified as they have unidirectional current flow and are most susceptible to electromigration failure. Most local interconnects transmit signals between devices in the form of bidirectional or alternating current (AC). In these cases,
an equivalent direct current (DC) which produces the same electromigration damage [13], such as the root-mean-square (RMS) of the AC, is assumed. On the other hand, clock signals usually operate with pulsed DC. Experiments [13] and modeling [14] have shown that the equivalent DC is given by the average of the pulsed DC, \( I_{\text{avg}} \), which is given by the expression

\[
I_{\text{avg}} = rI \quad \text{with} \quad r = \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}}
\]

where \( I \) is the current during the “on” time and \( r \) is the duty ratio given by \( t_{\text{on}} \) and \( t_{\text{off}} \) where \( t_{\text{on}} \) is the pulse width and the sum of \( t_{\text{on}} \) and \( t_{\text{off}} \) equals the period. The worst case loading of \( Vdd \) and \( Gnd \) lines can be identified using power consumption reports from a circuit simulation tool. However, estimating current flow at each segment in local interconnects is complicated and requires detailed circuit-level simulation which is an active area of research.

vi) Filter mortal interconnect trees by detailed calculation of steady-state stresses.

The concept of steady-state stresses in interconnect trees is an extension of the immortality condition in stud-to-stud lines. The maximum stress difference in an interconnect tree, \( \Delta \sigma_{\text{max}} \), is given by the path that has the highest sum of the \((jL) \) products, summing over the limbs in the path [15]. This is expressed by

\[
\Delta \sigma_{\text{max}} = \frac{Z^* e \rho}{\Omega} (jL)_{\text{eff}}
\]

with \( (jL)_{\text{eff}} = \max_{\text{pair } i,j} \left( \sum_k j_k L_k \right) \)

where \( \Delta \sigma_{\text{max}} \) is the stress difference between the anode and the cathode, \( Z^* \) is the effective charge number, \( e \) is the elementary charge, \( \rho \) is the electrical resistivity of the metal, \( \Omega \) is the atomic volume, and \( j_k \) and \( L_k \) are the current density in, and length of, segment \( k \), respectively. To filter the immune interconnect trees using \((jL)_{\text{eff}}\), repeat steps (iii) and (iv) by replacing \((jL)_{\text{eff}} \) with \((jL)_{\text{off}} \).

vii) Analyze remaining mortal interconnect trees with electromigration failure models.

A conservative default electromigration model based on the analysis of individual nodes (junctions, vias, or contacts) in trees is used to estimate the lifetimes of the mortal trees. The output of the model is the time-to-failure of a tree. Furthermore, numerical methods can be applied for detailed calculation of the time-dependent stress analysis. Software programs, such as MIT/EmSim [16] and CuEmSim [17], allow the calculation of stress evolution in multi-terminal interconnect trees.

viii) Apply full chip stochastic reliability model.

The \( t_{50} \) of each mortal interconnect tree is estimated using the default model or a linked simulation program (e.g. MIT/EmSim). The full chip reliability model combines the \( t_{50} \) of multiple interconnect trees from the same layout and provides a set of reliability metrics for the overall chip. The model is discussed in section 7.

4. Electromigration Lifetime Model

While simulation of electromigration in complex interconnects is possible, less computationally-intensive analytical models are needed for circuit level reliability analysis. A conservative model for the analysis of interconnected trees has been previously proposed by Hau-Riege and Thompson [15] and verified for Al-based dotted-I structures. An extension of that model for Cu interconnects is presented in [9]. Assuming a constant and time-independent diffusivity along a segment, time to void nucleation, \( t_{\text{nucl}} \), and time to extrusion, \( t_{\text{extr}} \), can be expressed in closed form using the critical stresses \( \sigma_{\text{crit}} \) and \( \sigma_{\text{extr}} \) at the node. At each node, the stress evolution of the whole subtree must be considered instead of just the limbs that are immediately connected at the node. Each subtree is then replaced with a semi-infinite limb with an effective diffusivity and current density.

Once a void nucleates, it starts to grow and leads to a resistance increase in one of the limbs. Assuming that the void spans the whole width and thickness of the interconnect, the void length is written as a function of time. The time at which one segment exceeds an acceptable resistance increase is expressed as \( t_{\text{grow}} \) and calculated using a closed form expression. Equations are described in detail in [9].

The TTF due to void formation at a node, \( t_{\text{void}} \), is taken to be the maximum of \( t_{\text{nucl}} \) and \( t_{\text{grow}} \). This is based on the conservative assumption that when a void nucleates at \( t_{\text{nucl}} \), the void is already of finite size. Thus, equating \( t_{\text{void}} \) as the sum of \( t_{\text{nucl}} \) and \( t_{\text{grow}} \) leads to an over-estimate of the lifetime of the node. Similarly, the TTF due to extrusions at a node, \( t_{\text{extr}} \), can be derived by considering the critical compressive stress for dielectric failure. The TTF for the node, \( t_{\text{fail}} \), is then conservatively estimated to be the minimum between \( t_{\text{void}} \) and \( t_{\text{extr}} \). All the nodes of an interconnect tree are evaluated individually and the smallest \( t_{\text{fail}} \) is taken to be the lifetime of the interconnect tree.

5. Contrast with Hierarchical Al interconnect Electromigration Analysis

Failure mechanisms in Cu and Al interconnects are significantly different due to their different architectural schemes. In Al metallization structures, the Al line has refractory metal layers above and below and tungsten (W) filled vias are used to connect interconnects from different levels. The \( jL_{\text{crit}} \) product for Al is much higher as the failure mechanism is void growth limited. On the contrary, \( jL_{\text{crit}} \) products are lower, probabilistic, and asymmetric due
to differences between via-above and via-below trees. In Al technology, W-filled vias fully block electromigration between interconnect trees. Via classification is not required in hierarchical analysis flow for Al technology.

6. SysRel Architecture and Algorithms

SysRel is developed using Java 2 for platform independent operation. The infrastructure of the CAD tool is based on ERNI and ERNI-3D [5, 6]. In addition to layout files from Magic (a widely used layout tool in academia) format, SysRel requires input for process parameters and critical stress numbers for use in models. Current estimates in interconnect trees are based on simulation of the layout with standard simulation tools. Figure 2 shows the flow diagram of SysRel.

![Figure 2. Flow diagram of hierarchical reliability analysis in SysRel.](image)

SysRel is a GUI-based interactive tool requiring user input before initiating a process in the flow diagram, and outputs results at each stage. A user can select all or any particular metallization layer in a layout for tree extraction. Extracted trees are high-lighted along a display of statistics. After each filtering algorithm, immortal trees are high-lighted in green and discarded from further analysis. Time-to-failures of mortal trees are computed and individual trees are ranked. Finally, time-to-failures for different trees are combined using a joint stochastic model and full chip reliability metrics are reported to users. Figure 3 shows a screen shot of SysRel with FIT vs time and time vs cumulative % failure plots with the output window, layout window, and tree-rank table.

![Figure 3. Screen shot of SysRel with reliability metrics plots, layout and output windows, and tree-rank table.](image)

7. Full Chip Statistical Reliability Model

The full chip statistical reliability model is based on a probability function for interconnect trees. Of the different probability density functions, the lognormal distribution is of primary interest in describing electromigration failure. The median-time-to-failure, \( t_{50} \), and standard deviation, \( \sigma \), fully define probability density function, \( f(t) \), of the lognormal distribution. The cumulative distribution function, \( F(t) \), is given by the integration of \( f(t) \). Given the distribution functions, the failure rate, \( \lambda(t) \), is defined as

\[
\lambda(t) = \frac{f(t)}{1 - F(t)}
\]

\( \lambda(t) \) is the conditional probability that a \( t \) hour-old component will fail in an additional time \( dt \). The failure rate has a unit of [time]^{-1}. In the IC industry, failure rates are most commonly expressed in FIT (Failure unit). 1 FIT is 1 in 10^6 failures per 1000 hours or 1 in 10^9 failures per hour. Therefore, FIT can by obtained using

\[
FIT = \lambda(t) \times 10^9
\]

Taking the time-to-failure derived using the default model as \( t_{50} \) and \( \sigma \) from experimental results, we can model the life-times of individual interconnect trees using the lognormal distribution. For full chip reliability analyses, it is conservatively assumed that all the failure units are in series, i.e. the chip is considered to fail if any of the units fail. The cumulative distribution function and failure rate of such a series system with \( N \) components is then expressed as

\[
F_s(t) = 1 - \left[ 1 - F(t) \right]^N
\]

and \( \lambda_s(t) = N \lambda(t) \)

To understand the impact of an individual failure unit on full chip reliability, it is important to have a set of reliability metrics. As the electromigration failure (wear out type failure) essentially dictates the long range lifetime of a chip, we propose to conduct full chip reliability analyses based on a target lifetime, \( T \), for the whole circuit layout. Given a target lifetime \( T \), reliability metrics useful to designers are: probability of survival, FIT along
lifetime, maximum FIT, and time to cumulative % failed. These metrics are calculated using the series formula above. Lognormal distribution is not self-reproducing for a series system and the proposed metrics do not require any assumption on the system’s failure distribution.

8. Simulation Results from SysRel

A 32-bit unsigned integer comparator is designed using a design flow from behavioral description with VHDL to physical layout. The tools used in the flow are Design Analyzer (analysis and synthesis tool), Silicon Ensemble (place and route tool) and Magic (layout editor). An IIT standard cell library for TSMC 0.18um process is used for synthesis [18]. Total dynamic power reported in place and route tool from library cell characterizations is 26.6mW at Vdd=5V. It is also possible to use a circuit simulator, such as HSpice, for estimating power dissipation. For this reliability analysis, we used the power report from place and route tool. The layout has up to 4 layers of metallization; metal1 and metal2 for intra-cell routing, and all metal layers for inter-cell routing. Power delivery lines are in metal1 and metal2 in ring format (figure 4). The layout size is approximately 164um x 164um.

According to the ITRS roadmap, a $j_{\text{max}}$ value of 0.96 MA/cm² and a $T$ of 105°C are used [2]. While the signal lines in the design are stressed with bidirectional current, the $Vdd$ and $Gnd$ lines have the worst case unidirectional current density of 0.42 MA/cm². The $Vdd$ and $Gnd$ lines are identified in SysRel. Table 1 shows the hierarchical simulation results using SysRel.

<table>
<thead>
<tr>
<th>Step</th>
<th>Layout Extraction</th>
<th># of Interconnect Trees</th>
<th>Metal Plane</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2</td>
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<td></td>
<td></td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>Total number of Interconnect Trees = 1085</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Step 2</th>
<th>Via-based ($j_{\text{max},L}$) filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of immortal trees identified</td>
<td>970</td>
</tr>
<tr>
<td>Number of trees for further analysis</td>
<td>115</td>
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</tbody>
</table>

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<thead>
<tr>
<th>Step 3</th>
<th>Via-based ($j_{\text{local},L}$) filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of immortal trees identified</td>
<td>111</td>
</tr>
<tr>
<td>Number of trees for further analysis</td>
<td>4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Step 4</th>
<th>Default Model (with $\sigma_{\text{nucl}} = 40$MPa)</th>
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<tbody>
<tr>
<td>MTTF of each tree</td>
<td>23.2 years</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Step 5</th>
<th>Full chip stochastic analysis ($\sigma=0.81$, lognormal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target chip lifetime</td>
<td>10 years</td>
</tr>
<tr>
<td>Probability of no failure</td>
<td>0.525</td>
</tr>
<tr>
<td>Max FIT</td>
<td>15.4k</td>
</tr>
<tr>
<td>Time of max FIT</td>
<td>10 years</td>
</tr>
<tr>
<td>$t_{50}$ for full chip</td>
<td>10.35 years</td>
</tr>
</tbody>
</table>

Figure 4 shows the layout after the final simulation step when the mortal trees are marked. According to the analysis, $Vdd$ and $Gnd$ lines in metal1 are prone to electromigration failure.

Figure 4. Layout view of the 32-bit comparator in SysRel. The mortal Vdd and Gnd lines are marked.

However, the $Vdd$ and $Gnd$ lines in metal2 are filtered out due to the via-position and the value of $(jL)_{\text{crit,sat}} = 3700$ A/cm. SysRel allows a user to input critical parameters, such as $(jL)_{\text{crit}}$ and $\sigma_{\text{nucl}}$, to assess the impact on overall reliability. Table 1 shows the result for a particular set of such input parameters. The resulting full-chip reliability metrics are pessimistic due to the poor reliability of the $Vdd$ and $Gnd$ lines in metal1. Increasing the width of those particular lines from 2.5um to 5um and running the simulation again, SysRel predicts a $t_{50}$ of each tree of 92.9 years, a $t_{50}$ for the full layout of 41.4 years, and a maximum failure rate of 510 FIT after 10 years.

9. Future Work

In the current version of SysRel, the liners at the base of the vias are assumed to be fully blocking, such that each interconnect tree is a fundamental reliability unit. However, non-blocking vias may occur due to processing defects of high-aspect ratio vias, liner rupture during stressing [8], or deliberate etching through vias during fabrication. In such cases, two interconnect trees at different levels of metallization will be connected into a 3D interconnect tree through the non-blocking vias. Future version of SysRel will therefore include the possible occurrence of non-blocking vias. Another major extension will be the incorporation of non-uniform temperature along the full chip layout. Currently an
10. Conclusion

We have described a new hierarchical approach for predicting the reliability of Cu-based interconnects in circuit layouts, and developed a new RCAD tool, SysRel, for such an analysis of full circuit layouts. Based on the differences in electromigration failure mechanisms from Al technology observed from experimental work, we present a (jL) product filtering algorithm with a classification of separate via-above and via-below treatments. After the filtering of immortal trees, a default model is applied to remaining trees to compute reliability figures for individual units. SysRel utilizes new reliability metrics based on the desired lifetime of a chip and combines reliability figures from individual fundamental reliability units (FRUs). Such a system-level approach allows the assessment of the impact of each FRU on the overall reliability goal for a chip at the design level.

11. Acknowledgements

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12. References


