A Methodology for Chip-Level Electromigration Risk Assessment and Product Qualification

Chanhee Oh, Haldun Haznedar, Martin Gall, Amir Grinshpon, Vladimir Zolotov, Pon Ku and Rajendran Panda
Motorola Inc.
(Rajendran.Panda@motorola.com)

Abstract

Even after the successful introduction of Cu-based metallization, the electromigration (EM) failure risk has remained one of the most important reliability concerns for most advanced process technologies. Ever increasing operating current densities and the introduction of low-k materials in the backend process scheme are some of the issues that threaten reliable, long-term operation at elevated temperatures. The traditional method of verifying EM reliability only through current density limit checks is proving to be inadequate in general, or quite expensive at the best. A Statistical EM Budgeting (SEB) methodology has been proposed to assess more realistic chip-level EM reliability from the complex statistical distribution of currents in a chip [1]. To be valuable, this approach requires accurate estimation of currents for all interconnect segments in a chip. However, no efficient technique to manage the complexity of such a task for very large chip designs is known. We present an efficient method to estimate currents exhaustively for all interconnects in a chip. The proposed method uses pre-characterization of cells and macros, and steps to identify and filter out symmetrically bi-directional interconnects. We illustrate the strength of the proposed approach using a high-performance microprocessor design for embedded applications as a case study.

1. Introduction

EM is an intrinsic wear-out mechanism that occurs in the interconnect metallization tracks. It occurs when the current density is sufficiently high to cause the drift of metal ions in the direction of the electron flow, and is characterized by the ion flux density. This density depends on the magnitude of forces that tend to hold the ions in place, i.e., the nature of the conductor, crystal size, interface and grain-boundary chemistry, and the magnitude of forces that tend to dislodge them, including the current density, temperature and mechanical stresses.

EM failures arise if a void, created at a point where the flux of the outgoing ions exceeds the incoming flux, becomes large enough to cause an open in the metal line. A hillock, leading to a short to the adjacent or overhead metal runs, is caused when the ions are piled up at a point where the incoming ion flux exceeds the outgoing flux. Thus, failures occur when there is an asymmetry in the ion flow, caused by the afore-said factors. In addition to temperature and current density, one other key factor involved in the failure mechanism is the mechanical stress induced by ion-flux barriers where ion flow through a contact with a different material is inhibited.

The generally accepted EM failure model is described through Black’s equation [2]. Specific parameters pertaining to Cu metallization have been reported. Activation energies are typically on the order of 1.0 eV, and the current exponent has been found to be close to unity, the theoretical value for a single component diffusion system [3,4]. The translation of bi-directional, pulsating unidirectional, or any other arbitrary current waveforms into effective DC currents, commonly applied in experimental tests, is described in various studies such as [5,6]. Within the frequency range of 1 KHz to about 1 GHz, the equivalent effective current density for non-DC current waveforms seems to be represented by the average current model. This assumption is used in this present study.

Traditionally, EM reliability of chip designs has been targeted by controlling the current densities through design-rule limits that correspond to the desired reliability level. These limits are extracted empirically from the lognormal failure distributions derived in the accelerated life tests on discrete test structures, and assuming certain current distributions in the product. For example, a design guideline may assume that no more than one via or contact in the final product will be at or near the maximum current limit specified for that via. Although such EM current density limits help in guiding the design process, they do not necessarily guarantee the expected reliability of the final product for various reasons:

- Process variations present a certain reliability risk, which is strongly dependent on the design.
- For products requiring longer design cycle and targeting a new process under development, the current limit rules need to be provided early on, even at a time when the process has not fully stabilized. This may result in significant differences in the parameters of the process used in the final product.
for deriving design guidelines and the process used for final production.

- The assumptions about current distribution in the product on which the design guidelines are founded may be violated for products employing aggressive design styles, higher operating temperatures, extended lifetimes and/or more stringent reliability targets.

Since design-for-reliability (DFR) is meant to achieve an overall reliability goal for the chip, fixed limits for reliability-related design parameters governing interconnect sizing and via placement cannot, all by themselves, guarantee the targeted reliability for the final product. It is necessary to verify the product’s reliability level based on the completed design and using an appropriate statistical reliability model. [1] presented such an approach using an extreme lognormal (series reliability) model wherein the product’s life is estimated from the failure risk of the constituent failure elements (discussed later) in the product. The challenge in following through such a verification methodology is obviously the effort required to estimate accurate current distributions in the chip. The effort required is very high since failure risks should be estimated for every interconnect element in the design that can significantly influence the resultant lifetime of the chip based on the statistical model.

One of the early CAD tools to support EM reliability verification is provided in the “Berkeley Reliability Tools” (BERT) in which EM lifetime of a metal interconnect, contact, or via is computed from arbitrary current waveforms [7]. The currents are computed using a SPICE simulation of the circuit, which restricts the applicability of the tool to very small circuits. In [8], this method is improved using a faster simulation engine and also considering the interconnect temperature obtained through simulation of a lumped thermal model. [1] used the statistical reliability approach for verifying a high performance chip. Recently, [9] proposed a full-chip analysis methodology wherein a substantial number of nets are filtered using conservative current estimates derived from driver strength, correlated distributed drivers, capacitive load, and relative switching activity levels, and the remaining high-risk nets are simulated accurately for various charging and discharging situations. The approaches in [1] and [9] require simulating an extremely large number of interconnect and circuit structures, despite the filtering mechanisms, in order to get the wide coverage of failure elements required for accurate lifetime prediction. As such, the above approaches do not scale well with the growing size of the chip designs.

In this paper, we present a methodology for full-chip coverage of EM risk assessment of interconnects through much reduced simulation effort. The proposed method simplifies the task through two main ideas:

- identification of unidirectional and bi-directional current elements, and
- characterization of standard cells, off-the-shelf components, and macros to exploit repetition for drastically cutting down the simulation effort.

The practicality of the proposed methodology is demonstrated through a case study, which is a high-performance microprocessor utilizing a most-advanced, 0.13 µm process technology applying Cu/low-k interconnect schemes with nine metal levels.

The reminder of the paper is organized as follows: In Section 2 we present the EM reliability model used in our approach and discuss what failure elements are considered in the model. Section 3 describes the proposed methodology and Section 4 the results from the case study. Conclusions are presented in Section 5.

2. EM Reliability Model

In this section, we describe the statistical reliability model used in our approach and the failure elements determining the parameters of the model.

2.1 The model

The stress factor, defined as \( S = \frac{I_{act}}{I_{lim}} \) for each interconnect segment (called an edge) is determined by the method described in Section 3. Here, \( I_{act} \) is the actual effective DC-current through the edge and \( I_{lim} \) is the maximum current for that type of structure, as specified in EM guidelines. We define stress factor \( S_{mn} \) as \( n \)-th stress value of the \( m \)-th structure class and \( N_{mn} \) as the occurrence frequency (count) of \( S_{mn} \).

The lognormal probability density function for each stress factor \( S_{mn} \) within each structure class \( m \) is given by:

\[
    f(t) = \frac{1}{\sigma_{m} t^{s_{m}} A_{mn} \sqrt{2\pi}} \exp \left( -\frac{1}{2 \sigma_{m}^{2}} \left[ \ln \left( \frac{t^{s_{m}} A_{mn}}{t_{50,m}} \right) \right]^{2} \right)
\]

where \( k \) is the current exponent, \( \sigma_{m} \) is the standard deviation of the logarithmic failure times for that structure class, \( t_{50,m} \) is the median time parameter in which 50% of the population has failed in that class, and \( A_{mn} \) is the temperature acceleration factor at worst-case operating conditions for the \( m \)th segment in the \( n \)th structure class. This is to accommodate the temperature profile due to local Joule heating and ambient temperature shift. The acceleration factor follows the traditional Arrhenius behavior.

The next step is to compute the corresponding cumulative distribution function and survival rate for each
stress factor within each structure class for a given target lifetime \( t \), \( \sigma_m \) and \( t_{50,m} \) as specified by the user for each class. This function is given by:

\[
F(t) = \int_0^t f(t') dt'.
\]

The survival rate for a given structure class is then given by:

\[
SR_m = \prod_{n=1}^{k_m} [1 - F(t)]^{y_{nm}},
\]

where \( k_m \) is the number of stress combinations for the \( m \)th class.

Finally, the EM risk for each structure class is calculated using:

\[
\hat{R}_m = 1 - SR_m,
\]

and EM risk of the entire chip (over \( r \) structure classes) is obtained as:

\[
\hat{R} = 1 - \prod_{m=1}^{r} (1 - \hat{R}_m) = 1 - \prod_{m=1}^{r} SR_m.
\]

The failure times are assumed to be statistically independent.

### 2.2 Failure Elements

Since the above statistical model is a series reliability model, a failure of any element at risk is considered to result in the failure of the whole chip. Therefore, for computing correct lifetime of a chip it is necessary to define its elementary structures that are at risk. Moreover, it helps to exclude all other elements from the analysis as this reduces the overall computational complexity of full chip EM analysis.

Since the Cu ion flux divergence occurs at where contacts or vias interface with metal, only such interface locations are at the risk of failure. Thus we need to consider only those wire segments that have a contact or via at either end or both ends. Another consideration is the fact that only an effective direct current may result in EM failure. Alternating currents with frequencies in the GHz range cannot create EM failures due to the slow time constants of metal diffusion at typical operating conditions [6]. If the current consists of both high frequency AC and DC components, then only the DC component creates EM failures.

Even though a chip uses direct current, many of the interconnect wires see only alternating current. Figure 1 shows a typical signal wire which is driven at one end and loaded at the other. After an equal number of rise and fall transitions, no segment of this wire (outside of the driver and load cells) would see a non-zero effective direct current through it as the electric charges carried forward and backward on this wire due to charging and discharging of the load capacitance are bi-directionally symmetrical.

The situation can be different, for example, in Figure 2 which shows a signal driven by two 3-state drivers. If one of the drivers always has transitions only between 0 and \( Z \) (high-impedance state) and the other only between the \( Z \) and 1, then asymmetrical charging and discharging paths are created. As a result the signal wire in this case can be expected to see an effective DC current.

Based on this simple observation, we can exclude all signal wires routed between cells and driven by non-three-state cells from the EM analysis. In fact, a vast majority of signal interconnects is of this type. This elimination helps to avoid full chip parasitic extraction and significantly reduces computational complexity of full chip EM analysis.

Another important phenomenon is the so-called Blech-effect [10]. It has been shown that no EM damage occurs below a critical interconnect length, given a certain current density. Accurate computation of the Blech-effect in complex interconnect tree and mesh structures requires constructing and solving a system of linear equations such as reported in [11]. Taking into account the Blech-length effect helps reduce the pessimism of the EM analysis significantly, because many wires in the cells are relatively short. However, experimental validation of the Blech-effect under pulsed operation in Cu-based interconnects has not been reported to our knowledge. Our methodology includes this step. Details will be reported in a forthcoming publication once an experimental validation under pulsed DC conditions has been obtained.

### 3. Proposed Methodology

Our EM risk assessment methodology adopts a cell-based analysis approach to effectively handle the large
data volume in typical chip designs. It consists of multiple functional components for: (1) pre-characterization of current on signal and power wires inside simple cells, (2) computing current on signal and power wires inside complex cells and custom macros by analyzing individual instances, (3) computing current on global signal wires, and (4) computing current on global power wires.

A flow diagram of our methodology is shown in Figure 3.

**Figure 3. Flow diagram of methodology**

Computations of average currents for wires inside cells and blocks are accomplished with different techniques depending on the complexity of their design: A cell which has only one output is considered as a simple cell, and the currents in the intra-cell wires are computed by first pre-characterizing the cell and then by scaling the wire currents based on the load and switching activity on the output. Load capacitances for the outputs are obtained from chip-level RC extraction, which includes all inter-cell wires. Switching activity (which is defined as the average number of switching transitions a wire experiences during a clock cycle) is obtained by collecting toggle counts on wires from the traces of chip-level functional simulation. Since simple cells are basic elements for design and typically are instantiated many times across a chip, this pre-characterization approach provides an extremely efficient analysis method.

Cells or custom-designed blocks which have more than one output are considered as complex cells. For complex cells, the pre-characterization approach is not practical due to potential dependence of wire currents on multiple output loads. In our approach, we perform separate cell-level current calculations on each instance of complex cells by applying actual loads and switching factors. Switching activity values for wires internal to complex cells are required for current computations, but typically not available from chip-level simulations. We assume a switching activity of 1 for all data wires and 2 for all clock wires to ensure that our current computation is conservative. Since the number of multi-output cell instances is typically much smaller than that of single-output cell instances, performing detailed current computations for each complex cell instance did not present a difficulty in terms of run times.

In addition to the current computation for intra-cell wires, parasitic extraction and EM analysis is also performed on the segments of global wires between cells and blocks. Since this does not require the detailed view of cells and blocks, the analysis is significantly simplified.

As said before, global wires driven by multiple three-state drivers may experience unidirectional current under both charging and discharging scenarios and are susceptible to EM failure. As long as three-state and non-three-state drivers are identified, our EM current computation automatically detects any unidirectional current by computing worst case current over all possible driving scenarios. To achieve this, we determine the driver type by analyzing the logic function of each driver during the pre-characterization of cells, and apply it during chip-level analysis. In some high speed designs, the use of three-state drivers at chip-level is limited due to timing concerns, and hence only a small number of global wires experience unidirectional current.

### 3.1 Techniques of current computation

For computation of average wire currents on signal nets, we use the charge flow-based model presented in [12]. By representing a driving gate and capacitive elements with charge sources, we obtain a linearized model where it requires only one solution per interconnect on a linear system of equations to compute all wire currents. Since the method does not require time-consuming transient analyses, it can efficiently analyze large chip-level interconnects as well as numerous intra-cell interconnects. Additionally, by considering a time interval during which an interconnect is undergoing opposite types of transitions (i.e. RISE and FALL) and different possible switching scenarios, the average current computation also makes it easy to determine if a wire segment has either unidirectional or bi-directional current. Non-zero average current indicates that there is a unidirectional current component due to the asymmetry in the charge flow during transitions.
Figure 4 shows the circuit transformation for average current computations according to the model. For further details refer to [12].

![Figure 4. Circuit transformation for average current computation](image)

3.2 Scaling of intra-cell currents with switching activity and load caps

A typical chip design contains millions of cells. For efficient computation of intra-cell currents on each instance of such cells, we take advantage of the fact that the average current on an output wire and supply wires is linearly dependent on its signal activity and load capacitance. We assume that currents on internal (i.e. non-output) signal wires are not dependent on output load since the variation due to the output load is small and can be ignored. Then, the average current on a wire can be represented as:

\[ I_{\text{avg}} \propto (S \cdot Q_{\text{max}} / T), \]

where the maximum net charge flow during charging and discharging, \( Q_{\text{max}} \), is linearly proportional to load capacitance. \( S \) and \( T \) represent signal activity and clock period, respectively.

Each single-output cell is pre-characterized for EM by computing the average current for each wire for 2 pre-determined output load values, and then fitting a line through the data points. During pre-characterization, the signal activity is assumed to be 1 (i.e. one transition per clock cycle).

Then, actual wire currents in each cell instance are computed simply by scaling the current values from the characterized data for the cell based on actual load and actual signal activity on the output net, as shown in Figure 5 (only capacitance scaling is shown).

![Figure 5. Current scaling according to cell load capacitance](image)

3.3 Estimation of Currents in Global Power Wires

Currents in global power routes (i.e. routes outside cells and blocks) are obtained using a full-chip power grid simulation tool described in [13]. The simulation uses a mix of dynamic current traces and average current estimates obtained from transistor-level and gate-level power simulations of cells, memories and custom macros.

4. Case Study

The proposed methodology was applied to a high-performance microprocessor design for embedded applications. The total power consumption at 105°C junction temperature, 1.3 V, and 1.3 GHz is about 27 W. This design encompasses a total of 286 million contacts and vias. A commercial extraction tool was employed to extract parasitic and geometric (width) information of power and signal routes. An in-house signal EM checker [12] was run on this data to generate the average DC currents for clock, signal, and power nets as inputs to a post-processor. There were a total of 269,978 global interconnects with no EM risk, since bi-directional currents with zero effective DC was flowing through them. The unidirectional nets were almost entirely internal to nets, especially at the output stages of the driver cells.

<table>
<thead>
<tr>
<th>Structure Class</th>
<th>( S_{\text{max}} )</th>
<th>( N(S_{\text{max}}) )</th>
<th>Structure Count at Risk</th>
<th>EM Risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>0.93</td>
<td>2</td>
<td>40,514,845</td>
<td>0</td>
</tr>
<tr>
<td>M2</td>
<td>0.62</td>
<td>2</td>
<td>13,130,690</td>
<td>0</td>
</tr>
<tr>
<td>M3</td>
<td>0.48</td>
<td>2</td>
<td>700,472</td>
<td>0</td>
</tr>
<tr>
<td>M4</td>
<td>0.12</td>
<td>2</td>
<td>20,114</td>
<td>0</td>
</tr>
<tr>
<td>M5</td>
<td>0.16</td>
<td>1</td>
<td>13,677</td>
<td>0</td>
</tr>
<tr>
<td>M6</td>
<td>0.0021</td>
<td>1</td>
<td>1,258</td>
<td>0</td>
</tr>
<tr>
<td>M7</td>
<td>0.00013</td>
<td>1</td>
<td>432</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 1 shows the EM-risk calculation results for all the nets with non-zero DC, based on the currents flowing...
through metal edges connected to contacts and vias, and as determined by the post-processor. Column 1 refers to the structure class, column 2 reports the highest stress factor, $S_{\text{max}}$, column 3 gives the number of links $N(S_{\text{max}})$ at that stress factor, column 4 counts the total amount of structures at risk in a specific class, and the last column gives the EM risk based on actual, experimental data. The target life for the embedded application is 10 years. The cumulative failure target is $F=0.1\%$ for the product population.

Another run first utilized an in-house power-analysis tool [13] to provide the current information through every piece of wire segment in the power distribution network. These were then fed to the post-processor to determine the EM risk on the power grid as well. The results are shown in Table 2.

**Table 2 Data for the power grid (same conditions as in Table 1):**

<table>
<thead>
<tr>
<th>Structure Class</th>
<th>$S_{\text{max}}$</th>
<th>$N(S_{\text{max}})$</th>
<th>Structure Count at Risk</th>
<th>EM Risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2</td>
<td>0.092</td>
<td>1</td>
<td>582,000</td>
<td>0</td>
</tr>
<tr>
<td>M3</td>
<td>0.11</td>
<td>5</td>
<td>216,295</td>
<td>0</td>
</tr>
<tr>
<td>M4</td>
<td>0.1</td>
<td>1</td>
<td>114,922</td>
<td>0</td>
</tr>
<tr>
<td>M5</td>
<td>0.088</td>
<td>1</td>
<td>160,864</td>
<td>0</td>
</tr>
<tr>
<td>M6</td>
<td>0.06</td>
<td>1</td>
<td>167,815</td>
<td>0</td>
</tr>
<tr>
<td>M7</td>
<td>0.14</td>
<td>1</td>
<td>95,122</td>
<td>0</td>
</tr>
<tr>
<td>M8</td>
<td>0.21</td>
<td>1</td>
<td>197,926</td>
<td>0</td>
</tr>
<tr>
<td>LM</td>
<td>0.14</td>
<td>1</td>
<td>318,827</td>
<td>0</td>
</tr>
</tbody>
</table>

Tables 1 and 2 indicate that most of the EM risk is concentrated in the lower levels of the 9-metal stack. The DC components for signal and clock nets decrease rapidly towards the upper levels in the hierarchy, whereas the power grid shows a relatively even current distribution. The power route metals showed much less maximum current stress due to much higher metallization to contain the IR drop. The main result of this study is the fact that only few failure links come close to the EM design guideline, and that the vast majority of stress factors are below the guideline limit. It has to be noted that the number of failure links at the maximum allowed design current strongly depends on the choice of these values. If lower design guideline limits are used, the effective number of links at these limits can quickly approach values of 1000 or more.

For this chip design which contains more than 56 million transistors, not counting fingered devices, the wire current calculation required about one hour on 3 workstations. The power and ground analysis was done in about 3 hours. Once the wire currents were computed, the EM-risk determination for all structure classes and the full-chip took less than an hour on a single workstation.

**5. Conclusions**

A cost- and time-efficient, full-chip EM risk assessment method was developed and applied to a high-performance microprocessor. The results indicate that most of the EM risk is concentrated in the lower metal levels. If aggressive design guideline limits based on highly reliable Cu-metallization processes are implemented, only few failure links approach the maximum allowed currents. However, this result changes if low design limits are chosen. The calculated life of the high-performance chip presented here, based on the presented methodology, is 104 years for a cumulative failure of $F=0.1\%$. Alternatively, the chip can be operated at 140°C if the target life of 10 years is kept as the limit.

**References**


