Low Power 260k Color TFT LCD One-chip Driver IC

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Abstract

In this study, we present a 260 k-color TFT LCD one-chip driving IC that consumes under 5 mW in the module, which is exceptionally low power consumption. To reduce power consumption, we used many power-lowering schemes in the logic and analog design. A driver IC for driving LCDs has a built-in graphic SRAM. Besides write and read operations, the graphic SRAM has a scan operation that is similar to the read operation of one row-line, which is displayed on one line in an LCD panel. Currently, the embedded graphic memory is implemented by an 8-transistor leaf cell and a 6-transistor leaf cell. We propose an efficient scan method for a 6-transistor embedded graphic memory that is greatly improved over previous methods. The IC is implemented in a 0.18 um process. The 0.18um mixed process is firstly used in

1. Introduction

Current telecommunication technology has improved amazingly. These improvements have revitalized handheld modules and increased services. Because of this, it is even more important that the chip enable voice communication, data, graphic images, and moving pictures. To use a handheld module for a longer time, each chip needs to become smaller and consume less power.

Improvements in telecommunications have made display technology improve too. The size of display equipment has become bigger and the resolution higher. Due to this, power consumption of display equipment has also become higher. Power reduction for display equipment has become a very important issue. The display equipment in handheld phones is super twisted nematic (STN) and thin film transistor (TFT) LCDs. Electro-luminescence will be a practical utility. Display material can have an altered arrangement according to the level of voltage or the amount of current. In accordance with the arrangement, the rate of a transmission changes. We can control the brightness of a display panel, and the black/white display panel is implemented with this method. The multi-color display panel is implemented by arranging an RGB(red, green and blue) color filter. The color rectangular panel is supplied by row-direct voltage and column-direct voltage. The difference of the two direct voltages is the driving voltage of the pixels. This method is called multiplex addressing. The LCD driver IC generates and supplies the voltage level.

This paper presents a 260 k-color TFT LCD one-chip driver module that consists of a gate driver and source driver. The gate driver generates the driving voltage of column direction and common voltage. Figure 1 shows how the TFT array is constructed. The gate driving voltage is of two types: a selected level and a non-selected level. The level of these voltages is determined by the characteristics of each panel. When one gate line is selected, the source IC drives data voltage levels that are valued by decoding stored data. The different voltage of the gate’s selected level and source’s data level determine the display material arrangement.

Currently, the LCD panel is implemented in mono, 4-gray, 256-color, 65k-color, and 260k-color for handheld phones. With a higher color resolution, the embedded memory capacity needs to be bigger in the LCD driver IC. With a larger memory capacity, the metal line from the logic part to the memory needs to be longer. Because of this, the embedded graphic memory-addressing block, the embedded graphic memory control block in the logic, and a time control block in the embedded graphic memory becomes more important in designing the embedded graphic memory. The internal control block in the embedded graphic memory is especially important in AC characterization. The power consumption of the merged memory also becomes a very important issue. With a higher resolution and bigger panel, a bigger embedded memory size is necessary. Because of this, shrinking the RAM size is a dominant factor in the chip size of a driver IC. Because of these factors, the architecture of the embedded memory was improved from a 8-transistor SRAM architecture to a 6-transistor SRAM architecture.

In this paper, section II presents the architecture of graphic driving IC. Section III discusses the architecture of the 8-transistor/6-transistor embedded graphic SRAM and the architectural defect of the write/read/scan method in 6-transistor architecture. In section IV, a low power scan method in 6-transistor architecture is proposed. In this chapter, another low power accessed method is proposed. In Chapter V, the implemented sample is compared in power
consumption. The chip samples are implemented in a 0.18 um process and tested in manual board

**Figure. 1 TFT one-chip driver IC diagram**

2. Structure of the driver IC

Generally, the driver IC is composed of a logic part, an analog part, and a memory part. The analog part is composed of the LCD driver, DCDC converter, voltage divider, and oscillator. The oscillator circuit generates a clock for display. The DCDC converter circuit receives the generated clock and generates the highest/lowest voltage level. The voltage divider circuit divides between the highest and lowest level. The driver block supplies the various voltages to the panel. Figure 1 is a block diagram of the implemented 260k TFT one-chip IC. The 260k TFT one-chip IC is composed of a logic, a merged memory, an oscillator, a DCDC converter block, a source/gate driver block and a common voltage generating block.

The logic part is composed of an MPU interface block, memory-addressing block, and timing control block. The MPU interface block interfaces between the driver IC and the external MPU. The memory-addressing block receives the decoded signal in the MPU interface and generates the memory address. The resister array is included in the gray scale generator. The implemented driving IC has three types of adjustment: a gradient adjustment, an amplitude adjustment, and a fine adjustment. The timing control block generates a signal, which controls the display panel.

The gate driver block drives the gate on/off level voltage (VGH/VGOF). The each voltage generating block sequentially generates each voltage. (Fig.2). The TFT panel must have a capacitor for storage. The driving method is a two-type per capacitor connection that is named the capacitor for storage in a TFT panel (CST) on the gate and the CST on the common.

The embedded memory is the same as normal memory. In addition, the embedded memory has the operation of accessing whole-bit cells in the X-address. The output data from memory is transferred to the source driver. The source driver drives the panel with the voltage level, which is decoded by the accessed data. One time, the gate driver circuit selects one line of the panel. The next time, the gate driver circuit selects the next line, and the embedded memory transmits a whole-bit cell in the next X-address. The gate driver circuit selects a next-column line. With this accessing process, one line of the LCD panel is displayed.

**Figure. 2. Sequence of the voltage generator**

The implemented 260 k TFT driver IC is assembled as in Fig. 5. The implemented IC is contacted with the panel’s chip-on–glass (COG).

3. Structure of graphic memory

The embedded graphic SRAM is composed of a bit cell core block, I/O & pre-charge block, a control block, a scan line decoding block, a word-line decoding block, a scan latch block, and several buffer blocks. The bit core block stores display data. The I/O & pre-charge block controls charging and discharging of the bit/bitb line. The scan/word line-decoding block controls the word-line cell in the bit core block. This block accesses stored data and stores data. The scan-latch block does scan operations.

The control block receives external write/read/scan enable signals from the address-generating block of the logic part and regenerates ram internal signals. The received-origin signal is transferred through a long metal line and the length of the metal line differs. Because of this, the write-enable signal of the most left word-line block can have a time gap with the most right word-line block. The slope of the external signal through the long metal line is low and the driven gate...
of the sloped signal consumes more power. If the origin signal is used without refining the I/O block and word-line block, the operation of the memory is unstable. Because of this instability, as the higher storage memory is embedded, regenerating the timing becomes more important.

The regenerated signal enables the access operation when the bit/bitb line is perfectly stable. The control block has an auto-detect circuit, which detects the bit/bitb stable time. In the 8-transistor graphic SRAM architecture, the read/write operation is the same as in a normal SRAM. However, a leaf cell has two additional transistors, which directly connect to the storage path. Because the additional two transistors are connected to the storage cell independently of the bit/bitb line, the 2-transistor can independently access stored data. The additional transistor with a different access path makes it possible to access storage data even though write/read is operating. Because the 8-transistor has an independent scan operation, the memory access logic for the embedded graphic SRAM is simple. However, because of the additional 2-transistor, the chip size is bigger than the 6-transistor graphic SRAM. In a mono STN driver IC and a low-resolution multi-color STN driver, the embedded graphic SRAM size is not dominant in a full chip. As the panel becomes bigger and the resolution becomes higher, the size of the embedded graphic SRAM becomes dominant in the driver IC. Due to this, currently, the 6-transistor embedded graphic SRAM is used in 256/65 k/260 k color driver ICs.

The RAM accessing logic block must control write/read timing and scan timing. The scan enable signal must be masked and the duration of masking is the writing time. In the writing time, the addressing block must transfer the writing address to the RAM. When the mask time is removed, the scan signal is transferred and the scan address must be transferred. The logical times can be a critical time violation and can cause a redundant signal. During the scan operation, the additional sense amplifier operates and the bit/bitb lines are discharged. Because of this, the 6-transistor architecture is inferior in power consumption.

4. Structure of graphic memory

In a general graphic SRAM, the power consumption of the write operation is overlooked. As the capacity of the graphic SRAM and panel size becomes bigger, the power consumption of graphic SRAM blocks is important issue in driver IC. Because of this power consumption, it is necessary to shorten the graphic SRAM internal transition time.

Normally, the signal of the external logic block has a long time period because of the timing margin. The embedded graphic SRAM receives the external signal and re-generates the optimized time signal, which is a shorter select time of the word line than the normal select time. The optimized time is a decision in time that the read/write operation is stable. This means that the bit/bitb has enough of a voltage level gap. If the bit/bitb gap is high, the power consumption is high and the memory operation is stable. If the bit/bitb gap is low, the power consumption is low and the memory operation is likely to be unstable.

This method is efficient for reducing power consumption because the open-time of a path from the bit/bitb to the leaf cell is shortened. This method can be used in the scan operation. This method can also reduce the time of the sense amplifier operation and word-line select[11]. In the scan operation of the 6-transistor embedded graphic SRAM, the power consumption is bigger than the 8-transistor graphic SRAM because column-direction connected bit/bitb cells are wholly charge/discharge. The scheme of the regeneration time is necessary in the embedded graphic 6-transistor memory.

Normally, the generated clock by an internal oscillator determines the scan clock and the frequency of the scan clock determines the display frame frequency. Because the frame frequency is normally several tens Hz which is a much lower frequency than the writing frequency of a moving picture, if the write and scan signal occur simultaneously, the scan signal must be masked by the writing signal.

Figure 5 describes the masking operation when the

![Figure 4. Comparison of 8-tr scan and 6-tr scan.](image-url)
scan signal and the writing signal occur concurrently. The write/read address and scan address are independently generated and supplied by the masking signal. While the scan signal is masked, the write signal is applied to the graphic SRAM. The other scan signals, except the first scan signal, access the same data as the first scan data. This method is not efficient, so we propose removing the redundant scan operation [11]. This method can reduce the redundant toggling scan signal and can deduce the power consumption of redundant toggling.

In this paper, we present more advanced method of the power saving. The case 1 of [Fig.6] is that the scan enable signal is generated during operating of wiring. The first input detect circuit decides the first signal and then the first input signal let the operation be active. The later input signal is hold in a waiting circuit. And then, the first operating is finished, the information signal of the finish input signal is applied to the first scan signal and then the signal is generated during operating wiring. The first power saving. The case 1 of [Fig.6] is that the scan enable signal is independently generated and supplied by the masking signal. The write/read address and scan address are concurrently executed. And each memory block has time control generating block. The time control generating block re-generates the write/read/scan signal from the write/read/scan signal of the logic. The re-generated write/read/scan signal can reduce the consumption of power in memory.

The oscillator circuit is located in between the memory block and the gate driver block. The gray scale block is located in the left part of the logic block. The source driver block is located above each memory macro-block. The four-quarter sides are wrapped by a pad.

The embedded graphic 646,272bit memory block is divided by 3 macro-blocks because of the reduced height of the chip and the metal delay. The optimization of the height and length is an important factor in the number of a net-die. Each macro-memory block can be selected by a select signal when the read/write signal is supplied. This method reduces memory access power. Scan operating can be concurrently executed. And each memory block has time control generating block.

The test is accomplished in a Q-tab manual test board. The power consumption is measured at 2.8 V. Table 1 describes the consumed current of only the logic part at the writing time at display-on. In the previous chip, power consumption is 1.1mA in 4MHz. In the presented chip, power consumption is 0.230mA. The 79% power consumption of the previous chip is reduced in the presented chip.
The writing and scan test is accomplished by a manual board with a PC interface. The write time is supplied in 4 µs, which is the minimum clock in the PC. In one scan enable duration, the total number of the minimum writing is 2, which is the scan method in previous algorithms.

Figure 8 is the module test environment. The basic signal is generated in a PC and the high-speed signal is generated in an FPGA board.

![Figure. 8 Module display.](image)

6. Conclusion

Currently, improvement in display resolution and panel size increases power consumption in driver ICs. In this paper, we proposed two methods that reduce the power consumption of access in an embedded graphic SRAM.

The first method is a regeneration time method, which receives access signals from the external logic and regenerates the optimum time. This method can be applied in the embedded graphic SRAM.

The second method removes the number of redundant scan signals. This method removes the number of redundant accesses and can be applied in a logic block. The efficiency of the proposed method is verified in the 0.18 um process. The total power consumption in the module is under 5 mW at a 2.8 V supply. Power consumption is measured in a normal display. The module is efficient in handheld equipment.

7. References


<table>
<thead>
<tr>
<th>Current (µA)</th>
<th>Previous scan mask method(4Mhz)</th>
<th>Presented method(4Mhz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1mA</td>
<td></td>
<td>0.230mA</td>
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