Abstract

A new solution to improve the testability of high resolution \( \Sigma \Delta \) Analogue to Digital Converters (\( \Sigma \Delta \) ADC's) using the quantizer input as test node is described. Both, the theory of the method and results from high level simulations for a 16 bit audio ADC example are presented. The analysis demonstrates the potential to reduce the computation overhead associated with test response analysis versus conventional techniques.

1. Introduction

Testing high-resolution mixed signal interface circuits in production requires high accuracy testers, large data storage resources and processor intensive response analysis. Test time, infrastructure and cost per device is therefore currently too high for this class of function. Much effort has been put into addressing this problem [1-8] but to date, there have been no major breakthroughs. Recently a more specific analysis [8, 9] into the effectiveness of specification testing for a generic class of high resolution interfaces has been carried to identify the ATE support required for testing high resolution virtual components (ViC’s) along with the possibilities for both partial and full Built-In Self-Test (BIST).

In this work the focus is on how to simplify and to accelerate the testing of high order sigma-delta converters for audio applications without degradation in the test quality. The proposed method uses the so-called noise transfer function of the converter as figure of quality. In practice this is achieved by a stimulus injection into either the primary input and the quantizer input and a subsequent spectral analysis of the ADC output. The technique supports the measurement of three important specifications: gain, noise, and distortion.

Following a brief description of the theory of oversampling converters in section 2, section 3 will discuss the noise transfer function method and present results from high level simulations to demonstrate the applicability of the method. Section 4 will draw conclusions.

2. Sigma-Delta Modulator

The oversampling converter contains a feedback loop in which the input \( x \) of the converter is compared with the output \( y \). The difference is then used to generate the output \( y \). Figure 1 illustrates the basic architecture. In the noise-shaping system of fig. 1, as will be shown later, the output \( y \) contains the converted but otherwise unmodified input \( x \), plus a filtered replica of the quantization error \( e \) introduced by the A/D converter function. The filtering suppresses \( e \) in the signal band. A digital filter is then used to separate the signal \( x \) from the noise \( n \) contained in \( y \) [10].

![Figure 1](image)

Figure 1  Noise shaping converter

Each output word from the oversampling converter is effectively a weighted average of many consecutive analogue input samples, and thus it is not practical to establish a direct mapping between an individual sample and the digital output. Hence, the performance of the function is measured by either comparing the input and the output spectra in the frequency domain, and/or the complete input and output waveforms in the time domain. From those comparisons the rms values of the signal and noise can be found and the signal-to-noise ratio SNR can be calculated. The SNR is determining the system resolution \( R \) which can be estimated from the approximate relation:

\[
R(\text{bits}) = \frac{\text{SNR(dB)}}{6} \quad (1)
\]

The linearity of the oversampling converter can also be characterized through the ratio of the signal power \( S \) and the total harmonic distortion power \( \text{THD} \).

If the transfer function \( H(z) \) of the analogue loop filter is modelled as a sampled-data analogue accumulator (e.g.
by a switched-capacitor integrator), and the additive noise is modelled by a quantizer, then an equivalent architecture like in fig. 2 can be used to model the modulator function. This linearized model can be analyzed in the z-domain.

**Figure 2** Delta-sigma modulator loop

The output is given by:

\[ Y(z) = H_S(z)X(z) + H_N(z)e(z) \]  

(2)

where \( H_S \) and \( H_N \) are the signal and noise transfer function functions, respectively. They are calculated from

\[ H_S(z) = \frac{H_a(z)}{H_a(z) + 1} = z^{-1} \]  

(3)

\[ H_N(z) = \frac{1}{H_a(z) + 1} = 1 - z^{-1} \]

where the latter parts of the equations follow since here the loop filter transfer function is:

\[ H_a(z) = \frac{z^{-1}}{1-z^{-1}} \]  

(4)

Thus, the digital output contains a delayed replica of the analogue input signal plus a noise component \( e \) shaped by the noise filtering function due to \( H_N \)

\[ |H_N(e^{j\omega T})| = 2 \sin(\omega T/2) \]  

(5)

where \( T = 1/f_s \) is the sampling period.

\( H_N \) in eq. (3), is clearly a high-pass filter function (fig.3), and hence it tends to suppress the quantization noise at low frequencies including the base-band, but enhances it near \( f = f_s/2 \). Thus, the noise power is swept out of the base band (where it would have overlapped with the signal) and into the high frequency range where it can be removed by digital low-pass filtering [10, 11]. The in-band noise power \( P_N \) of the delta-sigma modulator can be estimated from its linearized model (fig. 2). From eqs. (1)-(3), assuming \( \omega T << 1 \), the in-band noise power can be evaluated as:

\[ P_N = \int_0^{f_s} |H_N E|^2 df \]  

(6)

and for a first order delta-sigma it is:

\[ P_N = \int_0^{f_s} |H_N E|^2 df \approx \pi^2 \frac{2f_a}{36} \left( \frac{2f_a}{f_s} \right)^3 = \left( \frac{\pi A}{6} \right)^2 (OSR)^{-3} \]  

(7)

The noise-shaping function \( H_N(f) \) can be made more selective by using a higher-order loop filter. Two cascaded integrators are needed to realize a second-order loop filter, three to realize a third-order one, etc... To maintain the stability, the open-loop transfer function of the loop (which has all its poles at \( s=0 \) due to the cascaded integrators) must also have some finite zeros so that at the unity gain frequency a proper phase margin can be maintained [11].

Each loop in the higher order converter contains a delay. Delay-free loops are usually impractical, and two or more delays in a loop tend to impair the stability and hence also the SNR performance of the system [10, 11].

The sigma-delta system can also generate low-frequency (and then in-band) tones for special values of the input \( x \). This is generated by the periodic DAC output pattern that in average can equal \( x \) and hence the loop can settle into a steady state oscillation under these conditions. If the fundamental of this oscillation falls into the signal band, it may appear as a sine-wave tone of considerable amplitude in the final data output. This tone is called pattern noise and appears as sharp peaks in the output spectrum and a sharp dip in the SNR vs. \( |x| \) characteristic [10].

From this theory an important conclusion arises that the quality of the converter is dependent on the noise-shaping function and that thus, from it important information about the dynamic performance can be derived.
3. Testing the $\Delta \Sigma$ A/D by using the Noise Transfer Function

The test approach proposed here uses the noise transfer function (NTF) of the converter graphically represented in figure 3, to measure three important specifications of the ADC, which normally strongly impact the test time: gain, SNR and THD.

These measurements are executed by performing an FFT on the output signal, while at the quantization noise input (fig. 2), a sine wave of suitable frequency (test input signal in fig. 4) is injected as test signal. The node is normally accessible since often used to compensate the internal converter leakage.

In the remainder of this section, the method will be described using a high order 16 bit audio $\Sigma \Delta$ converter with a 24kHz bandwidth and clock frequency of 3.07 MHz. Results from high-level simulations [13] are presented for each of the specification measurements investigated.

3.1. Gain Evaluation measuring the Noise Transfer Function Attenuation

As described in the theory, the path from the quantizer node to the output of the modulator is effectively a high pass filter as described by eq. (3). This function attenuates the signal injected into the quantizer node in the band frequency. By using this concept, each signal injected into this node will be attenuated as well as the quantization noise in the signal band. The test procedure is then the same as the one used to test the attenuation of a high pass filter. The technique involves the injection of a sine wave of a known frequency into the so-called SUM node in fig. 4, within the converter bandwidth, in the example 24kHz. The analysis of the response essentially requires a comparison of the amplitude of the fundamental spectral line in the output spectra with the input amplitude. Knowing the amount of the expected attenuation to the chosen frequency, it is possible to evaluate the deviation from it and then the real attenuation or the gain. The measurement can be repeated several times to achieve better accuracy.

The amplitude of the sine wave is not crucial in this technique. The simulation results showed that for a 16 bit accuracy a test time of 0.05s is required which is half than the 0.1s generally required to measure the gain of the converter. This measurement is strictly related to the gain evaluation (as can be derived by the eq. 3) of the converter and can be considered as a substitute.

3.2. SNR Measurement

Another measurement which is possible by using the same test access, is the SNR evaluation. Considering the case where no signal is applied at the input of the ADC and a test signal injected into the test input, a spectral analysis (FFT) of the output, will contain only the in-band noise still present after filtering, plus the attenuated spectrum of the injected test signal. If a low pass filter (see red curve in the fig. 5) is used to amplify and extract the in-band spectral components, it is possible to evaluate both the quantization and the pattern noise.

The effect of applying the test signal to the new test access SUM is that on the output, the amplitude of the test stimulus is now attenuated as well as the noise in the signal band. Choosing the correct frequency for the test signal it is possible to increase the amplitude of the noise relative to the test signal. This simplifies the noise evaluation computations. The spectral line of the test signal can also be eliminated by a (digital) notch filter around the test signal frequency. However, this will have a slight impact on the in-band noise power.

Figure 6 shows the FFT over 65,536 samples at the output of the fourth-order single loop converter, when a sine wave of 20 kHz is used as test stimulus. The test signal (20kHz in fig.6), is attenuated and shifted in frequency increasing the visibility of the noise component. In tab. 1 the evaluation of $S/(N+\text{residual THD})$ is shown making use of a FFT for different numbers of points, when just an in-band amplification of 10 is considered. It is possible to...
see that the same result can be achieved with only 16.384 samples only loosing 0.5 dB of accuracy. By improving the low pass filtering and amplification, an additional reduction on the number of points can be achieved. The FFT evaluations have been carried out at the output of the modulator without post processing (low pass filtering) to reduce the noise level respect the signal, achieving anyway the noise reduction directly at the output of the decimator by its transfer function.

Comparing the method with the conventional technique, the computation time is significantly reduced since no curve fitting is required and the test waveform generation does not require sophisticated equipment.

From this measurement it is possible to directly obtain the in-band noise power, eq. (6), plus the total harmonic distortion. This is however not the dominant component since the most significant source of THD is the first integrator which has no effect as no signal is applied at the input of the converter. The resolution of 90dB, without in-band noise amplification can be achieved with 16.384 samples.

### 3.3. Measuring the THD

The evaluation of the THD cannot be achieved directly and still requires additional work to correlate with the electrical performance.

**Figure 6** FFT over 65536 samples: $S/(N+\text{THD})=0.6\text{dB}$.

**Table 1** Summary of the simulations results

<table>
<thead>
<tr>
<th>Samples</th>
<th>$S/(N+\text{residual THD})$ [dB]</th>
<th>Residual THD [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>65536</td>
<td>2.8</td>
<td>135.2</td>
</tr>
<tr>
<td>16384</td>
<td>3.4</td>
<td>135.6</td>
</tr>
<tr>
<td>8192</td>
<td>7.7</td>
<td>135.2</td>
</tr>
</tbody>
</table>

For this measurement both the input of the converter and the test input have to be stimulated, such that the distortion contribute of each block can be measured. An FFT has to be performed but only the amplitude of the spectral component due to the test signal has to be evaluated as test quality parameter. In fact due to the NTF this component is very sensitive to the dynamic parameters of the circuit (poles and zeros) especially if a high order modulator is considered (see paragraph 2). In fig. 7 the FFT at the output of the converter is shown where a 16 kHz sine-wave is injected at the $SUM$ node (fig. 4) while a 4 kHz sine-wave is applied to the input (fig. 4). The same electrical configuration as in fig. 7 is shown in fig. 8, where to introduce non-linearity, a diode at the first integrator input is inserted to model the distortion. By comparing the 16 kHz spectral lines in both diagrams, an attenuation of 10 dB can be detected, when the distortion model is applied. This difference is amplified and filtered to make the distortion evaluation easier.

### 4. Conclusion

In this paper a potential solution to improve the testability of $\Sigma\Delta$ ADCs has been described using the quantizer input as test node. Both a theoretical description of the method and results from investigations using a high level simulator to study a 16 bit audio ADC are shown. From the analysis the method appears promising and fast, as it does not require sophisticated computations as in...
case of conventional techniques. The on purpose use of the test input makes it compatible with the test access features such as in the IEEE1149.4 where a separate input and test input have to be provided. Higher frequency applicability is currently under further investigation.

5. Acknowledgements

This work has been carried out under the framework of the European Commission IST project “TAMES-2” Testability of Analogue Macro-Cells Embedded in System-on-Chip, Contract no.: IST-2001-34283. The author would like to thank Eric Compagne, Dolphin Integration and Steve Sunter, Logic Vision, for their valuable feedback on the ideas presented in this work.

6. References


