Evening Panel Discussion

March 23, 2004
7:00pm

IP Industry: Nordstrom or K-Mart?
The Trend Toward Tighter Relationships Between Suppliers and Users

Description
IP users are forging tighter relationships with their IP suppliers. A number of factors have contributed to this trend, including the difficulty of acquiring and integrating IP from many sources as well as the importance of high quality, easy-to-use IP. Although the need to use pre-designed IP in SoC designs is growing, any quality problem with that IP will have a disproportionately large impact on SoC design and integration cost. IP quality is more than just functional correctness—it also includes, for example, completeness of the deliverables as well as ease of implementation and integration. IP must also address successfully the issues introduced by nanometer process technology (e.g., low power, signal integrity, timing closure). In this interactive session, a panel representing SoC integrators (users), IP providers and semiconductor vendors will explore the various aspects of the IP user/vendor relationship, including business and technical issues. They will discuss the impact of these issues as well as what’s being done to address them, including design, verification and integration methodologies.

Panelists Statements:

**Joachim Kunkel**, Vice President of Engineering, DesignWare, Synopsys
In today’s SoC designs, third party IP is a necessity, not a luxury. For many SoC designs, the processor, memory and key IP blocks are bought, not built. This third party IP is clearly critical to the success of the design project. Meeting the technical and schedule targets of the SoC design project is essential to enable hard-pressed chip companies to meet their business goals. In looking for an IP provider, SoC design teams look for one that can reduce the overall risk of the design project. An IP provider that not only provides the IP that it needs, but also has the resources, capabilities and commitment to deal with whatever problems arise in the course of the project. Each chip project is really just a series of crises - power is too high, area is too large, timing is too slow, critical bugs are found at the last moment. Having an IP partner rather than an IP vendor can make the difference when these crises strike. That is what SoC design teams are looking for.
Neal J. Carney, VP of Marketing, Artisan Components

The emergence of the IP industry as a distinct and independent segment of the semiconductor industry is evidence of the value that can be derived from the economies of scale of horizontal specialization of portions of the overall semiconductor supply chain. Just as foundries have succeeded by focusing on manufacturing and EDA companies have succeeded by focusing on design automation tools, IP providers can succeed by focusing on delivering pervasive IP to a broad set of IC designers. There are a number of factors however that influence whether any particular IP company will succeed in delivering on this value proposition.

The first of these factors has to do with economies of scale. The fundamental premise of horizontal specialization is delivering a lower cost solution to the industry while achieving an attractive ROI to the investment community. For IP this can only be achieved through extensive leverage and re-use of IP solutions across multiple designs, companies and market segments. Standardization, whether de-facto or through standards groups certainly enhances the prospects for re-use.

Equally important to the success of horizontal specialization is the attention to the interfaces to adjacent layers in the value chain. For IP this means a seamless interface to process technologies and manufacturers as well as tight integration into the user design environment in terms of design methodology, reference flows and the requisite EDA view support. Creative business models and partnering models are essential to creating these seamless interfaces and delivering the value customers expect when they outsource IP.

Peter Hirt, IP Program Manager, Central R&D Group, ST Microelectronics

Design teams are integrating 3rd party IP blocks of dramatically increasing number and complexity into their SoC designs. This has introduced technical as well as business challenges that drive the relationship of supplier and vendor closer and closer together. For the IP to be able to increase productivity while reducing risk, the IP supplier needs to offer: quality, breadth, stability, and a close partnership relationship.

Quality is much more than just functional quality (although that’s certainly critical). It also includes solid IP architecture for reuse. The IP should be more complete and easy-to-integrate, since assembling many IP blocks from different suppliers dramatically increases risk — this means IP providers need to supply complete subsystems, including hardware as well as supporting software (e.g., drivers). Verification IP needs to be included which supports post-integration, system-level testing as well as block-level testing. Quality IP must also have silicon proof/demo vehicles and independent certification, where possible, for interoperability and function (e.g., USB-IF, PCI SIG).

IP suppliers need to have a wide portfolio of IP, with appropriate expertise to support it. While helping to reduce technical integration risk, this also substantially reduces the number of complex business and legal interactions required to use IP. With pre-negotiated contracts, IP rights and pricing, we can make it much easier for our design community to use the IP and spend their time on value-added design.

Given the intense requirements on IP suppliers, it’s critical that we work with stable companies able to form tight business and technical relationships with us. On the business side, we seek good business value with flexible business models. As close partners, one of the key elements is transparent communication, especially with new IP still under development. This includes both good project and well as post-development communication, like release planning and access to information about all issues, with early warning when issues arise—since they definitely will.

IP reuse is a business of trust and partnership. This close relationship between IP supplier and vendor is mutually beneficial and will enable a growing IP market as well as successful, timely SoC design.
**Mamta Bansal**, Manager- Foundation IP, PMC-Sierra, Burnaby, Canada

There is an extensive amount of IP available from a large number of IP Suppliers. Success of a product is directly linked to IP quality. For a chip to be manufacturable, all IP must meet functional and performance requirements over process, voltage and temperature variations. IP must also be immune to reliability issues such as electromigration and signal integrity. Delivery of accurate timing and power views which work seamlessly in the DSM design flow is key to meeting schedules as well as post-tape-out success. It is a daunting task to evaluate and select an IP with no real quality standard among IP suppliers. One current initiative that has the potential to aid in setting a standard is the Quality IP (QIP) metric initiated by the VSIA, and now with joint efforts of the VSIA and FSA to achieve widespread industry adoption. From the IP User’s point of view, it will provide an objective way of comparing IP Provider’s practices and the resulting IP quality. From the IP Supplier’s point of view it will provide a way of proving to IP User’s the achieved level of quality, and therefore can be used as a marketing differentiator. QIP by itself is not enough, but it does have the potential of being a catalyst to drive changes in the way IP Supplier’s verify IP and prove to IP User’s that IP works as required.

**Tim Holden**, Strategic WW EDA Vendor Relations Manager, ARM Limited Cambridge UK

ARM is famous for its partnership which ARM users can draw upon to make their ARM design the finest possible. What is not spoken about so often is that ARM also works closely with its partners during the IP creation. As the IP is designed in advance of it being re-used, in complete SoC’s it is likely to be one of first designs in the world to be subjected to the demands of the latest silicon manufacturing processes and due to the diverse nature of the applications, and diverse silicon processes, the re-usable IP will be designed in to, it will experience more corner cases than the ‘used only once’ design parts. It has to be designed to be robust enough to cope with these extremes. Close relationships with early adopter customers, silicon foundries, EDA tool suppliers and ARM research and development has ensured that ARM supplies high quality, robust silicon IP that works in today’s advanced silicon processes and those of the future.

**Marlon R. Murzello**, Vice President, Consumer Custom Solutions Engineering, LSI Logic Corporation