Device Optimization for Ultra-Low Power Digital Sub-Threshold Operation

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ABSTRACT

Digital circuits operated in the sub-threshold region (supply voltage less than the transistor threshold voltage) can have orders of magnitude power advantage over standard CMOS circuits for applications requiring ultra-low power and medium frequency of operation. It is possible to implement sub-threshold logic circuits using the standard transistors that are designed primarily for ultra high performance super-threshold logic design. However, a Si MOSFET so optimized for performance in the super-threshold regime is not the best device to use in the sub-threshold domain. In this paper, we propose device designs apt for sub-threshold operation. Results show that the optimized device improves the delay and power delay product (PDP) of an inverter chain by 44% and 51%, respectively, over the normal super-threshold device operated in the sub-threshold region.

Categories and Subject Descriptors

1.1 [**Technologies and Digital Circuits**]: Emerging logic and memory technologies, Device design, Low power low leakage circuits, Memory circuits, Cooling technologies, Battery technologies

General Terms: Design

Keywords:

Device optimization, sub-threshold operation, ultra-low power applications.

1. INTRODUCTION

In recent years, the demand for power sensitive designs has grown significantly. This tremendous demand has mainly been due to the fast growth of battery-operated portable applications such as notebook and laptop computers, personal digital assistants, cellular phones and other portable communication devices. Further, due to the aggressive scaling of transistor sizes for high performance applications, not only sub-threshold leakage current increases exponentially, but also gate leakage and reverse biased source-substrate and drain-substrate junction band-to-band tunneling (BTBT) currents increase significantly [1-3]. The unwanted tunneling currents may severely limit the functionality of the devices. In the VLSI system design space, considerable attention has been given to the design of medium power, medium performance circuits (tens to hundreds of MHz clock rates). Well known methods include: voltage scaling [4], [5], switching activity reduction [6], [7], architectural techniques of pipelining and parallelism, and CAD issues of device sizing, interconnect [8], [9] and logic [10], [11] optimization. However, these methods are not sufficient in many applications such as portable computing gadgets, medical electronics, etc., where ultra-low power consumption with medium frequency of operation (tens to hundreds of MHz) is the primary requirement. To cope with this, design of digital sub-threshold logic was investigated with standard devices operated in the sub-threshold region (supply voltage less than the threshold voltage of the transistor) [12], [13]. Due to the exponential I-V characteristics of the transistor (schematic shown in Fig. 1a), sub-threshold logic gates provide near ideal voltage transfer characteristics (VTC). Furthermore, in the sub-threshold region, the transistor input capacitance is less than that of strong inversion operation. The transistor input capacitance, C_i in sub-threshold is a combination of intrinsic (oxide capacitance (C_{ox}) and depletion capacitance (C_d)) and parasitic (overlap capacitance (C_{do}), fringing capacitance (C_{if}, C_{of}), etc.,) capacitances of a transistor (Fig. 1b) and is given by [14]

$$C_i = series(C_{ox}, C_d) \parallel C_{if} \parallel C_{of} \parallel C_{do} \qquad (1)$$

In contrast, the input capacitance in strong inversion operation is dominated by the oxide capacitance. Due to the smaller capacitance and lower supply voltage (< threshold voltage of the transistor, V_{th}) digital sub-threshold circuits consume less power than their strong inversion counterpart at a particular frequency of operation. However, since the sub-threshold leakage current is used as the operating current in sub-threshold operation, these circuits cannot be operated at very high frequencies.

In previous work, standard transistors were operated in the sub-threshold region to implement sub-threshold logic. By standard transistors is meant the super-threshold transistors that are used for ultra high performance design. It is only prudent to investigate if these standard transistors are well suited for sub-threshold operation. In this paper, we show that for a particular technology generation, lower power and higher performance can be achieved in the sub-threshold region by redesigning the devices specifically for sub-threshold operation.

2. DOPING PROFILE CONSIDERATIONS

Scaled device technologies demand non uniform doping profiles to provide good control on the electrical characteristics of the device. It is an established fact that for scaled super-threshold transistors it is essential to have halo and retrograde doping to suppress the short channel effects [15]. The main functions of halo doping and retrograde wells are to reduce drain induced barrier lowering (DIBL), prevent body punch-through and control the

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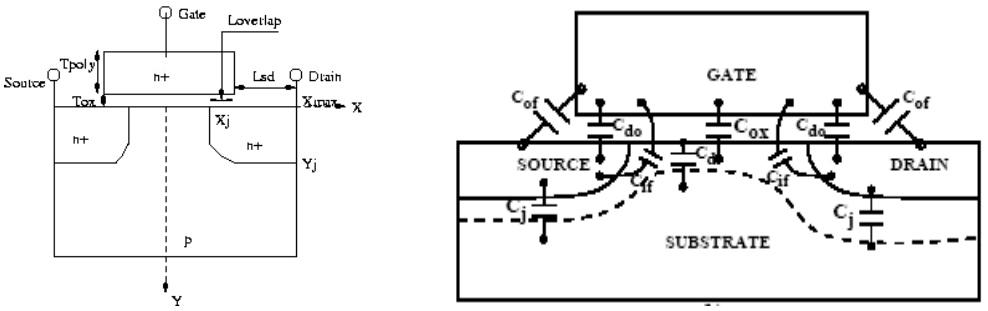

Fig. 1: a) Architecture of the device. (b) The schematic showing the different capacitance components.

threshold voltage of the device independent of its sub-threshold slope. However, in sub-threshold operation, it is worthwhile to note that the overall supply bias is small (in the order of 150mV~300mV). Consequently, the effects of DIBL and body punch-through are extremely low. Further, as long as we meet an I_{off} budget, the better the sub-threshold slope (S) leads to a better device. Since our interest is in the region below the threshold voltage, it is not of any interest to us, where the threshold voltage of the device actually is, as long as we meet a predefined I_{off} and S. Hence, it can be qualitatively argued that the halo and retrograde doping are not essential for sub-threshold device design. In the following sections we would quantitatively show the same.

The absence of the halo and retrograde doping has the following implications:

- *A simplified process technology in terms of process steps and cost.*
- *A significant reduction of the junction capacitances.* The halo regions near the source-substrate and the drain-substrate regions significantly increase the junction capacitances thereby increasing the switching power and the delay of the logic gates. The absence of the halo/ retrograde doping will reduce this junction capacitance.

It should however, be noted that the doping profile in these optimized devices should have a high-to-low profile. It is necessary to have a low doping level in the bulk of the device to:

- Reduce the capacitance of the bottom junction.
- Reduce substrate noise effects and parasitic latch-up problems.

However, the high to low profile does not require any special sputtering or ion-implant step (as is required for halo/retrograde doping) and hence, significantly reduces the process complexity and cost [18].

3. MODELING I_{SUB} AND CAPACITANCES FOR NON UNIFORM CHANNEL DOPING

This section represents the general approach used to formulate the model for the junction capacitance, the depletion capacitance and the subthreshold current of a MOSFET. The formulation, developed for NMOS transistors, can be easily extended to PMOS transistors. Device structures with Gaussian-shaped channel ("super halo" channel doping) and source/drain (S/D) doping profiles have been considered while deriving these models. A schematic of the device structure (symmetric about the middle of the channel) is shown in Fig. 1a. The 2-D Gaussian doping profile in the channel ($N_a(x,y)$) and S/D ($N_{sd}(x,y)$) can be represented as [16]:

$$x > 0,$$

$$N_a(x,y) = A_p \Gamma_{xa}(x) \mathrm{K}_{ya}(y) + N_{SUB}$$

$$\textbf{where, } \mathrm{K}_{ya}(\mathbf{y}) = exp\left(\frac{-(y-\alpha_a)^2}{\sigma 1_{ya}^{\,2}}\right);\ 0 \le y \le \alpha_a$$

$$= exp\left(\frac{-(y-\alpha_a)^2}{\sigma 2_{ya}^{\,2}}\right);\ y > \alpha_a \qquad (2)$$

$$\textbf{and} \quad \left[\begin{array}{ll} \Gamma_{xa}(x) = exp\left(\frac{-(x-\beta_a)^2}{\sigma_{xa}^{\,2}}\right); & 0 \le x \le \beta_a \\ = \mathbf{1}; & x > \beta_a \end{array}\right]$$

Similarly, the S/D doping ($N_{sd}(x,y)$) can be represented as:

$$x > 0,$$

$$N_{sd}(x,y) = A_{sd} \Gamma_{xsd}(x) \mathrm{K}_{ysd}(y)$$

$$\text{where, } \mathrm{K}_{ysd}(\mathrm{y}) = exp\left(\frac{-(y)^2}{\sigma_{ysd}^{\,2}}\right) \qquad (3)$$

$$\text{and} \quad \left[\begin{array}{ll} \Gamma_{xsd}(x) = exp\left(\frac{-(x-\beta_{sd})^2}{\sigma_{xsd}^{\,2}}\right); & 0 \le x \le \beta_{sd} \\ = 1; & x > \beta_{sd} \end{array}\right]$$

where, A_p and A_{sd} represent the peak "halo" and S/D doping respectively. N_{SUB} is the constant uniform doping in the bulk and is much less compared to contributions from Gaussian profiles at and near the channel and S/D regions. Parameters α_a, α_a α_{sd} (=0), β_a and β_{sd} control the positions and $\sigma 1_{ya}$, $\sigma 2_{ya}$, σ_{xa} and σ_{ysd}, σ_{xsd} control the variances of the Gaussian profiles in channel and S/D regions.

It should be noted here that in the body of the MOSFET, the peak doping is found near the source drain junctions and the doping falls off towards the surface as well as deep in the bulk of the device. This constitutes the halo and the retrograde doping profiles. Unless otherwise specified in this paper we have used NMOS (N_{ref}) and PMOS (P_{ref}) transistors with L_{eff}=50nm, W_{eff}=1μm and channel doping profile α_a=0.021μm, $\sigma 1_{ya}$=0.014μm $\sigma 2_{ya}$=0.014μm β_a=0.031μm, σ_{xa}=0.030μm and S/D profile from [15].

3.1 Modeling Subthreshold Current (Ids)

In the sub-threshold state of a device (Vgs < Vth) the current flowing from the drain to the source of a transistor is known as the

subthreshold current. The subthreshold current flowing through a transistor is given by [14],

$$I_{sub} = \frac{w_{eff}}{L_{eff}} \mu \sqrt{\frac{q\varepsilon_{si} N_{cheff}}{2\Phi_s}} v_T^2 exp\left(\frac{V_{gs} - V_{th}}{S v_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{v_T}\right)\right) \qquad (4)$$

where, N_{cheff} is the effective channel doping, Φ_s is the surface potential, S is the subthreshold swing and v_T is the thermal voltage given by kT/q. Using the charge sharing model and following the procedure given in, the threshold voltage can be expressed as :

$$V_{th} = V_{FB} + (\Phi_{s0} - \Delta\Phi_s) + \gamma\sqrt{\Phi_{s0} - V_{bs}}\left(1 - \lambda\frac{X_d}{L_{eff}}\right) + \Delta V_{NWE} \qquad (5)$$

where, V_{FB} is the flat-band voltage, Φ_{s0} zero bias surface potential, γ is the body factor, $Cox = \varepsilon_{sio2} / tox$ is the oxide capacitance, X_d is the depletion layer thickness, λ is a fitting parameter (~1) and ΔV_{NWE} is the narrow-width correction factor given in [17]. $\Delta\Phi_s$ is the reduction of the surface potential (Φ_s) of short channel devices from its zero bias value due to short channel effects like DIBL and V_{th} roll-off [14]. Different parameters in the above model depend on the effective channel and source/drain doping [14], [16], [17]. We have evaluated the effective channel (N_{cheff}) and source/drain doping (N_{sdeff}) considering the exact 2-D Gaussian doping profile (given in (2), (3)) as given below:

$$N_{sdeff} = \frac{1}{\Delta_{SD}} \iint_{\Delta_{SD}} N_{sd}(x,y)\,dxdy = \frac{A_{sd}}{\Delta_{SD}} \int_{x-X_j}^{x=L_{gate}/2+L_{sd}} \Gamma_{xsd}(x)\,dx \int_{y=0}^{y=Y_j} K_{ysd}(y)\,dy$$

$$N_{cheff} = \frac{1}{\Delta_{ch}} \iint_{\Delta_{ch}} N_a(x,y)\,dxdy + N_{sub} = \frac{A_p}{\Delta_{ch}} \int_{x=-L_{eff}/2}^{x=+L_{eff}/2} \Gamma_{xa}(x)dx \int_{y=0}^{y=X_d} K_{ya}(y)dy + N_{sub} \qquad (6)$$

where, $\Delta_{SD}=(L_{overlap}+L_{sd})Y_j$ is S/D area, $L_{overlap}$ is the gate and the S/D overlap length and L_{sd} is the S/D length as shown in Fig. 1a. $\Delta_{ch}=L_{eff}X_d$ is the area of the channel region which is under the influence of gate. To calculate the effective doping X_d is assumed to be α_a since most of the depletion charge is confined in the region $y = 0$ to $y = \alpha_a$. Since we have considered the exact Gaussian nature of the doping profile (instead of approximating it as step profile as described in [17]), we have been able to capture the effect of change in the doping profile more accurately.

The subthreshold slope (S) for the short channel device, considering the penetration of the drain induced electric fields in the centre of the channel is given by:

$$S \approx 2.3\frac{mkT}{q}\left(1 + \frac{11t_{ox}}{X_d} e^{-\pi L/(X_d + 3t_{ox})}\right) \qquad (7a)$$

where the body effect coefficient, m is given by:

$$m = 1 + \frac{3t_{ox}}{X_d} \qquad (7b)$$

Fig. 2 shows the variation of I_{off} with the peak of the halo doping, A_p. Device simulations have been carried out with the device simulator MEDICI and the results have been compared. An important aspect here is that we have not changed the location of the peak of the halo or the variances of the Gaussian profiles. Only the effect of the peak of the halo doping (and consequently the effective doping in the entire channel) has been studied. It can be noted that as the peak of the halo doping decreases, I_{off} increases as expected. The standard device presented in [15] has $A_p = 2 \times 10^{19}\ cm^{-3}$. The work function of the standard device has been adjusted so that it gives an I_{off} of 1nA. In all our simulations the same gate work-function has been used.

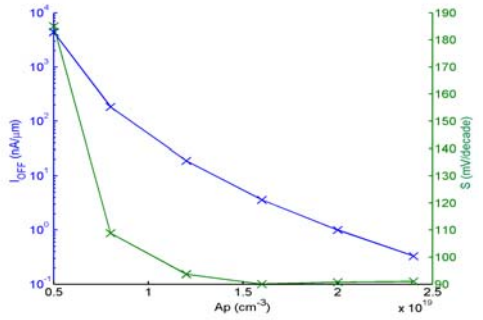

Fig 2: The variation of I_{OFF} and S with the peak of the halo doping, A_P. Solid line shows results from our model and markers show MEDICI simulations.

Fig 2 also shows how S varies with the peak of the halo doping. It can be noted that as the doping concentration falls, the short channel effects start dominating and the subthreshold slope increases fast.

3.2 Modeling Junction Capacitance (C_J)

For a symmetric device the capacitance expressions for the drain and the source junctions will be identical. Hence, here we have considered only the drain junction. The junction capacitance is given by:

$$C_J = \frac{w_{eff}\, l\, \varepsilon_{si}}{W_{dj}} = w_{eff}\, l \sqrt{\frac{\varepsilon_{si} q}{2(\psi_{bi} + V_j)}\left(\frac{N_a N_d}{N_a + N_d}\right)} \qquad (8)$$

where N_a and N_d are the doping concentrations on the two sides of the junction, ψ_{bi} is the built-in potential across the junction and V_j is the potential applied across the junction. The length l is the length of the junction and w_{eff} is the effective width of the NMOS. The expression for capacitance cannot be analytically computed because the width of the junction varies along the length l. To obtain an accurate analytical estimate of the total junction capacitance, we can apply the "rectangular junction" approximation (Fig. 3). Using this approximation the total capacitance at the drain junction is given by:

$$C_{J-drain} = C_{side} + C_{bottom}$$
$$w_{eff}(x_2 - x_1)\sqrt{\frac{\varepsilon_{si} q}{2(\psi_{bi} + V_j)}\left(\frac{N_{aside} N_{dside}}{N_{aside} + N_{dside}}\right)}$$
$$+ w_{eff}(y_2 - y_1)\sqrt{\frac{\varepsilon_{si} q}{2(\psi_{bi} + V_j)}\left(\frac{N_{abottom} N_{dbottom}}{N_{abottom} + N_{dbottom}}\right)} \qquad (9)$$

Where, N_{aside} and N_{dside} are given by:

$$N_{aside} = \frac{1}{|y_2 - y_1|}\int_{y_1}^{y_2} N_a(X_j, y)dy$$
$$N_{dside} = \frac{1}{|y_2 - y_1|}\int_{y_1}^{y_2} [N_{sd}(x = \beta_{sd}, y) - N_a(x = \beta_a, y)]dy \qquad (10)$$

ψ_{biside} (the built-in potential for a step junction) is given by :

$$\psi_{biside} = \frac{kT}{q} ln\left(\frac{N_{aside} N_{dside}}{n_i^2}\right) \qquad (11)$$

X_j and Y_j are found by solving following equations:

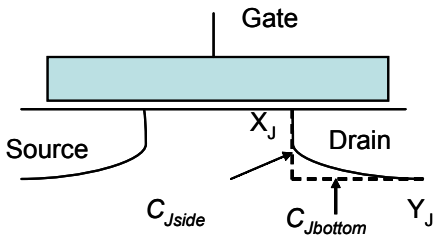

Fig 3. The 'rectangular junction' approximation.

$$N_{sd}(X_j, y=0) = N_a(X_j, y=0)$$
$$N_{sd}(x=x_{\max}, Y_j) = N_a(x_{\max}, Y_j) \quad (12)$$

For simplicity y_1=0 and $y_2 = Y_j$. For bottom junction x_1=X_j and $x_2 = x_{max}$..

The doping profile has a distinctive effect on the total junction capacitance of the device. As the doping concentration increases, the junction width decreases and hence the capacitance increases. Fig. 4 illustrates, for the same variance in the Gaussian profile, how the peak of the doping changes the net junction capacitance.

3.3 Modeling Other Parasitic Capacitances and the Intrinsic Gate Capacitance

Having derived an analytical model for the junction capacitance, the next logical step would be to model the other capacitances in the device. The direct overlap capacitance component is obtained as:

$$C_{do} = \frac{\varepsilon_{ox} w_{eff} (L_{gate} - X_J)}{t_{ox}} \quad (13)$$

Solving Laplace's equation analytically with proper boundary conditions the outer and inner fringe components can be expressed as:

$$C_{of} = \frac{2\varepsilon_{ox} w_{eff}}{\pi} \ln\left(1 + \frac{t_{gate}}{t_{ox}}\right) \quad (14a)$$

$$C_{do} = \frac{2\varepsilon_{si} w_{eff}}{\pi} \ln\left(1 + \frac{X_J}{2t_{ox}}\right) \quad (14b)$$

where the gate height t_{gate} has been chosen 60nm [15]. It should be noted that out of the three major overlap capacitance components, the direct overlap component is the major contributing factor.

Apart from the extrinsic parasitic capacitances described above, the intrinsic device capacitance also plays a pivotal role to determine:

- The total input capacitance (vide equation (1))
- The MOSFET body effect coefficient, m (vide equation(7b))

This intrinsic device capacitance is given by the parallel combination of the oxide capacitance, C_{ox} and the device capacitance, C_d

$$C_d = \frac{\varepsilon_{si} w_{eff} L_{eff}}{X_d} \quad (15)$$

It has been mentioned in reference to the Gaussian doping profiles that the peak of the doping occurs at a certain depth α_a in the device. Since the variances of the Gaussian profile in the y direction, $\sigma 1_{ya}$, $\sigma 2_{ya}$ are smaller than the location of the peak, α_a the depletion region extends till the peak of the halo irrespective of the value of the doping, A_P. This is one of the major features of the halo and retrograde dopings.

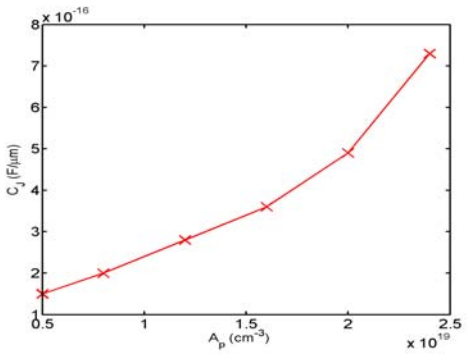

Fig 4: The variation of the junction capacitance, C_J with the peak of the halo, A_P. Solid line shows results from our model and markers show MEDICI simulations

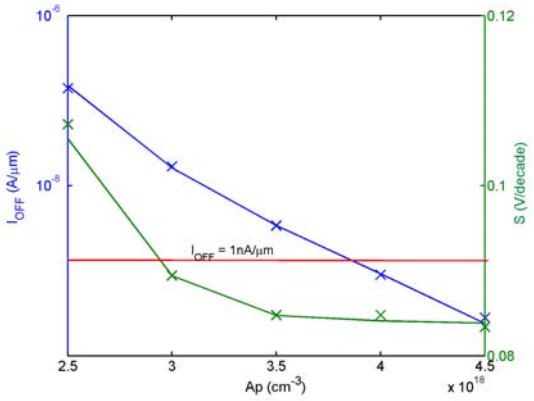

Fig 5: I_{OFF} and S for the high to low doping profile for varying A_P. Solid line shows results from our model and markers show MEDICI simulations.

Consequently, in devices with a deep retrograde well, the junction depth, X_d and hence the device capacitance C_d remains almost insensitive to the value of the peak doping A_p and depends only on α_a. The intrinsic device capacitance remains invariant with A_p (~1fF/μm). Note further that in the subthreshold regime the depletion capacitance reduces the intrinsic gate capacitance from its super-threshold value of C_{ox} and the junction capacitance is comparable to C_{ox}. Hence, both are equally important in determining the overall switching capacitance.

From the modeling and analysis of super halo devices, we may note the following:

- In subthreshold region of operation, both the intrinsic device capacitance as well as the parasitics (mainly junction capacitance) is of equal importance.
- Junction capacitance can be reduced by reducing the peak of the halo doping but that increases I_{OFF}.
- S can be decreased by decreasing the body effect coefficient, m. This requires an increase in X_d and this in-turn increases I_{OFF}.

Hence an optimal subthreshold device would reduce C_J as well as S without increasing I_{OFF}. We have already argued qualitatively in section (2) that deep implants like halo and retrograde would not be essential for low voltage subthreshold operation and that a high to low doping profile should be usable to design subthreshold devices. In the following section let us focus on a high to low doping profile of the devices. The 2-D Gaussian doping profile can be easily modified to give a high to low doping profile by

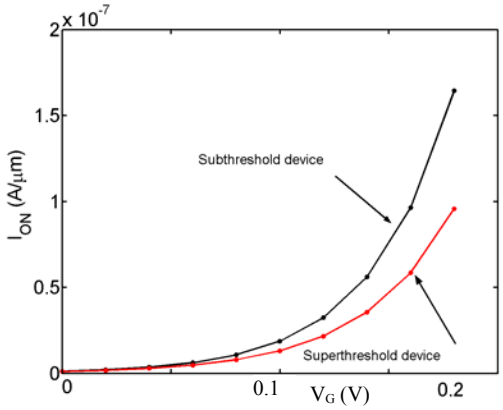

Fig 6: I_D-V_G for the super-threshold and the sub-threshold device for *iso*-I_{OFF} (1nA/μm).

setting α_a=0.021μm, $\sigma 1_{ya}$=∞ $\sigma 2_{ya}$=0.014μm σ_{xa}=∞. This ensures that the channel doping has no variation in the x-direction while in the y-direction it is constant at a value A_p till α_a and thereafter falls off exponentially with a variance $\sigma 2_{ya}$.

4. DEVICE DESIGN WITH HIGH TO LOW DOPING PROFILES

It has been noted that by decreasing the peak halo doping, the junction capacitance can be reduced. This would increase the I_{OFF} and for very low values of the doping concentration the subthreshold slope too will be affected. The increase in I_{OFF} and S can be compensated for by increasing $\sigma 1_{ya}$ and for the simplified process technology it will be useful if the high to low doping profile ($\sigma 1_{ya}$=∞) can be used. Fig. 5 shows how the off current and subthreshold slope varies with A_p for such a doping profile. A doping concentration of A_p=3.8×10^{18} cm^{-3} gives an off current of 1nA. Further the subthreshold slope of this device (~83mV/decade) is better than the standard super-threshold device(~90mV/decade). Fig. 6 shows that the optimized sub-threshold device has a higher on-current for *iso*-I_{OFF} compared to the super-threshold device.

Another important aspect for the sub-threshold device is the junction capacitance. The junction capacitance of the optimized device is lower than the super-threshold device because the lower over-all junction doping. In comparison to C_J=4.9×10^{-16}F/μm for the super-threshold device, for the subthreshold device the

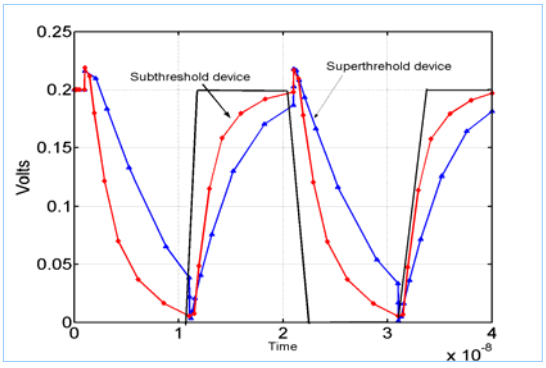

Fig 7: The transient response of an inverter with i) super-threshold and ii) sub-threshold devices.

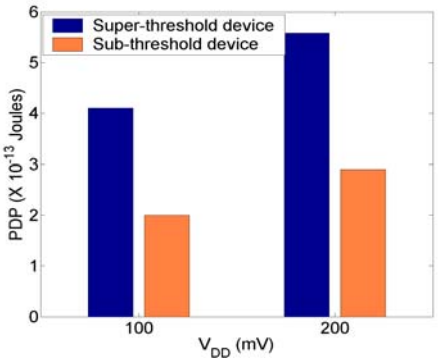

Fig 8: Variation of PDP with the V_{DD} for the super-threshold and the optimized sub-threshold device both operated in sub-threshold region.

junction capacitance (by analytical model, section 3.2 and also verified by device simulator MEDICI) is C_J=3.2×10^{-16} F/μm. Hence the junction capacitance decreases by approximately 35%. The intrinsic device capacitance remains unaffected because the depletion region extends till α_a which has not been changed here. Thus the optimized subthreshold device has a better sub-threshold slope, S and a lower junction capacitance at *iso*-I_{OFF} conditions.

5. CIRCUIT SIMULATIONS

The optimized sub-threshold device gives a better I-V characteristics and a lower junction capacitance. To verify its impact on circuit level performance, we simulated an inverter driving a similar inverter. Fig. 7 shows the transient simulations of the inverter with the standard super-threshold device and also the sub-threshold device. It can be noted that the proposed sub-threshold device has smaller delay owing to its higher on-current and reduced junction capacitance. Simulations show that the delay decreases by *44%* (from 3.4ns in case of the super-threshold device operated in sub-threshold to 1.9ns for the optimized sub-threshold device). This indeed shows that the speed of operation of the digital sub-threshold circuit can be increased by proper device design so that it operates at a few Mega Hertz. Further, the reduced junction capacitance results in reduced dynamic (or switching) power. Fig. 8 shows how the power delay product (PDP) of the inverter circuits built with i) standard devices and ii) sub-threshold devices compare for two different valued of V_{DD} (the devices are in subthreshold for both the V_{DD} values). It can be noted that the optimized subthreshold devices provide *51%* improvement in PDP.

6. OPTIMIZED SUBTHRESHOLD DEVICES IN SUPER-THRESHOLD OPERATION

We have shown that by proper designing of the NMOS for subthreshold operation, both delay and power can be reduced. We have argued qualitatively in section 2 that highly doped halo/retrograde implants would not be necessary for such low voltage devices. It will be worthwhile to investigate if the proposed devices can be used for super-threshold mode of operation. One of the major reasons for using heavily doped halo implants is to restrict the sub-surface flow of current and effects of punch-through. Punch-through occurs when the source and the drain depletion regions merge and there is a flow of drift current

under the high electric field in the depletion region. Increased halo doping restricts the widening of depletion width and hence prevents the source and drain junctions from merging together. Let us consider our optimized sub-threshold device and let us apply an increasing V_{GS} to it. Fig. 9 illustrates the sum of the source and the drain depletion widths (W_{source} and W_{drain}) as a function of V_{DS}. The effective channel length L_{eff} is shown distinctively. It can be noted that at a V_{DS} of around 0.8V, the depletion widths merge ($W_{source} + W_{drain} = L_{eff}$) and the gate loses control on the channel. This is an occurrence of breakdown and the device can no longer be used. A constant subsurface current starts and even for zero V_{GS} this current flows continuously. This proves conclusively that the sub-threshold device cannot be used for super-threshold operations and for high performance design (involving high V_{DD}) it is essential to have halo/retrograde implants.

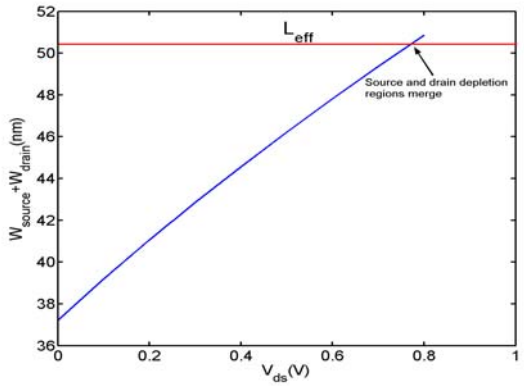

Fig 9: Merging of the source and the drain depletion regions when the sub-threshold device is operated in super-threshold region.

7. CONCLUSIONS

In this paper we propose an optimized transistor structure for digital sub-threshold operation. Although our simulations have been carried out for a 50nm effective-length technology, the underlying idea of the work is applicable to any scaled technology. We also showed that digital sub-threshold circuits can be optimized to operate at higher frequencies than what the standard super-threshold transistors do provide. The optimized sub-threshold devices show more than 50% improvement in power-delay-product. Another important contribution of this work is that we have demonstrated that a simpler doping profile for the channel is adequate for sub-threshold devices. Due to the low operating voltage, the halo/retrograde channel doping can be removed and a simple high to low doping profile is adequate for sub-threshold operations. Our study shows that such a doping profile has lower peak doping concentration, thereby reducing junction capacitance. This in turn improves the circuit delay and power dissipation. It is therefore, necessary to design optimum device structure for subthreshold operation in order to achieve minimum possible power consumption in the circuit at a particular frequency of operation.

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