ABSTRACT
Universal Mobile Telecommunication System (UMTS) front end design is challenging because of the need to optimize power while satisfying a very high dynamic range requirement. Dealing with this design problem at the transistor level does not allow to explore efficiently the design space, while using behavioral models does not allow to take into consideration important second-order effects. We present an extension of the platform-based design methodology originally developed for digital systems to the analog domain to conjugate the need of higher levels of abstraction to deal with complexity as well as the one of capturing enough of the actual circuit-level characteristics to deal with second order effects. We show how this methodology applied to the UMTS front-end design yields power savings as large as 47% versus an original hand optimized design.

1. INTRODUCTION
The design of analog and RF systems is largely dominated by heuristics and trial-and-error approaches. This situation is mostly due to the number of second order effects, non orthogonality between design parameters and complex device physics that have made the problem analytically intractable. These difficulties force designers to work at the circuit level using circuit simulation as the work horse to assess whether the design satisfies the constraints and has satisfactory performance. Since simulation is in general slow for these circuits, only a few alternative designs are generated and compared. If optimization is used at all it is used at the parametric level and not at the architectural level, leaving a large portion of the design space unexplored.

Platform-based design as presented in [1] has emerged as a novel paradigm to allow designing at higher level of abstraction while considering lower level physical properties. Summarizing the basic principles of the methodology, a platform can be considered as a library of components together with (i) a set of rules that describes legal ways of connecting these components and (ii) models that express their behavior and performance measures in terms of physical quantities such as time, power and area. The design process at the level of abstraction of the library consists of selecting a legal composition of the library elements (platform instance) that satisfies the performance requirements and optimizes a chosen quantity. Once the platform instance is selected, the designer moves to a lower level of abstraction where each of the elements of the selected instance is now a specification and has to be implemented with another lower level platform instance. The process terminates when the components of the design are all available in their physical form. The quality of the design depends critically on the choice of the elements of the libraries and on the quality of the performance models. The larger is the number of components, the larger is the design space and hence the better the final design is if the design space can be explored efficiently. On the other hand, if the number of component is small, design space exploration is fast and can be optimized but we may miss some interesting solution. The trade-off between the number of elements and the complexity of the exploration is at the heart of the methodology. In addition, the quality of the performance models determines whether the choice of the platform instance is sound. If the models are too inaccurate there is little confidence that the selected platform satisfies the constraints let alone optimality. This methodology is a meet-in-the-middle approach: the bottom-up phase corresponds to building the behavioral and performance models of the library elements as well as the characterization of the composition rules; the top-down phase corresponds to the selection process for the platform instance and to the propagation of constraints to the lower level abstractions.

This methodology can be applied to many design problems including the analog domain [2]. However, the challenges posed by the construction of analog performance models appears to make its application problematic. In this paper, we present a concrete example that demonstrates the effectiveness of Analog Platforms in system level analog design performing design space exploration and architecture selection for a state-of-the-art Universal Mobile Telecommunication System (UMTS) fully integrated direct conversion receiver front-end. UMTS provides several challenges to RF designers, mainly due to continuous transmission and reception; nonetheless, a direct conversion architecture is a viable solutions due to the channel bandwidth that makes $\frac{1}{2}$ noise and DC offsets less important. This design case leverages the topologies presented in [3] to build suitable platform elements for the receiver front-end. The performance to optimize in this paper is power.

This paper is organized as follows: Sec. 2 introduces
Analog Platforms, describing their features and abstraction properties and focusing on how architectural constraints are propagated at the behavioral level. Sec. 3 introduces the UMTS receiver architecture used in the case study. In Sec. 4, the bottom-up platform generation phase is accurately described. Sec. 5 deals with the top-down design phase, introducing high level system constraints and deriving behavioral model accuracy requirements based on sensitivity analysis. Design exploration is then performed through optimization and finally, in Sec. 6, some conclusions are drawn.

2. ANALOG PLATFORMS

High level behavioral models have been proposed for several classes of circuits and with different accuracy/complexity tradeoffs. Traditionally, behavioral models are used in two complementary ways: during the early design stages, simple models are introduced to test the overall system functionality and estimate sensitivities with respect to some performance figures (usually measuring non-ideal effects). Then, actual design proceeds partitioning system specifications on the analog subsystem based on past design experience and with some hints provided by (functional) high-level simulations. In the complementary approach, behavioral models are used to verify the overall system functionality once the detailed design has been completed. In this case, the models provide in general better accuracy since they do have as reference a fully completed design. Powerful techniques in this class are model order reduction [4], [5].

Analog Platforms (APs) have been introduced to provide a new abstraction level for system level analog designers. An AP approach allows annotating (functional) behavioral models with performances obtained through platform characterization and interconnection models. APs consist of design components with behavioral models \( \mu(\text{in}, \text{out}, \zeta) \), interconnections with their models \( \iota(\text{in}, \text{out}, \zeta) \) and performance models for both \( \mathcal{P}(\zeta) \). Design flow based on APs consists on two phases, bottom-up platform characterization and top-down design exploration. Platform characterization consists of selecting one or more circuit topologies described by their circuit configurations (e.g. transistor sizings and/or bias) with parameter vectors \( \kappa \) (lying in a configuration space \( \mathcal{I} \)) and circuit performances with vectors \( \zeta \) (lying in a performance space \( \mathcal{O} \)). At the behavioral level, \( \zeta \) is a vector of parameters controlling non idealties and second order effects of behavioral models, such as gain, bandwidth, and noise. A performance model, then, is a relation \( \mathcal{P} \) on \( \zeta \) such that \( \mathcal{P}(\zeta) = 1 \) iff \( \zeta \) is achievable with some vector \( \kappa \) and the current circuit topology and technology. In [6] an approximation scheme for \( \mathcal{P} \) based on Support Vector Machine (SVM) classifiers is presented based on statistical sampling of configuration vectors \( \kappa \). However, the number of samples required to achieve good accuracy levels increases exponentially with the dimensionality of \( \kappa \). Therefore, a set of conservative constraints is enforced on \( \kappa \) through Analog Constraint Graphs (ACGs) [7], capturing simple circuit constraints necessary for correct circuit operation (e.g. MOS in saturation, input matching and so on). ACGs drastically reduce the effective number of simulations required to get performance models, so that few thousand simulations are sufficient for platform generation.

The top-down phase consists of selecting a platform instance evaluating system performances at behavioral level and of performing optimizations to explore the design space. Optimizations are intrinsically constrained by performance models to contemplate only feasible solutions for each block in the system, so that, independently of system level constraints and cost functions, the choices resulting from the optimization process are achievable with some circuit configuration. The abstraction process involved in platforms allows running optimizations over several possible circuit topologies for each system component at once, thus effectively performing topology (architecture) selection as part of the optimization process.

Composability of behavioral models to allow hierarchical design flows is an essential part of the methodology. APs provide a set of interconnection models \( \iota(\text{in}, \text{out}, \zeta) \) to allow composition. In fact, analog circuit composition may significantly alter single circuit behavior, while behavioral model composition is a pure mathematical operation with no intrinsic side effects. Unfortunately, no general guidelines are available for interface model generation. A correct-by-construction (even though potentially inefficient) modeling guideline consists of identifying a set of factors \( \lambda = [\lambda_S, \lambda_L] \) that characterize the interface (both the source and load sides) and of using them to derive composability rules. In the linear case, \( \lambda \) may be the vector of source and load impedances. \( \lambda \) is then appended to the performance vector \( \zeta \), so that the loading effect of \( B \) on \( A \) in \( A \rightarrow B \) can be accounted for. In fact, performances for \( A \) are simulated considering an equivalent load \( B_{eq}^A(\lambda_S^A, \lambda_L^A) \), while performances for \( B \) are simulated with an equivalent source \( A_{eq}^B(\lambda_S^B, \lambda_L^B) \). Then, \( \lambda^A = \lambda^B \) is imposed as a composition rule.

![Figure 1: Direct conversion UMTS receiver architecture. The shaded area indicates the blocks considered in the case study.](image1)

![Figure 2: Interface parameter \( \lambda \) during composition A-B and characterization of A and B.](image2)
Input Signals
---

\( f_1 = 2.101 \text{ GHz, } -30 \text{ dBm} \)
\( f_2 = 1.965 \text{ GHz, } -33 \text{ dBm} \)
\( f_2 = 1.964 \text{ GHz, } -33 \text{ dBm} \)
\( f_2 = 2.0325 \text{ GHz, } -40 \text{ dBm} \)
\( f_2 = 1.964 \text{ GHz, } -30 \text{ dBm} \)

<table>
<thead>
<tr>
<th>Performance</th>
<th>Input Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>( f_1 = 2.101 \text{ GHz, } -30 \text{ dBm} )</td>
</tr>
<tr>
<td>IM2</td>
<td>( f_1 = 1.965 \text{ GHz, } -33 \text{ dBm} )</td>
</tr>
<tr>
<td>IM3</td>
<td>( f_2 = 1.964 \text{ GHz, } -33 \text{ dBm} )</td>
</tr>
</tbody>
</table>

Table 1: UMTS tests used for receiver performances.

(Fig. 2). Since \( \lambda \) is part of the performance vectors \( \zeta_A \) and \( \zeta_B \), the composition rule imposes that performances for \( A \) and \( B \) be compatible with the interface loading and, consequently they can be used to constrain behavioral models. On a case by case basis, however, more specific rules may be adopted for improving characterization efficiency and allow more flexible composition rules.

3. CASE STUDY: UMTS FRONT END

The design of an UMTS front end is a very challenging case study. With minimum power consumption as a driving principle, optimal receiver performances are far from trivial. Just as an example of the tradeoffs involved, direct conversion architectures require excellent second order linearity performances, which are difficult to achieve in fully integrated solutions without the help of external high Q filters. This sets a very high dynamic range requirement on the front-end. The difficulty of the problem has made UMTS front-end design an ideal case study to show the effectiveness of the platform-based design method in exploring analog design spaces, even on systems, such as RF, that are intrinsically difficult to deal with at system level.

The UMTS receiver front end architecture is the one originally presented in [3] and reported in Fig. 1. The transmission (TX) section is not implemented but it is considered since it is the main source of interference for UMTS devices. The Local Oscillator (LO), even though implemented in the original design, has not been modeled in this paper. System level design decisions for receivers involve gain, noise and non-linearity (among the others) partitioning along the receiver chain so that optimum performances are achieved at minimum cost (e.g. power consumption). Optimal partitioning is plainly impossible if we resort to circuit simulation as the only support. Indeed, designer currently partition the system according to experience and intuition, hardly a rigorous approach to optimality and feasible only if designers are really experienced.

4. THE BOTTOM-UP PHASE

The receiver architectural space consists of two different inductively degenerated LNA topologies, reported in Figs. 3 and 4, and a direct conversion mixer reported in Fig. 6. The selected topologies, together with properly defined configuration spaces \( \mathcal{I} \) are the elements of the top level platform and determine the exploration space. We will refer to the receiver behavioral model reported in Fig. 5. The LNA is modeled as a transconductor, \( \mu_{LNA} : V \times \zeta_{LNA} \rightarrow I \). An interface model is inserted to couple the LNA to the mixer behavioral model with an overall transimpedance behavioral model, \( \zeta : I \times \lambda \rightarrow V \). Finally, the mixer model down-converts the signal to baseband \( \mu_{MIX} : V \times \zeta_{MIX} \rightarrow V \). Platform characterization has been performed using the Spectre RF simulator to evaluate performances and a client/server framework [8] capable of generating circuit configurations \( \kappa \) according to ACGs and extracting performances from simulations. Tab. 3 reports details on performance model generation.

4.1 Low Noise Amplifier

We considered two different LNA topologies, the original inductively degenerated nMOS amplifier reported in [3], and a current reuse pMOS amplifier described in [9]. The npMOS amplifier allows obtaining higher gain and linearity values for a given current consumption. However, it requires a larger die area due to the larger number of inductors, and is more complex to design due to the larger number of degrees of freedom. Based on the analysis of [10] and [9]. Analog Constraint Graphs were developed to generate random circuit configurations according to minimum Noise Figure design criteria, input matching and general circuit bias constraints, thus reducing the exploration search space \( \mathcal{I}_{def} \subseteq \mathcal{I} \) by several orders of magnitude (Tab. 3). Both LNA topologies adopt a common behavioral model, so that they can be merged in terms of performance models \( P_{LNA} = P_N \cup P_{NF} \) and their performances compared during the optimization phase. Platform characterization has been based on the evaluation setup reported in Tab. 2.

The complexity of the model depends on the required accuracy in the frequency domain, which spans \( 1.96 \rightarrow 2.32 \)
The interface loading effects can be separated in our knowledge, no previous behavioral modeling effort dealt quantitatively with the problem of behavioral models tail the interface LNA-mixer and showing how more flexible rules can be obtained on a case-by-case basis. To the best of our knowledge, we introduce an ad-hoc extension to the general formalism. This allows all intermodulation products to be considered when characterizing the mixer. This has also the pos-

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_{LNA}$, $Q$, $f_0$</td>
<td>AC $1GHz \rightarrow 3GHz$</td>
</tr>
<tr>
<td>$NF$</td>
<td>noise $1.5GHz \rightarrow 2.5GHz$</td>
</tr>
<tr>
<td>$IM3$</td>
<td>PSS $@f_1 = 2.03GHz$, $V_{in1} = -40dBm$; PAC $@f_2 = 1.961GHz$, $V_{in2} = -30dBm$</td>
</tr>
</tbody>
</table>

Table 2: LNA performance evaluation setup.

GHz, determined by both linear and non-linear in-band receiver requirements. Since inductively degenerated topologies exhibit frequency responses far from being flat on such a spectrum, the overall model consists of an input filter and a non-linear transconductor. The input filter is a second order band-pass filter parameterized by quality factor, central frequency and maximum value. The transconductor is a third order polynomial model introducing linear gain and $3^{rd}$ order intermodulation distortion. The LNA Noise Figure ($NF$) is introduced through the following expression:

$$N_{LNA} = 4KTR_s \cdot |g_m \cdot Z_L|^2 \cdot 2.101GHz \cdot F_L$$

where $R_s = 50\Omega$, $T = 300K$, $g_m$ is the transconductor gain and $Z_L$ the output impedance. In order to get conservative performance estimates, $F_L$ is the average LNA noise Factor in the whole $2.11 \rightarrow 2.17 GHz$ bandwidth.

The performance model $P$ is a relation in a 12-dimensional space that is impossible to render graphically. A hint on the Power-NF projection can be obtained from the optimization trace in Fig. 8. The automatic characterization process generated LNA configurations that achieved 2.8 dB minimum NF in the nMOS case and 2.1 dB in the pMOS (given a 50 $\Omega$ impedance match). The maximum gain is 25 dB for the nMOS topology and 27 dB for the pMOS. The performance Area was estimated in both LNA and mixer cases by exploiting a Matlab script. For this purpose, die occupation of MOS transistors was approximated with $WL$ product, capacitors and resistors were considered as square and, finally, simple spiral inductors were assumed.

4.2 LNA-mixer interface

Stand-alone behavioral models achieve excellent accuracy in capturing inter-dependencies of different performance figures through performance models. However, this does not automatically translate into accurate receiver models, unless interconnection effects are introduced. In this subsection, we introduce an ad-hoc extension to the general composition rule introduces in Sec. 2 analyzing with some detail the interface LNA-mixer and showing how more flexible rules can be obtained on a case-by-case basis. To the best of our knowledge, no previous behavioral modeling effort dealt quantitatively with the problem of behavioral models interface. The interface loading effects can be separated in linear and non-linear contributions. Considering the linear part, CMOS active mixers may be accurately represented by parallel connection of a capacitor and a resistor (resulting by the Miller equivalent of the gate drain-overlap capacitance) dependent on mixer geometry. Therefore, when different mixers are connected to the same LNA, maximum gain and output tuning frequency are altered, thus varying LNA voltage gain. However, since the LNA is cascoded, the output current is less sensitive to load variations than the output voltage (as confirmed by both simulations and analytical computation). Interface effects are more pronounced as far as distortion is concerned. When large signals drive the mixer topology reported in Fig. 6, the gate-source capacitances of the transconductor get modulated by the signal, which translates into interface-generated intermodulation distortion (Fig. 7 shows the intermodulation increase when an LNA drives a mixer or an equivalent linear load).

We addressed both problems adopting a transconductor as the LNA model, therefore characterizing the LNA-mixer interface in current rather than voltage. For the linear behavior, this allows more accurate gain predictions as a function of mixer load. The LNA voltage output is then computed inserting an equivalent RLC impedance $Z_L$, as reported in Fig. 5. $Z_L$ is changed during the characterization process as part of configurations $\kappa$ so that its effects can be included in performances $\zeta$. Interface distortion has been addressed attributing it entirely to the mixer. This is achieved characterizing mixer performances using a current source to inject tones into the mixer. In fact, current sources do not shunt the capacitance modulation effects as voltage source would do, thus allowing all intermodulation products to be consid-

Figure 5: Behavioral model of the receiver.

Figure 6: Mixer schematic.
The interconnection model \( \{ in, out, \lambda \} \) is then the output resonant tank. Overall, model composition is achieved in the following way: \( \lambda_{LNA} = \{ C_{L}^{Mix}, L, Q \} \) (\( L \) is the inductance in \( Z_L \), \( Q \) is the quality factor of \( Z_L \) and \( C_{L}^{Mix} \) the capacitance in \( Z_L \) coming from the mixer) characterizes the interface used during LNA characterization (the quality factor \( Q \) and the mixer input capacitance \( C_{L}^{Mix} \) are obtained through simulations). \( \lambda_{Mix} = C_{Mix}^{L} \) is the actual mixer input capacitance. Then, an output load \( Z_L \) is inserted to convert LNA transistor current into a voltage. \( Z_L \) presents inductance \( L \) and \( Q \) as in \( \lambda_{LNA} \). A strict composition rule then requires that the mixer actually presents \( C_{Mix}^{L} = C_{Mix}^{L} \) at its input, so that performances can be accurately estimated. However, due to the weak dependency of linear response on \( C_{Mix}^{L} \) (remember that non-linear effects are embedded in the mixer), a looser composition rule may be derived that allows for a non-negative \( C_L \) in parallel with \( C_{Mix}^{L} \) to resonate with \( L \) at \( f_0 = 2.1 \) GHz. Therefore, the composition rule can be formulated as:

\[
\lambda_{LNA} = \{ C_{Mix}^{L}, L, Q \} \\
\lambda_{Mix} = C_{Mix}^{L} \\
\lambda_{LNA}(1) \geq \lambda_{Mix}
\]

We should finally note that, as far as distortion in concerned, the mixer output provides accurate results while the LNA output appears as linear as a stand-alone LNA.

### 4.3 Mixer

The mixer behavioral model is a Volterra baseband equivalent model with two different paths for linear and intermodulation signals, as described in [11]. Since the direct conversion mixer exhibits a low pass behavior due to the \( RLC \) load, the linear path consists of a linear gain stage and a first order low-pass filter. The linear performance indices are obtained by measuring \( CG(f) \) both at DC and at 1 MHz through simulation.

The non-linear path is accounted for by a third order polynomial (which includes the even coefficient \( k_2 \) to evaluate the \( IM2 \) of the whole receiver). The polynomial coefficients are obtained from simulations according to:

\[
y = k_1 x + k_2 x^2 + k_3 x^3 \\
k_1 = CG(1MHz) \\
k_2 = \frac{IM2(2GHz)}{1MHz} \\
k_3 = 4 \frac{IM3(1MHz)}{V^3}
\]

where \( CG \) (conversion gain) is evaluated at 1 MHz to maximize accuracy on linear tests according to Tab. 1 (the Local Oscillator (LO) shifts input frequency downwards by \( f_{LO} = 2.1 \) GHz). In order to evaluate second order intermodulation products, a constant 3x worst case mismatch has been enforced. Since the mixer is driven by a current source during characterization, interface distortion is embedded into \( k_3 \) according to:

\[
IM3_{Mix} = \frac{3}{4} k_3 V_{in}^3 = \frac{3}{4} k_3^L + CG \cdot k_3^{CG \cdot L} V_{in}^3
\]

Table 3: Characterization process results. \( I_{eff}/I \) measures the effectiveness of AC gains in constraints in reducing the number of simulations required for performance model generation.

<table>
<thead>
<tr>
<th>Platform</th>
<th>( \text{dim}(I) )</th>
<th>( \text{dim}(O) )</th>
<th>( I_{eff}/I )</th>
<th>Time</th>
<th>#Sim</th>
</tr>
</thead>
<tbody>
<tr>
<td>nLNA</td>
<td>11</td>
<td>8</td>
<td>(&lt; 1.9 \cdot 10^{-8})</td>
<td>50h</td>
<td>2080</td>
</tr>
<tr>
<td>npLNA</td>
<td>13</td>
<td>8</td>
<td>(&lt; 7.9 \cdot 10^{-7})</td>
<td>52h</td>
<td>2480</td>
</tr>
<tr>
<td>Mixer</td>
<td>20</td>
<td>7</td>
<td>(&lt; 3.8 \cdot 10^{-8})</td>
<td>81h</td>
<td>2240</td>
</tr>
</tbody>
</table>

5. THE TOP-DOWN PHASE

We are interested in deriving the most general constraints that guarantee UMTS compliance that can be exploited to compare different front ends during exploration. Several considerations have to be accounted for when deriving minimum requirements for direct conversion UMTS front ends. While the large signal bandwidth allows using a solution with moderate \( \frac{1}{2} \) noise and DC offsets, sensitivity and intermodulation requirements remain hard to satisfy. From the system level, sensitivity requirements can be expressed in terms of oscillator phase noise, noise figure and second order non-linearity with the following relations as originally
Table 4: Mixer performance evaluation setup.

derived in [3]:
\[ D_2 = \frac{1}{G_R} (P_2 + N + P_{rm}) \leq -99\text{dBm} \] (1)

where \( P_2 \) is the output-referred second-order distortion power, \( N \) the output-referred noise power, \( P_{rm} \) the output-referred power due to reciprocal mixing and \( G_R \) the front-end gain. Similar considerations may be applied to third order distortion leading to the condition:
\[ D_3 = \frac{1}{G_R} (P_3 + N + P_{rm}) \leq -96\text{dBm} \] (2)

Eqns. (1) and (2) summarize feasibility requirements for a UMTS direct conversion receiver and will be used in the receiver optimization process. All quantities involved in equations are evaluated by means of behavioral models for the LNA and the mixer. A frequency-domain simulator has been setup to evaluate receiver performances given platform behavioral models and a performance vector \( \zeta = [\zeta_1, \zeta_2] \). Since the top-down phase is characterized by design exploration using behavioral models, it is of utmost importance to assess both the required accuracy of the receiver behavioral model and the sensitivity of the optimization on receiver performance estimations.

5.1 Model accuracy requirements

Model accuracy requirements have been derived through sensitivity analysis based on the feasibility constraints (1) and (2). Assuming that we can tolerate errors less than 3 dB on both \( D_2 \) and \( D_3 \), we derived constraints on model accuracy. Perturbations on \( D_2 \) can be expressed as:
\[ \frac{\Delta D_2}{D_2} = \frac{\Delta N}{N} \left( \frac{N}{G_R^2 D_2} \right) + \frac{\Delta P_2}{P_2} \frac{P_2}{G_R^2 D_2} - 2 \frac{\Delta G_R}{G_R} \leq 30\% \] (3)

We did not consider reciprocal mixing terms since the LO platform was not built. In the rest of the paper, we assume that phase noise is constant at the -155 dBc/Hz value reported in [3]. In order to derive the single terms in (3), we use a simplified frequency domain receiver model with polynomial non linear stages described by:
\[ |V_{in}| \approx A \cdot G_L \cdot CG \] (4)
\[ N_0 = 4KTR_0 (G_L F_L \cdot CG) + CG \cdot IRN_M \] (5)
\[ |V_{IM_2}| \approx \frac{kM}{2} A^2 G_L^2 \] (6)
\[ |V_{IM_3}| \approx \left[ \frac{kL}{2} A^3 \cdot CG + \frac{kM}{2} (AG_L)^3 \right] \] (7)

where \( G_L \) is the LNA gain, \( CG \) is the mixer Conversion Gain, \( F_L \) is LNA noise factor, \( IRN_M \) is the input referred noise of mixer, \( k_2 \) and \( k_3 \) are non-linearity coefficients. A two-tone input with amplitudes \( A_1 = A_2 = A \) has been assumed and the frequency dependency of the system has been neglected. Using Eqns. 4-7, we can derive:
\[ \frac{\Delta N}{N} \approx 2 \frac{\Delta G_L}{G_L} + 2 \frac{\Delta CG}{CG} \] (8)
\[ \frac{\Delta P_2}{P_2} = \frac{\Delta G_L}{G_L} + 2 \frac{\Delta k_2}{k_2} \] (9)
\[ \frac{\Delta G_R}{G_R} = \frac{\Delta G_L}{G_L} + \frac{\Delta CG}{CG} \] (10)

and finally, substituting Eqns. 8-10 into 3:
\[ \left| \frac{\Delta D_2}{D_2} \right| = \left| \frac{\Delta N}{N} \left( \frac{N}{G_R^2 D_2} \right) + \frac{\Delta P_2}{P_2} \frac{P_2}{G_R^2 D_2} - 2 \frac{\Delta G_R}{G_R} \right| \leq 30\% \] (11)

If we assume variations to add in power, Eqn. (11) describes an ellipsoid in \( \mathbb{R}^3 \), relating LNA gain and mixer second order nonlinear coefficient and gain. Similar expressions can be obtained for \( D_3 \) starting from (2). Overall, sensitivity analysis results can be exploited to set accuracy requirements on behavioral models. If we allow maximum error on \( G_L \) and \( CG \) to be 5% and use nominal values as in [3] to evaluate Eqns. 3 and 11, then errors on mixer second and third order intermodulation product may be tolerated within 174% and 147% in power (respectively 74% and 69% in worst case additive contributions) having an overall accuracy of 30% on feasibility constraints.

5.2 Model validation

To validate model accuracy we compared our models with SPECTRE simulations both for the single blocks and for the entire receiver system. For the LNA, linear response error is within 5% in a ±120 MHz bandwidth around \( f_0 \). Third order intermodulation product is reproduced with an accuracy better than 30% on a 200 MHz × 200 MHz square in the \( f_1,f_2 \) when \( V_1 = -40\text{dBm}, V_2 = -30\text{dBm} \). The complete receiver model was finally validated over 165 composable platform instances. Receiver behavioral models were compared with corresponding circuit level simulations, as reported in Tab. 5. Note that (i) distortion tones are sensitive to cumulate non-linearity inaccuracies with linear gain errors, therefore are intrinsically difficult to model exactly; (ii) since the characterization process tends to generate mixers with large transistors (and thus good matching properties), device mismatch becomes small and makes simulations unreliable unless expensive accuracy settings are used, which is however not necessary due to the IIP2 saturation introduced in Sec. 4.3. As for \( IM_3 \), we opted to add the mixer and LNA contributions in Eqn. (7) discarding phase information (which is out of the scope of the behavioral models used) so that conservative estimates are provided.

Overall, behavioral models accuracy is compatible with the requirements derived in the previous section for power additive errors. Significant improvements over the results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>( CG, IRN )</td>
<td>PSS @fRSS = 2.1GHz, ( V_{inCG} = -40\text{dBm} ); PAC 2.1GHz → 2.03GHz, ( V_{inCG} ) noise 10kHz → 1.92MHz</td>
</tr>
<tr>
<td>( IM2 )</td>
<td>PSS @( f_1 = 1.966GHz ), ( V_{inIM2} = -78dBm ); PAC @( f_2 = 1.959GHz ), ( V_{inIM2} )</td>
</tr>
<tr>
<td>( IM3 )</td>
<td>PSS @( f_1 = 2.03GHz ), ( V_{inIM3} = -69dBm ); PAC @( f_2 = 1.961GHz ), ( V_{inIM3} )</td>
</tr>
</tbody>
</table>

Table 5: Comparison between receiver behavioral simulations and Spectre simulations. Rows show (for different quantities) the percentage of receivers providing an error lower than the value in column.

\begin{tabular}{|c|c|c|c|}
\hline
Performance & ±2dB & ±3dB & ±6dB \\
\hline
\( IM3_{LNA}(2.101GHz) \) & 93% & 99% & 100% \\
\( LNA_{out}(1.965GHz) \) & 88% & 98% & 100% \\
Linear_{out}(1MHz) & 99% & 99% & 100% \\
\( IM2_{out}(1MHz) \) & 10% & 36% & 65% \\
\( IM3_{out}(1MHz) \) & 15% & 39% & 80% \\
\hline
\end{tabular}
shown in Tab. 5 seem hard to obtain due to the compactness of the behavioral models involved and the relevance of parasitics and second-order effects at RF.

5.3 Optimization

In our methodology, optimizations can be efficiently carried out since the architectural space is well delimited and performance models that can be evaluated quickly are provided. By annotating behavioral models with architectural constraints, we can afford to use expensive stochastic optimization algorithms such as simulated annealing. The selection of an optimal cost function to drive the optimization process is an issue since multiple objectives are usually pursued [13]. However, we can perform our computations with a number of different trade-off parameters to expose the designer to a number of potential performance of the design, letting her to decide on the trade-off she is satisfied with.

In our case, we casted a design space exploration problem as an optimization problem over a receiver platform consisting of two LNAs and a mixer. We set up different optimization problems for different cost functions and constraints. Eqs. (1) and (2) were used as UMTS feasibility constraints. The cost function is a weighted sum of power, area and penalty functions. In mathematical terms, the optimization problem can be formulated as:

\[\min_{\zeta \in \Omega_{\text{Gain}}} \left\{ \theta_1 \cdot P + \theta_2 \cdot F_1(NF - NF) - \theta_3 \cdot F_2(G - G) + \theta_4 \cdot F_3(A) \right\} \]

s.t.

\[
D_2 \leq -90 \text{dBm}, \quad D_3 \leq -90 \text{dBm} \\
P_L(\zeta_L) = 1, \quad P_M(\zeta_M) = 1, \quad \lambda_{LNA} \geq \lambda_{Mix}
\]

(12)

\(F_1\) is a tanh-shaped penalty function that forces the receiver NF not to exceed \(NF\) (the minimum allowed NF obtained by the simultaneous solution of Eqs. (1) and (2)) by more than a few tenths of dB. \(F_2\) is a parabolic penalty function that controls both the width of the allowed gain variations with respect to the \(G = 31\) dB (value of the reference design) and area penalty. Note that, since the LNA platform is built as the union of performance models corresponding to two LNA topologies, \(P_L = 1\) if either \(P_L^{np}(\zeta_L)\) or \(P_L^{m}(\zeta_L)\) is 1.

As a consequence, the optimization problem automatically selects LNA topology and platform parameters (in this case LNA and mixer performances) that are optimal in the sense specified by (12).

Platform-based analog design casts the optimization problem in the performance space (\(\zeta\)) rather than the configuration space (\(\kappa\)). From circuit designer perspective, it may seem an unnatural choice, however it is the key to perform architecture selection automatically since all unnecessary implementation details (e.g. topology sizing) are hidden behind the platform abstraction. At the end of the optimization process, an optimal performance vector \(\zeta\) is returned (along with optimal topologies where applicable). Given \(\zeta\), minimum distance configurations (nearest neighbors) can be recovered among the configurations simulated during the platform characterization process. The corresponding configuration vectors \(\kappa\) can then be returned as starting points for low-level optimization refinements.

Due to the high dimensionality of performance model relations and the tight correlation among performance figures, generic simulated annealing engines tend to be very inefficient in generating feasible configurations. Therefore, we developed a customized optimization library based on [14] that embeds performance constraints in its random configuration generator. Receiver optimization can then be performed in \(\approx 30\) min. on an Athlon XP2600 workstation, generating more than 50,000 receiver configurations.

5.4 Results

Several optimization runs were performed according to different cost functions, as reported in Tab. 6. Due to the stochastic nature of the algorithm, the optimization process may end up in a local minimum. Therefore, we performed each run 5 times selecting the median solution. Tab. 6 shows optimizations sorted by tighter constraints and/or more demanding cost functions. The first column reports the absolute minimum power solution for a UMTS compliant front end. Power savings of 47% are achieved with respect to the original design, which however has higher performances than basic UMTS requirements. On the other hand, if a reward function is used for NF lower than the minimum required, power savings of 30% can be obtained, as reported in the second column. The third column constrains the re-
receiver gain to be equal to the reference design 31 dB gain. The added constraint provides an optimal solution with 40% power savings. The fourth column, which adds a safety margin of 2 dB with respect to NF, provides a design that is very similar to the original design. From the system equations (4)-(7) and UMTS constraints (1)-(2) it can be inferred that a margin of 2 dB on NF allows for IIP2 and IIP3 errors respectively of 20 dB and 15 dB (well within the model accuracy). The fifth column reports optimization results when area is included as well. This case selects a different LNA topology (nPMOS) as it allows, coupled with the mixer, to meet UMTS constraints with smallest (estimated) area. Finally, we note that the reference NF performance is not immediately comparable with optimization NF, since an average NF was used here while minimum was reported for the receiver. Moreover, input impedance matching was relaxed in the reference design providing further improvements in noise performances.

A pictorial view of the architecture selection process is shown in Fig. 8. Tab. 7 reports receiver performances derived from optimization of case 3 and performances of closest receiver instances. Tabs. 8 and 9 report detailed LNA and Mixer performance breakdown for the optimal receiver. Overall, the optimization process proved to be a very flexible and efficient mean for evaluating system level tradeoffs in a systematic way. A design criterion leading to a solution very close to the original design was found, which shows that the original design could be considered optimal according to a cost function that was not known in an explicit form at design time.

### 6. CONCLUSIONS

We demonstrated the effectiveness of the analog platform based design paradigm on a state-of-the-art UMTS receiver front-end. Exploiting accurate models intrinsic in the platform abstraction, efficient exploration of the UMTS design space was possible at the behavioral level. A range of different tradeoffs have been exposed to designers, allowing the selection of optimized platform instances. Results show that exploring different corners of the design space allows very important savings in power consumption, leading to a minimum power UMTS front end consuming as low as 9.6 mW. Finally, the proposed methodology allows performing architecture selection as part of the exploration process and evaluating new architectures very efficiently.

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### 8. REFERENCES


