ABSTRACT
Scan-based designs effectively reduce test generation complexity and thus deliver improved fault coverage. Nevertheless, the traditional scan architectures suffer from increased test time and test data volume. The CircularScan architecture [1] provides a flexible environment for test cost reduction. The new scan design enables the use of the captured response of the previously applied test pattern as a template. The subsequent pattern is loaded by efficiently performing the necessary changes on the template through the functionality provided by the new architecture, conceptually exploiting the inherent low specified bit density of the test patterns. We explore the space of possible design alternatives built on the CircularScan architecture; the design alternatives are presented with accompanying test application methods. The experimental results indicate a substantial test cost reduction, reaching 90% levels. The proposed scheme is not only easily scalable but also promises further reductions in test cost when applied to large state of the art ICs.

1. INTRODUCTION
The increasing level of integration capability enables the incorporation of enhanced functionality into a single chip. Nonetheless, the increasing complexity of the circuits imposes a limitation to the applicability of sequential test generation. Scan-based designs have emerged as a solution to keep the complexity of test generation within practical limits. Full scan-based design enhances the controllability and observability of a circuit by configuring all memory elements in the circuit as a shift register.

The reduced test generation complexity achieved by the scan-based designs can be costly in terms of test application time and test data volume as a result of the serial access mechanism. Employing multiple scan chains can reduce test application time; nevertheless, the increase in the number of scan I/O pins necessitates a higher cost automatic test equipment (ATE) with high pin counts and high memory bandwidth. Current costs of such ATEs range at the levels of thousand dollars per pin [2]. A number of methods have been proposed in the literature to reduce test cost [1, 3, 4, 5, 6, 7, 8, 9]. Generally, the proposed schemes utilize a compression method in conjunction with an on-chip decomposition hardware. Golomb code [3] and Nine-Coded [4] compression schemes exploit the variable frequencies of test pattern blocks so as to efficiently store the test data. The scan cells are partitioned into the internal scan chains in [5] and all scan chains are loaded in parallel by the same test data; serial load is used for the faults that cannot be detected by the parallel load. A feedback architecture that enables the use of prelude vectors to resolve the dependencies generated by the parallel load mode in [5] is presented in [6], essentially eliminating the serial test patterns. The number of scan chains visible to the tester is reduced in [7] through a decompression network that exploits the low specified bit density of the test vectors. A part of the captured response is utilized in constructing the subsequent test vector in [8]. A configurable circular scan design is presented in [9], wherein the scan chains are constructed in a grid-like structure.

In order to enjoy the reduced test generation complexity delivered by scan-based designs, the high test application time and test data volume have to be reduced. It is paramount furthermore to ensure that the approach for test cost reduction limits the number of scan I/O pins due to the high cost of current ATEs with high pin counts. In practice, even compacted deterministic test patterns generally consist of a small number of specified bits, 1-5%, as reported [10]. Although the specified bit density of the test patterns is quite low, the traditional scan architecture does not allow the exploitation of this property. The unspecified bits of the test patterns are set randomly or by deterministic algorithms, resulting in the fully specified test pattern being shifted in.

A novel scan architecture that conceptually exploits the aforementioned low specified bit density of test patterns for test cost reduction is presented in [1]. The proposed scan architecture, denoted as CircularScan, configures the scan chains in a circular form. The new architecture differentiates itself from the previously published methods in a number of aspects. The circular configuration of the scan chains enables the use of the captured response as a template and also supports the multiple rotations of the scan chain content. Although previous approaches such as [8] also use the captured response for the next pattern, they partially shift out the captured response, using the remaining parts of the response for the next pattern. Since the captured response is not fully observed, a computationally complex analysis is required to provide full fault coverage. CircularScan, on the other hand, enables the observation of the captured response fully after the first rotation, eliminating any possible fault coverage loss. The original scan I/O pins are utilized only for addressing the scan cells that are at variance with the next pattern. CircularScan subsequently facilitates an exponential increase in internal scan chain count, delivering a commensurate reduction in average access time to a particular scan cell in comparison to the traditional scan architecture.

Although CircularScan harbors a slew of novel properties as outlined in the last paragraph, its rather restricted form as described in [1] sharply limits its applicability. The proposed design utilizes all scan inputs to address a conflicting location on the template and the conflicting bits are updated one at a time. Furthermore, CircularScan as constructed in [1] introduces a new problem that does not exist with the traditional scan architecture. Since the captured response is used as a template, when an error is captured in the scan cells, it may continue to stay in the scan cells. Although it does not pose a problem to testing, as one may observe the failure for all subsequent test vectors after the first failing test vector, the
diagnostic resolution of the test set may diminish in comparison to a traditional scan architecture.

Although the technique is rather limited in [1] and suffers from a loss of diagnostic resolution, the underlying properties of CircularScan are quite promising and evince a large design space of various alternatives worthy of exploration. In this paper, we identify the design space that is rooted on the underlying properties of CircularScan and point to the possible directions in this design space. Furthermore, various test application methods with possible designs are discussed.

Section 2 discusses the design space based on the fundamentals of CircularScan. Section 3 outlines two particular design alternatives that in some sense constitute two extremal points of the design space and discusses their functionalities as a case study. Section 4 presents a number of test application methods with the alternative designs. Section 5 outlines a diagnosis process that solves the problem of diagnostic resolution loss in CircularScan. Section 6 presents an experimental evaluation of the discussed architectures and a brief conclusion is offered in section 7.

2. DESIGN SPACE

In the traditional scan architecture, since the test data is shifted into the scan chains one bit at a time, the low specified bit density of the test vectors cannot be exploited. The CircularScan architecture allows for the rapid application of only the specified bits of a test pattern in a substantially reduced test application time. The design employs a small number of scan I/O pins in order to keep the cost of the ATE low and the captured response of the applied patterns is fully observed in order to preserve the original fault coverage of the test set. However, since only one bit can be updated each cycle, the test slice with the maximum number of conflicting bits defines the test application time; a quite high number of rotations subsequently may be necessary in order to apply a single pattern.

At least one dimension in which the traditional CircularScan architecture can be extended is through the introduction of a broadcast mechanism to enable loading multiple bits each test cycle. The original design uses all possible scan inputs for addressing the internal scan chains, essentially aiming at maximizing internal scan chain count and subsequently attaining a maximum decrease in average scan chain length. The motivation for maximizing the internal scan chains leads us to the use of only one of the scan selection input combinations for the broadcast mode, delivering the broadcast control mechanism through a minimal decrease in the number of the internal scan chains as can be seen in Figure 1. When the scan selection input combination reserved for the broadcast mode is assigned, all scan chains are broadcast with the logic value on the data input, setting all the bits in the current slice to the particular logic value. Multiple benefits accrue through the examination of various broadcast alternatives, primarily drastic test application time reductions and also most importantly resolution of the diagnosis problem that traditional CircularScan introduces.

The use of all possible scan inputs through a decoder may potentially address an exceedingly large set of scan chains in the circuits with a high scan input count. If the scan input count is larger than 16 for instance, it may not be practical to have 32K scan chains. Assuming that S scan inputs and 2^m internal scan chains exist, only n scan inputs are required to address 2^n internal scan chains and the utilization of the remaining m=(S-n) scan inputs enables the exploration of various design alternatives. In [1], these design alternatives are overlooked and only a single bit update mechanism that needs only the addressing of each single scan chain is employed. Naturally, a rather complex addressing mechanism by exploiting a control mechanism the remaining unutilized m scan inputs in the original design points to a possible direction in the design space. n scan inputs can be used to deliver the original addressing mechanism as depicted in Figure 2 and the remaining m scan inputs can be utilized to select among 2^m different combinations such as odd numbered cells, even numbered cells, and various other partitioning mechanisms. The addressing block can be shaped according to the circuit structure, test set or to trade off between addressing complexity and hardware overhead.

As mentioned above, broadcasting is a quite powerful mechanism due to its support for diagnosis and various test application alternatives. The utilization of the remaining m scan inputs for controlling various configurations of a reconfigurable broadcast network points to additional directions in the design space as depicted in Figure 3, enabling the selection among one-bit-update or various broadcast configurations. One important advantage of having extra control signals to select either one-bit-update or broadcast mode is that since the scan selection inputs are not used for broadcast control, they can be utilized to carry test data during the broadcasting.

The complex addressing mechanism and reconfigurable broadcasting structure constitute distinct axes in the design space; they can be combined in the same design to generate aggressive architectures to reduce test cost.

One simple but effective design alternative is reserving one scan input to select between broadcast/one bit update modes instead of using a scan selection input combination. Since the scan selection inputs are not needed to activate the broadcast mode, all of them can be utilized to broadcast test data. Scan chains are partitioned into groups and each of them is broadcast with a different scan input. Consequently, the restriction of the original broadcast method to assign all bits of a test slice to a common value is eliminated and each group of a test slice can be assigned to a different logic value. This method will be analyzed in detail in section 3.

In this section, design alternatives that can be built on the traditional CircularScan have been discussed. Due to their simplicity and the possible test cost reduction they promise, we select two design alternatives that are located at two distinctly different points of the spectrum in our subsequent case study. The design that uses one of the scan selection input combinations for the broadcast mode is selected as the first case study in order to explore possible improvements on CircularScan with simple modifications. In order to observe the contribution of extra scan inputs in the simplest form, the design with a single addressing mechanism and a dedicated scan

![Figure 1: Full Test Slice Broadcasting](image1)

![Figure 2: Complex Addressing Schemes](image2)

![Figure 3: Reconfigurable Broadcast Network](image3)
input pin to select between broadcast/one-bit-update modes is selected as a second case study. In section 3, these particular designs are presented in detail and section 4 presents various test application alternatives that were infeasible with traditional CircularScan.

3. DESIGN ALTERNATIVES

The first design, denoted as Full Broadcast, allocates one of the possible scan selection input combinations for the broadcast mode as depicted in Figure 2. In the second design, denoted as Dedicated Broadcast, as shown in Figure 4, one of the scan inputs is dedicated to distinguish between the one-bit-update and the broadcast mode. In the one-bit-update mode, both designs utilize only one of the original scan I/O pins to load the test data instead of all N scan I/O pins being used for loading the test data in the traditional scan architecture. The remaining scan inputs are used to identify a particular internal scan chain through a decoder, enabling an exponential increase in comparison to the traditional scan architecture. Although the number of scan chains is exponentially increased while retaining the original scan I/O count, parallel access to the scan chains is limited, making only possible a load to a single scan chain each cycle.

In these architectures, scan chain outputs are also connected to the scan chain inputs in addition to being connected to the MISR. In the test application process, not only the selected scan chain but also the remaining scan chains shift one bit. The scan selection inputs identify a scan chain and test data is loaded through the data input to the selected scan chain. Since scan chain outputs are connected to scan chain inputs through a selection unit and all scan chains shift, only the cell at the head of the selected scan chain is set with new data and the remaining cells are sourced with the current content of the scan cells at the tail end of the chains. Consequently, at the conclusion of a complete rotation of the scan chains, the captured response of the previously applied pattern is sourced to the MISR with no change, providing full observability, and the captured response remains in the scan cells with only one bit change on each slice. In Full Broadcast, when the scan input combination that has been assigned to the broadcast mode is selected, all scan chains are loaded with the same value on data input. In Dedicated Broadcast, when the broadcast mode is selected, the scan chains are divided into \( N - 1 \) groups and the broadcast inputs in the selection units of the scan chains in the same group are connected to a particular scan I/O pin. Consequently, the broadcast mode adds to Dedicated Broadcast the functionality of assigning the scan chains in the same group to a common value, thus augmenting its previously discussed functionality of setting a selected scan cell in the current slice.

4. TEST APPLICATION

Any possible design in the discussed design space that supports the broadcast mode provides flexibility to explore various test application approaches. Test application is first presented in its simplest form in section 4.1 by utilizing the extra functionality provided by the broadcast mode. A test generation method, considering the constraints introduced by the new scan design, is presented in section 4.2; section 4.3 proposes an iterative constrained compaction process in order to further exploit the proposed scan architectures. The compaction algorithm employed in this work, a slightly modified version of the one presented in [7], is shown in Figure 5.

4.1 Test Application with Broadcast Mode

Essentially, the captured response on the scan cells to the previously applied test pattern is used as a template for the next test pattern. The content of a scan cell is changed if it corresponds to a specified bit of the next pattern to be applied and if its current content is at variance with the particular specified bit. In the current test slice, if a set of bits differs from the corresponding bits in the scan cells, one of them is selected through the decoder and the value in the scan cell is updated through the data input. In the test application with the one bit update strategy as in the original CircularScan, the test slice with the highest number of conflicting bits determines the rotation count of the scan chain content. The broadcast mode is to be preferred for updating the content of the template in the process of obtaining the next test pattern if there exists a logic value with fewer occurrences than the number of conflicting bits. The other logic value, ‘0’ or ‘1’, with the higher count in each scan chain group of the current slice is selected to initially load the scan chain groups with it by using the broadcast mode. The specified bits in need of the complementary value are toggled using the original update procedure.

**Example** This example utilizes Dedicated Broadcast. The same steps can be used to apply test vectors with Full Broadcast by assuming all scan chains as a single group. Assume that the captured response for the previously applied test pattern in a test application process is given in Figure 6(a) and the next test pattern to be applied is given in Figure 6(b). If the traditional scan architecture with 5 scan I/O pins and a total of 40 scan cells is used, the application of the next test pattern requires a total of 8 cycles assuming perfectly balanced scan chains. In Dedicated Broadcast, 5 scan I/O pins support 8 internal scan chains, resulting in 5 scan cells for each scan chain as in Figure 4. An examination of the test data shows that
respectively, enabling the load of the slices 1, 3, 4 and 5 in one cycle each. Although the update of the conflicting bits in slice 2 requires 4 cycles, necessitating 4 full rotations of the scan chain content, a closer look reveals that the specified bits in each group are all logic 0s or 1s in slice 2. Therefore, the broadcast mode can be utilized to set all the specified bits of slice 2 in one cycle.

In the first cycle, chain 5 is selected through the scan selection inputs and logic 1 is shifted through the data input. All the other chains are sourced with the data in the scan outputs. Since all scan outputs are connected to the MISR, the captured response on the last slice is fully observed after the first cycle and the scan content is shown in Figure 7(a). Scan chains 2, 5 and 1 are selected in cycles 2, 3 and 5 and logic 0, 1 and 0 are shifted through the data input, respectively. In cycle 4, the broadcast mode is selected and logic 1, 0, 1 and 0 are shifted into scan chain groups, respectively. The scan content is shown in Figure 7(b)-(d) after the cycles 2, 4 and 5, respectively. The test application time is reduced to 5 cycles instead of the original 8 cycles in a traditional scan architecture and an associated test data volume reduction to 25 bits from the original 40 bits is attained. The resultant new test data is shown in Figure 8, wherein the first three bits of each entry denote the scan selection inputs, the fourth bit denotes the data input and the last bit denotes the broadcast mode bit.

Although the provided example assumes a fully known test response, the proposed approach is still applicable when the captured response includes unknown values. If a specified bit of the next pattern corresponds to an unknown value on the captured response, the unknown value is updated by the corresponding specified value of the subsequent pattern. On the other hand, if an unspecified bit of the next pattern corresponds to an unknown value on the captured response, the unknown value can be kept as is with no change and fault dropping is performed with a partially specified test vector; alternatively, the unknown value can be set to a specific value through the one bit update functionality of the architecture.

### 4.2 Test Generation under Constraints

The presented test application process uses the test sets that have been generated with no particular heed paid to the structure of the design. A test generation process that utilizes the properties of the architecture can deliver increased benefits in cost reduction. The broadcast mode provides an opportunity to set all the bits of a test slice without using the captured response on the scan cells of this particular slice. Nonetheless, the scan chains in the same group are constrained to the same logic value. A test generation even under the aforementioned constraints may be able to detect a large subset of the faults in the circuit. Since the new test set is generated under the assumption that the scan chains in the same group are assigned to the same logic value, the application of a test vector requires only one full rotation of the scan chains, utilizing the broadcast mode at each cycle.

A subset of the faults remains undetected after the test generation with the constrained values. Test generation for the undetected faults is performed by removing the constraints, resulting in a second test set. The second test set is applied as in section 4.1 by using the captured response as a template.

### 4.3 Compaction under Constraints

As presented in section 4.2, a high fault coverage can be provided with a test generation that imposes the constraints to the bits of the test slices, enabling a test vector application for each rotation. Although this constrained test generation provides an effective solution for the detectable faults, the test set for the remaining faults is generated from the test cubes by the compaction procedure shown in Figure 5. The provided compaction procedure assumes no knowledge regarding the structure of the design.

The compaction procedure is slightly modified in order to exploit the properties of the architecture. The compatibility check step of the compaction procedure is updated as follows. Initially, the maximum rotation count for the test application is set to 1. The compatibility check step calculates the rotation count in the architecture after a possible compaction; the compaction is allowed only if the rotation count after the possible compaction does not exceed the current maximum rotation count. When no more compaction is possible and the faults remain in the fault list, the maximum rotation count is increased. The presented incremental constrained compaction procedure iterates until the fault list is exhausted.

### 5. Diagnosis Process

All design alternatives that have been discussed enable the use of the captured response as a template for the next pattern. While the template is being updated for the next pattern, the captured response is fully sourced to the MISR after the first rotation. If a fault exists on the captured response, since it is fully observed on the MISR, it poses no problem for test purposes. Nevertheless, the outlined process constitutes a challenge during the diagnosis application. If any faulty part of the captured response is used for the next pattern with no alteration, all subsequent test patterns fail until the faulty part is corrected. Since a sequence of failures occurs after the first failure, the diagnostic resolution of the test set decreases. For example, in Figure 9(a), the pass/fail information is shown for the faults $f_1$ and $f_2$ when a test set of 5 patterns is applied. The pass/fail information suffices to distinguish the given fault pair. If the architectures that use the captured response as a template are employed and any faulty part of the captured response is used for the next pattern after the application of the second test pattern, the fault propagates to the other patterns and a pass/fail information as shown in Figure 9(b) may be observed, making the faults $f_1$ and $f_2$ indistinguishable.

The broadcast mode enables the setting of all the bits of a test slice, clearing any possible fault on the captured response. Subsequently, the broadcast mode can be utilized throughout the first rotation of scan chains during the application of each test vector,

\[
\begin{array}{cccccc}
& T_1 & T_2 & T_3 & T_4 & T_5 \\
T_1 & P & F & F & F & F \\
T_2 & P & F & F & F & F \\
T_3 & P & F & F & F & F \\
T_4 & P & F & F & F & F \\
T_5 & P & F & F & F & F
\end{array}
\]

**Figure 9: Diagnostic Information**
removing any fault part on the captured response. The outlined broadcast solution for the diagnosis problem may increase test application time; yet as the diagnosis application frequency pales in comparison to the test application frequency, the increase in diagnosis application time can be assumed to be negligible. Consequently, any design alternatives that support the broadcast mode can solve the problem of diagnostic resolution loss of the original CircularScan.

The sufficiency of limited pass/fail information at particular sets of points during diagnostic application to deliver full pass/fail resolution instead of observing individual pass/fail information after each test vector has been previously shown in [11]. Consequently, it suffices to apply the outlined full broadcast solution only for a subset of test vectors instead of all test vectors, thus improving the diagnosis application time.

6. EXPERIMENTAL RESULTS

The performance of the proposed method has been analyzed on the larger ISCAS89 [12] benchmark circuits. The ATALANTA test generation tool [13] and the HOPE fault simulation tool [14] have been used for the experiments.

In the first set of experiments, test application time and data volume reduction ratios are analyzed with both Full Broadcast and Dedicated Broadcast for three different test application methods; test application with no architecture specific test generation, $M_1$ as in section 4.1, test application with test generation under imposed constraints, $M_2$ as in section 4.2, and test application with an incremental constrained compaction, $M_3$ as in section 4.3. Table 1 lists test time reduction results, wherein the second, third, fourth and fifth columns denote test application time reductions with the methods $M_1$, $M_2$ and $M_3$ in both Full Broadcast and Dedicated Broadcast for scan I/O pin counts of 7, 8 and 9, respectively. The reduction in test cost is calculated by comparing the result obtained to that of the traditional scan architecture for the same number of scan inputs. As CircularScan [1] constitutes the most relevant comparison point, the seventh columns for scan I/O pin counts of 7, 8, and 9 in Table 1 report the results in [1] for comparison purposes. A closer look indicates that Dedicated Broadcast delivers, on average, a 42% improvement in comparison to [1]; it can be seen that the average improvement is even further magnified as the scan input count grows. Additional confirmation of the superiority of Dedicated Broadcast can be obtained by looking at the test data volume reduction ratios which closely track those of test time reduction; Table 2 reports the highest reduction ratios, $M_3$, among $M_1$, $M_2$ and $M_3$ together with the previously reported results of [1] for each.

All scan architectures based on the circular structure exploit the low specified bit density of the test vectors to reduce test data volume and test application time. Nevertheless, the specified bit densities of test sets for the ISCAS benchmark circuits are quite high in contrast to the values reported for industrial circuits. The results in Tables 1 and 2 show that test cost reductions reaching 90% levels are achievable even with the high specified bit densities of the test sets of the ISCAS benchmark circuits. It is to be expected that the proposed approach delivers even further reductions for the larger industrial circuits, wherein typical specified bit densities of 1-5% prevail.

The outlined design alternatives exponentially increase the number of scan chains while retaining the original scan input count. Consequently, the test cost savings of the method can be observed best in circuits with a high scan cell and scan I/O pin counts. Since the benchmark circuits are comprised of quite a small set of scan cells, test cost reduction can be reported herein up to the scan I/O pin count of 10 only. Consequently, the reported test cost reduction levels even for this small number of scan I/O pins promise a further increased test cost reduction for the large state of the art ICs. The steady increase in cost reduction as the scan I/O count gets larger in Tables 1 and 2 supports the expected higher levels of test cost reduction in the larger circuits.

In a second set of experiments, in order to analyze the effect of the specified bit density of the test vectors on test cost reduction, the compaction process is slightly modified to terminate when the specified bit density reaches a predetermined value. The graph in Figure 10 depicts test time reduction for the specified bit densities of 1-5% and for scan I/O counts from 7 to 10 when method $M_1$ is employed on the largest benchmark circuit, $S38584$. The steady increase in test time reduction as the specified bit density gets smaller and as the scan I/O count gets larger supports the expected benefits of the proposed method.

Table 1: Test Application Time Reduction

<table>
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<tr>
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Table 2: Test Data Volume Reduction

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$^1$ [1] reports results up to scan I/O pin counts of 9 only.
$^2$ Results for other circuits are omitted due to space limitations.
The ever-increasing complexity of today's state of the art ICs limits the applicability of sequential test generation; scan-based designs are subsequently widely employed to reduce test generation complexity. Nonetheless, scan-based designs substantially increase test application time and data volume. A scan architecture with a circular structure and an addressing mechanism defines a substantial design space of promising results. In this paper, this design space has been explored and possible directions in the design space have been identified.

The possible design alternatives exponentially increase the number of scan chains while retaining the original number of scan I/O pins visible to the ATE. The new designs enable the use of the captured response in the scan cells as a template for the subsequent pattern with the help of its circular configuration. Since only a small subset of scan inputs suffices to support a realistic number of internal scan chains, the remaining scan inputs may be used for various design alternatives, particularly for a complex addressing mechanism and a reconfigurable broadcast network. These design alternatives are explored and a number of test application methods that exploit the extra functionalities are presented.

The experimental results indicate that a substantial reduction in test cost can be achieved, exceeding 90% levels for some benchmark circuits even with the simpler design alternatives. The proposed designs promise even further test cost reductions for large state of the art ICs with high scan I/O pins.

### 8. REFERENCES


