A Soft Error Rate Analysis (SERA) Methodology

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Abstract—We present a soft error rate analysis (SERA) methodology for combinational and memory circuits. SERA is based on a modeling and analysis-based approach that employs a judicious mix of probability theory, circuit simulation, graph theory and fault simulation. SERA achieves five orders of magnitude speed-up over Monte Carlo based simulation approaches with less than 5% error. Dependence of soft error rate (SER) of combinational circuits on supply voltage, clock period, latching window, circuit topology, and input vector values are explicitly captured and studied for a typical 0.18 µm CMOS process. Results show that the SER of logic is a much stronger function of timing parameters than the supply voltage. Also, an “SER peaking” phenomenon in multipliers is observed where the center bits have an SER that is orders of magnitude greater than that of LSBs and MSBs.

I. INTRODUCTION

Soft errors caused by particle hits [1], [2] are a serious problem for modern SRAM designs due to reduced feature size and supply voltage. Empirical soft error rate (SER) model has been proposed for SRAMs [3]. It predicts SER from critical charge $Q_{crit}$, drain area, neutron flux and other empirical parameters. Researchers have shown that SER in logic is posing a threat now [4] and will increase by orders of magnitude within the next few years [5]. Not much work on modeling and analysis of SER in logic is seen in open literature, although industry is clearly interested [4], [6]. Past work is based on expensive and time-consuming Monte-Carlo simulations [7], [8] or experiments [9] for specific combinational circuits in a specific technology and thus are hard to generalize. Prior work [5], [6] has also attempted the modeling of SER of logic circuits from a microarchitectural perspective. It is shown that a single $Q_{crit}$ value is not sufficient to describe SER in logic circuits, as both the storage nodes (e.g., D-flip-flops or registers) and the combinational circuit nodes are susceptible to particle hits. A single event transient (SET) generated by a particle hit at a combinational circuit node may experience electrical, latching-window, and logical maskings [5] before it reaches the next pipeline stage. So far there does not exist any work in studying the impact of transistor sizes, logic depth, circuit topology, clock speed, D-flip-flop (DFF) speed, supply voltage scaling, and input vector values on the SER of logic.

In this paper, we present a soft error rate analysis (SERA) methodology for combinational and memory circuits. SERA is based on a modeling and analysis-based approach that employs a judicious mix of probability theory, circuit simulation, graph theory and fault simulation. Dependence of SER on supply voltage, clock period, latching window, logic depth, circuit topology, and input vector is explicitly captured. Several interesting results are derived using SERA:

1. The SER of logic is a much stronger function of the clock period and DFF latching window than supply voltage. This implies that supply voltage reduction for energy-efficiency will not make SER significantly worse. For example, the SER of a 32 × 32 parallel carry-save array multiplier in a TSMC 0.18 µm technology increases by more than 50X when the latching window is decreased by 20% from 120 ps while it increases by only 28% when the supply voltage is decreased by 20% from 1.8 V.

2. SER analysis of multipliers shows an “SER peaking” phenomenon where the SER of MSBs and LSBs are three orders of magnitude greater than that of center bits.

3. SER of combinational circuits are indeed comparable or more than those of SRAMs with similar sizes. The SER of a 32 × 32 multiplier in 0.18 µm technology is higher than that of a 1 Kb SRAM in the same technology.

The paper is organized as follows. A probabilistic model is developed in section II, which relates soft error rate and soft error probability conditioned on an effective particle hit. SERA techniques for complex combinational circuits are presented in section III. Results from SERA are shown and compared with empirical model and Monte Carlo simulation in section IV. Conclusions and SER-tolerant circuit design guidelines are discussed in section V.

II. PROBABILISTIC ANALYSIS

We consider a canonical clocked logic circuit (CCLC) composed of a combinational circuit with latched primary inputs and outputs as shown in Fig. 1(a). Note that a memory array is a special case of CCLCs where only storage elements are present. A chip can then be treated as a network consisting of CCLCs.

Definition 1: A soft error is said to have occurred in the CCLC if a DFF captures the single event transient (SET) generated by a particle hit.

A. Soft Error Rate

The upper bound on the SER (number of soft errors per unit time) of a chip is given by

$$SER_{\text{chip}} \leq \sum_{k=1}^{N_C} SER_{\text{CCLC},k}$$

(1)

where $N_C$ is the number of CCLCs on the chip. The above equation is a tight bound only if all CCLCs are independent from each other. The SER of a memory array, for example, is the sum of SER for each memory cell. The modeling of different system-level derating mechanisms in a microsystem, which results in reduction in overall SER, has been explored in [6]. We focus on the modeling of SER in a CCLC in this paper.

The SER of a CCLC is defined as

$$SER_{\text{CCLC}} = R_{PH} \cdot \alpha \cdot P(\text{SE})$$

(2)

where $R_{PH}$ is the particle hit rate, $\alpha$ is the fraction of effective particle hits (those resulting in charge generation), and $P(\text{SE})$ is the probability of soft error conditioned on an effective particle hit. Note that the product $(R_{PH} \cdot \alpha)$ denotes the rate of effective particle hit. The concept of effective particle hit is an abstraction of several
In this paper, we will derive the rate of effective particle hit from an (NCS) method [10] and burst generation rate (BGR) model [11]. It is beyond the scope of this paper to discuss the physical processes in which particles interact with a semiconductor substrate to produce bursts of charge [2]. It is beyond the scope of this paper to discuss the physical nature of this phenomenon, which has been modeled in prior work such as neutron cross section (NCS) method [10] and burst generation rate (BGR) model [11]. In this paper, we will derive the rate of effective particle hit from an empirical model [3].

The hit rate of different particle types, such as alpha particles or neutrons, are available from experiments [2]. The particle hit rate \( R_{PH} \) caused by cosmic ray neutrons, for example, is given by

\[
R_{PH} = \int_{E_{n,\text{min}}}^{E_{n,\text{max}}} F_n(E_n) dE_n \cdot A_t
\]

where \( F_n(E_n) \) is the altitude and location-dependent neutron flux [12] defined between neutron energies \( E_{n,\text{min}} \) and \( E_{n,\text{max}} \), \( A_t \) is the total silicon area of the CCLC. We will derive \( P(SE) \) and \( \alpha \) in sections II-B and III-A, respectively.

\section{Soft Error Probability}

In this section, we define the probability space, over which the probability of soft errors conditioned on an effective particle hit will be estimated. We assume single effective particle hit within a clock period, which results in single event upset (SEU). This assumption is justified by typically small value of particle flux (total neutron flux at sea level is 56.5 m\(^{-2}\)s\(^{-1}\)) [12], small chip area and short clock period. The probability experiment, probability space, and events of interest are defined as follows.

**EXPERIMENT** With reference to Fig. 1, an effective particle hit in a CCLC with \( B \) output DFFs and \( M \) internal circuit nodes have the following outcomes:

1) \( \omega_{hc,p}^{(j)} \): the generated charge \( q \) is collected by \( p \)-type drain of the \( j \)-th circuit node.
2) \( \omega_{hc,n}^{(j)} \): the generated charge \( q \) is collected by \( n \)-type drain of the \( j \)-th circuit node.
3) \( \omega_{ha,p}^{(j)} \): the generated charge \( q \) is collected by \( p \)-type drain of the \( i \)-th DFF sample stage.
4) \( \omega_{ha,n}^{(j)} \): the generated charge \( q \) is collected by \( n \)-type drain of the \( i \)-th DFF sample stage.
5) \( \omega_{hm,p}^{(j)} \): the generated charge is collected by the \( p \)-type drain of the \( i \)-th DFF hold stage.
6) \( \omega_{hm,n}^{(j)} \): the generated charge is collected by the \( n \)-type drain of the \( i \)-th DFF hold stage.
7) \( \omega_{ho} \): the generated charge is not collected by a circuit node, DFF sample stage or hold stage.

where \( j \in \{1, 2, ..., M\} \) and \( i \in \{1, 2, ..., B\} \).

**Definition 2:** The sample space \( \Omega \) is:

\[
\Omega = \left\{ \omega_{hc,p}^{(1)}, \omega_{hc,n}^{(1)}, ..., \omega_{hc,p}^{(M)}, \omega_{hc,n}^{(M)}, \omega_{ha,p}^{(1)}, \omega_{ha,n}^{(1)}, ..., \omega_{ha,p}^{(B)}, \omega_{ha,n}^{(B)}, \omega_{hm,p}^{(1)}, \omega_{hm,n}^{(1)}, ..., \omega_{hm,p}^{(B)}, \omega_{hm,n}^{(B)}, \omega_{ho} \right\}
\]

The triple \( (\Omega, B, P) \) is the probability space, where \( B \) is the corresponding \( p \)-field and \( P \) is a probability measure.

**Definition 3:** The events of interest are:

1) \( SE^{(i)} \): a soft error at the \( i \)-th output bit.
2) \( SE \): a soft error at any output bit; \( SE = \bigcup_{i=1}^{B} SE^{(i)} \).
3) \( HC_{p}^{(j)} \): \( \{ \omega_{hc,p}^{(j)} \} \); \( P(HC_{p}^{(j)}) = \frac{A_{hc}}{{A_t}} \).
4) \( HC_{n}^{(j)} \): \( \{ \omega_{hc,n}^{(j)} \} \); \( P(HC_{n}^{(j)}) = \frac{A_{hc}}{{A_t}} \).
5) \( HS_{p}^{(j)} \): \( \{ \omega_{ha,p}^{(j)} \} \); \( P(HS_{p}^{(j)}) = \frac{A_{ha}}{{A_t}} \).
6) \( HS_{n}^{(j)} \): \( \{ \omega_{ha,n}^{(j)} \} \); \( P(HS_{n}^{(j)}) = \frac{A_{ha}}{{A_t}} \).
7) \( HM_{p}^{(j)} \): \( \{ \omega_{hm,p}^{(j)} \} \); \( P(HM_{p}^{(j)}) = \frac{A_{hm}}{{A_t}} \).
8) \( HM_{n}^{(j)} \): \( \{ \omega_{hm,n}^{(j)} \} \); \( P(HM_{n}^{(j)}) = \frac{A_{hm}}{{A_t}} \).
9) \( HO \): \( \{ \omega_{ho} \} \).

\[
P(HO) = \frac{1}{A_t} \left[ A_t - \sum_{j=1}^{M} (A_{hc}^{(j)} + A_{hc,a}^{(j)}) - \sum_{i=1}^{B} (A_{ha}^{(i)} + A_{ha,a}^{(i)} + A_{hm}^{(i)} + A_{hm,a}^{(i)}) \right]
\]

where \( A_{hc,a}^{(j)}, A_{hc,a}^{(j)}, A_{ha,a}^{(j)}, A_{hm,a}^{(j)} \) and \( A_{hm,a}^{(j)} \) are the sensitive \( p \)- and \( n \)-type drain areas of corresponding circuit nodes, respectively.

Events 1 and 2 are the soft error events of interest and will be further quantified in the succeeding sections. Events 3 to 9 are elemental effective particle hit events. Event 3 and 4 are illustrated in Fig. 1(b). Events 5 to 8 acknowledge the fact that commonly-used master-slave DFFs have two stages: sample and hold, both of which are susceptible to particle hits (see Fig. 1(c)). Event 9 is associated with a particle hit occurring at an irrelevant location, e.g., an empty space on substrate or the source terminal of a transistor connected to supply rail (see Fig. 1(d)). Event 9 does not cause soft errors, i.e., \( P(SE^{(i)}|HO) = 0 \). The charge released by an incoming particle can be collected by a circuit node only if the particle hit occurs within a sensitive area around the node [7], [13]. This property is quantified by the definitions of probabilities of elemental events as shown above. These will be evaluated in section III-A.

The probability of soft error at the \( i \)-th output bit is derived from the principle of total probability as...
Because CMOS gates are uni-directional, we can assume that an effective particle hit at the sample or hold stage of one DFF does not introduce soft errors in another DFF. The above Equation of $P(\text{SE}^{(i)})$ is simplified to

$$P(\text{SE}^{(i)}) = \sum_{j=1}^{M} \left[ P(\text{SE}^{(i)}|\text{HC}_p^{(j)}) P(\text{HC}_p^{(j)}) + P(\text{SE}^{(i)}|\text{HC}_n^{(j)}) P(\text{HC}_n^{(j)}) \right]$$

$$+ \sum_{j=1}^{B} \left[ P(\text{SE}^{(i)}|\text{HS}_p^{(j)}) P(\text{HS}_p^{(j)}) + P(\text{SE}^{(i)}|\text{HS}_n^{(j)}) P(\text{HS}_n^{(j)}) \right]$$

$$+ \sum_{j=1}^{B} \left[ P(\text{SE}^{(i)}|\text{HM}_p^{(j)}) P(\text{HM}_p^{(j)}) + P(\text{SE}^{(i)}|\text{HM}_n^{(j)}) P(\text{HM}_n^{(j)}) \right]$$

Fan-outs from a particular gate, as illustrated in Fig. 1 (b), make it possible for one effective particle hit event to cause soft errors at more than one output bit and hence the following inequality holds:

$$\max \left\{ P(\text{SE}^{(i)}) \right\} \leq P(\text{SE}) \leq \sum_{i=1}^{N} P(\text{SE}^{(i)})$$

(5)

III. SOFT ERROR RATE ANALYSIS

In this section, we develop the framework of SERA for complex combinational circuits. We first describe the methodology and extract important model parameters in section III-A. The conditional probabilities appearing in (4) are extracted from an inverter chain circuit via circuit simulations in section III-B. In section III-C, these results are utilized together with graph theory and fault simulation to analyze the SER of complex combinational circuits.

A. Methodology

The quantities defined in (3) and (1) can be extracted from cosmic ray data [2], [12] and chip layout. In this section, we describe the methodology to obtain the conditional probabilities appearing in (4).

The impact of an effective cosmic ray neutron hit on a circuit node is modeled by a time-dependent pulse current source at a drain node [14]:

$$I(q,t_{PH})(t) = \begin{cases} 
0 & t < t_{PH} \\
\pm \frac{2q}{\tau} \sqrt{1 - \frac{t_{PH}}{t}} e^{-\frac{t}{\tau}} & t \geq t_{PH}
\end{cases}$$

(6)

where $q$ is the amount of collected charge, $t_{PH}$ is the time instant at which a particle hits the node, and $\tau$ is a process technology-dependent time constant [3]. Note that the polarity of the current source is determined by whether the charge is collected by a p or n-type drain, as a drain node can collect only the minority carriers from the substrate or a well [15]. A particle hit occurring at a p-type drain would, for example, induce a current pulse with negative sign in (6), which means positive charge is being injected to the node and the voltage may increase momentarily as a result.

The conditional probabilities in (4) can be determined by applying the current waveform in (6) to various nodes of the circuit in Fig. 1(a). The polarity of the current source together with the logic state of victim node determines whether the logic state is corrupted. If, for example, the logic value of a node is 1 and the current source attached to that node has positive polarity due to a particle hit at a n-type drain, a 1-0-1 SET may occur. On the other hand, a particle hit at a p-type drain will only reinforce the logic state 1. The outputs of DFFs are observed to determine whether the SET will be captured. The sampling clock edge arrival time $t_{ce}$ is defined relative to the instant a particle hit occurs which is assumed to be at time 0 for convenience (see Fig. 2). Three conditions must be satisfied for a soft error to occur: 1.) logical masking must not occur, 2.) SET pulse arriving at DFF input B must encompass the DFF latching window, 3.) pulse amplitude at DFF input must be large enough.

Condition 1 is illustrated in Fig. 2(a). Condition 2 is satisfied if the pulse delay $t_{d}$ is close to $t_{ce}$ and if the pulse duration $t_{p}$ is greater than the sum of DFF setup time $t_{set}$ and hold time $t_{h}$, as illustrated in Fig. 2(b). Attenuation of a noise pulse when it propagates through cascading gates may cause the violation of condition 3. Note that the above three conditions are only qualitative explanations. The proposed methodology accurately models all these effects.

The expressions of conditional probabilities corresponding to effective particle hits at p-type drains are given by (those at n-type drains are similar):

$$P(\text{SE}^{(i)}|\text{HC}_p^{(j)}) = \int_{(q,t_{ce}) \in S_{q,t_{ce}}^{(j)}} f_{Q}(q) f_{T}(t_{ce}) dt_{ce} dq$$

(7)

$$P(\text{SE}^{(i)}|\text{HS}_p^{(j)}) = \int_{(q,t_{ce}) \in S_{q,t_{ce}}^{(j)}} f_{Q}(q) f_{T}(t_{ce}) dt_{ce} dq$$

(8)

$$P(\text{SE}^{(i)}|\text{HM}_p^{(j)}) = \int_{q=0}^{\infty} f_{Q}(q) dq$$

(9)

where $S_{q,t_{ce}}^{(j)}$ and $S_{q,t_{ce}}^{(j)}$ are sets of soft-error-inducing $(q,t_{ce})$ combinations corresponding to effective particle hits at the p-type drain of jth internal circuit node and jth DFF sample stage, respectively. The parameter $Q_{crit,m,p}$ is the critical charge for the jth DFF hold stage, if the effective particle hit occurs at the p-type drain. The functions $f_{Q}(q)$ and $f_{T}(t_{ce})$ are the probability density functions (PDF) of collected charge and sampling clock edge arrival time, respectively.

Because a particle hit is independent of the clock edge arrival, we assume $f_{T}(t_{ce})$ to be a uniform distribution in the range $[0, T_{clk}]$, where $T_{clk}$ is the clock period. We show next that $f_{Q}(q)$ is an exponential distribution.

The hold stage of a DFF is similar to a 6-T SRAM cell and can be characterized with a single critical charge value $Q_{crit}$ [16]. Its soft error rate is derived from (2), (3), (4), (9) and the equations in Definition 3 as shown below:
the value of \( q \) and \( t_{co} \) as illustrated previously in Fig. 2. We choose equally-spaced data points in the set \( \Lambda \) defined as

\[
\Lambda = [0, Q_{\text{max}}] \times [0, T_{\text{clk}}]
\]

with step sizes of \( \Delta q \) and \( \Delta t \), respectively.

For every particle hit location, a flag function \( F(q, t_{co}) \), defined to equal one when there is a soft error and zero when no error occurs, is obtained from HSPICE simulations. The discretization of (7)-(9) as applied to the inverter chain circuit results in:

\[
P(\text{SE}|\text{HC}_p^{(j)}) = \sum_{(q, t_{co}) \in \Lambda} f(q) \Delta q f_T(t_{co}) \Delta t_{co} F_{\text{HC}_p^{(j)}}(q, t_{co})
\]

\[
P(\text{SE}|\text{HS}_p) = \sum_{(q, t_{co}) \in \Lambda} f(q) \Delta q f_T(t_{co}) \Delta t_{co} F_{\text{HS}_p}(q, t_{co})
\]

\[
P(\text{SE}|\text{HM}_p) = \begin{cases} \sum_{q=Q_{\text{crit}}}^{Q_{\text{max}}} f(q) \Delta q, & Q_{\text{crit}} < Q_{\text{max}} \\ 0, & Q_{\text{crit}} \geq Q_{\text{max}} \end{cases}
\]

where a finite value \( Q_{\text{max}} \) is used as the upper limit in the summation in (20). This reduces the simulation run times. The error caused by this approximation is less than 2% if \( Q_{\text{max}} = 4Q_s \) due to the exponential distribution in (16).

The conditional probabilities in (18) - (20) and those corresponding to particle hits at n-type drains (similarly derived) are evaluated in a TSMC 0.18 \( \mu \)m technology. In order to save space, we only show the average of conditionals corresponding to p and n-type drains (denoted with effective particle hit events without a subscript) in Fig. 4. Note that these two types of conditionals will be used separately in section III-C while analyzing the SER for complex combinational circuits.

As shown in Fig. 4(a), the conditionals are non-monotonic functions of clock period \( T_{\text{clk}} \). The conditionals are zero when \( T_{\text{clk}} \) is small because the uniformly distributed sampling clock edge always arrives before the SET arrival at the DFF input. The conditionals start to increase when \( T_{\text{clk}} \) is large enough such that the propagated SET starts to encompass the DFF latching window (see Fig. 2(b)). The curves in Fig. 4(a) peak when \( T_{\text{clk}} \) is approximately equal to the pulse delay \( t_{dd} \). The conditionals drop when \( T_{\text{clk}} \) becomes so large that the fraction of clock edges arriving later than the SET arrival keeps increasing with \( T_{\text{clk}} \). In 0.18 \( \mu \)m process, the conditional probability \( P(\text{SE}|\text{HM}) \) is at least two times greater than the other conditionals. The other conditionals though small have significant impact on the overall SER because a logic circuit usually has many more combinational circuit nodes than memory nodes (DFF hold stages). It is also observed that \( P(\text{SE}|\text{HC}^{(j)}) > P(\text{SE}|\text{HC}^{(i)}) \) if \( j < i \). This is due to the attenuation of SET in both amplitude and duration when it propagates through the inverter chain.

Fig. 4(b) shows an increasing DFF latching window duration \( (t_{\text{set}} + t_{\text{th}}) \) results in a reduction of conditional soft error probabilities. This is because a master-slave DFF with wider latching window is less sensitive to fast-switching SETs. Other DFF styles, such as those with a semidynamic frontend, can be used in this simulation setup as well to obtain the corresponding conditional probabilities. Fig. 4(c) shows that different conditionals vary differently with supply voltage \( V_{dd} \). The conditionals \( P(\text{SE}|\text{HS}), P(\text{SE}|\text{HC}^{(1)}) \) and \( P(\text{SE}|\text{HC}^{(2)}) \) decrease with \( V_{dd} \) because the SET generation mechanism, which dominates for nodes closer to the DFF, becomes weaker at higher \( V_{dd} \) due to stronger active pull-up or pull-down path in the gates. The conditionals \( P(\text{SE}|\text{HC}^{(3)}) \) and \( P(\text{SE}|\text{HC}^{(5)}) \) increase with \( V_{dd} \) because the delay between SET generation and SET arrival at DFF...
input plays a dominant role for nodes farther away from the DFF. The delay decreases as \( V_{dd} \) increases and hence it is more likely for the pulse to get latched. The conditional \( P(SE|HC) \) happens to sit in the transition region between two regimes and is non-monotonic.

**C. SERA for Combinational Circuits**

The procedure of SERA for combinational circuits is illustrated by the flow chart in Fig. 5. We decompose a circuit into a collection of circuit nodes with a gate between each pair of nodes. The gate is modeled as an equivalent inverter. This results in multiple inverter chains and thus the results in the previous section can be employed. For accuracy, three new factors are accounted for: 1) transistor sizing and multiple fan-ins are reflected by changing the size of equivalent inverter, 2) extra load due to fan-outs is modeled by adding a capacitor to the output of each inverter, 3) logical masking is emulated.

Steps (i) in the flow chart converts a gate-level netlist to a graph where vertices and edges correspond to internal circuit nodes and gates, respectively. A path length denotes the number of gates between two nodes. This step only needs to be done once for a given circuit. Note that the gate-level netlist also contains transistor sizing information so that an equivalent inverter chain can be extracted to obtain soft error probabilities on a path. User-provided or randomly-generated input vectors are used in step (ii), making an effort to average out variations in SER for different input vectors. Logical masking mechanism is accounted for in steps (iii) and (iv). The logic values of all vertices are first computed based on the input vectors. For every vertex, its logic value is temporarily flipped to see whether the value can propagate through an edge to an adjacent vertex. The adjacency list representation of the circuit is then updated to emulate the logical masking mechanism. In step (v), a path-search algorithm finds all paths between a given pair of primary output bit and internal circuit node. The length of each path is also recorded. If multiple paths exist between a pair of nodes (reconvergent fan-out), circuit simulation shows that the noise pulse generated by a particle hit can propagate along various paths and arrive at DFF input at different instants with none or little overlapping due to different path delays. Hence the following approximation holds for the soft error probability at \( i^{th} \) primary output bit conditioned on a particle hit at \( j^{th} \) internal circuit node (see an illustration in Fig. 6):

\[
P(SE_{i}^{(j)}|HC_{i}^{(j)}) \approx \left\{ \begin{array}{ll}
\min \left( 1, \sum_{k=1}^{N_{i,j}} P(L_{i,j,k}^{k}) \right) & , V(j) = 0 \\
0 & , V(j) = 1
\end{array} \right. 
\]  \hspace{1cm} (21)

\[
P(SE_{i}^{(j)}|HC_{n}^{(j)}) \approx \left\{ \begin{array}{ll}
\min \left( 1, \sum_{k=1}^{N_{i,j}} P(L_{i,j,k}^{n}) \right) & , V(j) = 0 \\
0 & , V(j) = 1
\end{array} \right. 
\]  \hspace{1cm} (22)

where \( V(j) \) is the logic value of node \( j \), \( N_{i,j} \) is the number of unique path lengths between the \( j^{th} \) internal circuit node and the \( i^{th} \) primary output bit, \( L_{i,j,k}^{p} \) is the \( k \)-th path length corresponding to a particle hit at p-type drain, \( L_{i,j,k}^{n} \) is the \( k \)-th path length corresponding to a particle hit at n-type drain, and \( P(L_{i,j,k}^{p}) \) or \( P(L_{i,j,k}^{n}) \) is the corresponding conditional soft error probability for the inverter chain circuit shown previously in Fig. 3. Note that only paths with unique lengths are accounted for. This approximation results in a slight overestimation of the conditional probabilities since the propagation of a noise pulse along two paths with the same length may weaken, if not cancel, each other. We show in section IV-A that this approximation does not result in significant degradation in estimation accuracy for most circuits.

Substituting (4) and equations from Definition 3 in (2) yields the soft error probability and hence SER of the \( i^{th} \) bit:

\[
SER^{(i)} = F \cdot \alpha \left[ \sum_{j=1}^{M} \left( P(SE_{i}^{(j)}|HC_{p}^{(j)}) \cdot A_{i,p}^{(j)} + P(SE_{i}^{(j)}|HC_{n}^{(j)}) \cdot A_{i,n}^{(j)} \right) + P(SE_{i}^{(j)}|HS_{p}^{(j)}) \cdot A_{i,p}^{(j)} + P(SE_{i}^{(j)}|HS_{n}^{(j)}) \cdot A_{i,n}^{(j)} + P(SE_{i}^{(j)}|HM_{p}^{(j)}) \cdot A_{i,p}^{(j)} + P(SE_{i}^{(j)}|HM_{n}^{(j)}) \cdot A_{i,n}^{(j)} \right]
\]  \hspace{1cm} (23)

where the conditionals \( P(SE_{i}^{(j)}|HC_{p}^{(j)}) \) and \( P(SE_{i}^{(j)}|HC_{n}^{(j)}) \) are calculated from (21)–(22), and the other conditional terms from (19)–(20).

**IV. RESULTS**

In this section, we compare the results of SERA with those of empirical model and Monte Carlo simulation. We show that SERA
achieves excellent accuracy with orders of magnitude reduction in run times. We show the effect of logical masking and input vector value on SER of combinational logic circuits. We also present the estimated SER for multipliers of various size as an example. The dependence of SER on supply voltage and DFF latching window is explicitly shown.

A. Comparison with Empirical Model and Monte Carlo Simulations

To our best knowledge, empirical SER data for combinational circuits is not available in open literature. Therefore, we validate the proposed SERA methodology by a two-step approach. We first compare the results from SERA with existing empirical SER data for SRAMs [3], [15], knowing that an SRAM cell is nothing but a special case of CCLC. Study of SER as a function of supply voltage for 6-T SRAM cells in 0.35 μm and 0.6 μm processes shows consistent results. The worst case difference is 8% and can be well attributed to the difference in process parameters.

Secondly, we propose to use Monte Carlo circuit simulations to verify the SER of a few small test circuits predicted by SERA. The number of simulated random events required in a Monte Carlo simulation for statistically significant predictions of SER depends inversely on the actual error rate. For example, if the failure rate expected from simulation is $10^{-16}$ errors/sec, which is a typical SER value for a single SRAM cell [3], of the order of $10^{17}$ simulated events would be appropriate to achieve statistical significance. Evidently, the huge sample sizes typically needed in SER Monte Carlo simulation preclude the direct use of a nuclear interaction or semiconductor device simulation program. As shown in Fig. 7, we propose a methodology to run Monte Carlo simulations using HSPICE. A data set is generated pseudo-randomly, each entry of which is composed of input vectors, particle hit location and pulse current source parameters. This data set is then provided to HSPICE to perform data-driven transient simulations.

We conducted comparisons on a Dell Precision Workstation 650n (with Intel Xeon 2.8GHz CPU and 1GB RAM) running Redhat Linux. Table I shows the run times of SERA ($t_{SERA}$) and one million Monte Carlo simulations ($t_{MC}$), as well as the difference between their SER results ($\Delta SER$) and run time speed-up. We observe excellent matching (less than 4% difference) with 90000X - 180000X speed-up for three small circuits with 5, 8, and 11 gates, respectively. The total run time of Monte Carlo circuit simulation grows so rapidly with the number of gates that it is impractical to simulate a 4 x 4 multiplier. SERA, on the other hand, can analyze large circuits as is evident from Table I.

B. Multiplier SER

We present the SER of multipliers as predicted by SERA. At sea level (New York City), the total neutron flux $F$ is $56.5 \text{ m}^{-2} \text{s}^{-1}$ (see [12]). The sea level SER in unit of FIT (Failure-In-Time) is defined as the number of errors in $10^9$ hours. As stated earlier, the SER of combinational circuits is a function of the input vector value, because the logical masking mechanism changes with input. Fig. 8 shows the importance of taking logical masking into account. Ignoring logical masking would have resulted in an unreasonable over-estimation of SER, especially for the MSBs. Fig. 9 shows the variation of SER with input vector values. SER values for the center bits tend to spread...
more than the LSBs and MSBs, because logical masking mechanism varies more with input vector values due to the large number of paths leading to those bits.

The SER averaged over 10000 input vector values are shown for individual bits of parallel carry-save array multipliers of various sizes under nominal supply voltage and clock frequency in Fig. 10. Two factors influence the SER for an output bit: 1.) the number of paths between the output bit and any internal circuit node, and 2.) logical masking. The former dominates for LSBs while the latter dominates for MSBs. This results in the peaking of individual bit SER at a bit position roughly two thirds of the full output precision away from the LSB. Fig. 11 shows the fraction of SER contributed by DFF memory element for multipliers of various sizes. As the size of multiplier increases, less and less SER is contributed by DFF memory element.

Both upper and lower bounds on the overall SER are calculated from (2) and (5) as follows:

\[
\max_i \text{SER}^{(i)} \leq \text{SER} \leq \sum_{i=1}^B \text{SER}^{(i)}
\]

where \(B\) is the number of output bits. We use these bounds for plotting convenience. The results are compared with SRAMs of various sizes in Fig. 12. The SER lower bound of a 32 x 32 multiplier is close to the SER of a 1 kb SRAM in the same technology while its upper bound is close to SER of a 10 kb SRAM. The SER of a 32 x 32 multiplier is further plotted as a function of supply voltage \(V_{DD}\) and DFF latching window \(t_{set} + t_h\) in Fig. 13. For simplicity, only the SER upper bound is plotted. A wider latching window can very effectively decrease the error latching probability (see Fig. 4(b)) and hence the soft error rate. The \(P(\text{SE}|\text{HM})\) terms do not depend on latching window and start to dominate after \(t_{set} + t_h\) is greater than roughly 120 ps so the reduction in SER thereafter becomes negligible. On the other hand, higher \(V_{DD}\) does result in a slight reduction of SER. This weak dependence of SER on \(V_{DD}\) is because the conditional probabilities are relatively weak functions of \(V_{DD}\) (see Fig. 4(c)). In fact, the SER increases by more than 50X when \(t_{set} + t_h\) is decreased by 20% from 120 ps while it increases by only 28% when \(V_{DD}\) is decreased by 20% from 1.8 V.

V. CONCLUSIONS

We propose a SER analysis methodology, referred to as SERA, that achieves five orders of magnitude speed-up over Monte Carlo based approaches with less than 5% error. The proposed methodology also points to several design guidelines for introducing soft error-tolerance in logic circuits, such as supply voltage tapering, increasing logic depth and DFF setup time. Research in the area of CAD of soft-error tolerant circuits and systems is wide open. For example, future work can focus on evaluating the impact of circuit style and technology scaling on SER as well as characterization of SER of various arithmetic units so that soft-error tolerant architectures and algorithms can be designed.
Fig. 11. The contribution of SER from DFF memory element at individual bit positions for multipliers of various sizes: (a) $4 \times 4$, (b) $8 \times 8$, (c) $16 \times 16$, and (d) $32 \times 32$.

Fig. 12. Comparison between overall SERs of multipliers and SRAMs.

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