Digital Background Gain Error Correction in Pipeline ADCs

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Abstract

This paper presents a new digital technique for background calibration of gain errors in Pipeline ADCs. The proposed algorithm estimates and corrects both the MDAC gain error of the stage under calibration and the global gain error associated to the uncalibrated stages without interruption of the conversion and without reduction of the dynamic rate. It is based on the use of a stage with two input-output characteristics, depending on the value of a digital noise signal.

Key Words: Analog-to-Digital Converter, Pipeline ADC, Background Calibration, On-line Calibration.

1. Introduction

High-speed high resolution for communications needs high performance of the analogue blocks in data converters as well as self-correction/self-calibrating techniques. In the particular case of Pipeline ADCs, correction techniques can improve the linearity of sub-ADCs dealing with the transition errors, but for resolution greater than 10 bits, a calibration technique is necessary. Moreover, even for lower resolutions calibration can relax the analogue block specification. This aspect is of particular interest in current high-speed high resolution ADC converters due to the existing constrains between gain and bandwidth of amplifiers. Thus, one possibility to improve the performance of the converter is to relax the gain specification and increase the bandwidth, correcting the errors associated to the limited gain with a calibration scheme.

Any calibration method requires two operations: error measurements and calibration codes calculation. There exist foreground calibration techniques that need the interruption of the normal converter operation to start a calibration cycle. Normally, the error measurements are obtained just after power is turned on. Thus, any miscalibration, environmental change such as temperature, power supply or component aging cannot be overcome if the system works continuously. However, background calibrations deal with these performing error measurements during the ADC operation.

We can distinguish two different approaches for background calibration. *Virtual-background techniques* where error measurements are performed during the normal operation, but the calibration codes are still calculated in a foreground mode. They need an extra circuitry to realise the operation of the stage under calibration [1-2], or they are based on creating artificial time slots for calibration purpose [3-5]. In contrast, *true background calibration techniques* [6-11] follow a completely different approach using the conversion results for calibration.

Some *true background calibrations* use a noise calibration signal together with the normal input, to allow background calibration [6,10]. One disadvantage of these techniques is the reduction of dynamic range because part of the input full scale is used by the calibration signal. This limitation has been solved at least for Interleaved ADCs using a chopper offset cancellation technique, in combination with a digital filter scheme, increasing drastically the complexity of the system [11].

In this paper, a new digital *true background* calibration method for Pipeline ADCs without reduction of the dynamic rate is presented. The algorithm uses a stage with two different input-output characteristics to correct both the MDAC gain error of the stage under calibration and the global gain error associated to the uncalibrated stages, without interruption of the conversion and without reduction of the dynamic rate. The two stage transfer characteristics are controlled by a digital pseudorandom noise signal $N[i]$.

2. Two-residue Stage

Figure 1 shows a simplified scheme of the two-residue stage. It is constituted by a sub-ADC and a Multiplying-DAC (MDAC). The sub-ADC converts its analogue input signal x to a digital code c_n, according to its resolution r always less than the final resolution r_T,

$$c_n \in [-2^{r-1}, 2^{r-1} - 1] \quad (1)$$

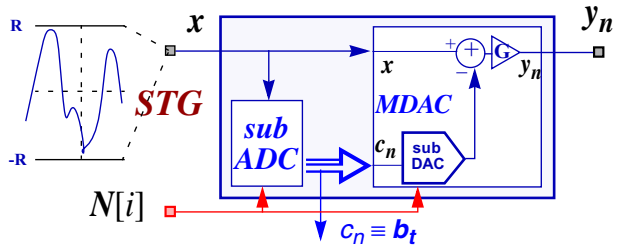

Fig. 1 New two-residue stage

This code is transformed to an analogue representation by the digital to analogue converter (sub-DAC) inside the MDAC block, and it is subtracted from the input signal. Then, the residue y_n is adapted to the next stage using the interstage amplifier G. The additional input $N[i]$ is the noise signal controlling the two possible configurations of the stage. If $N[i] = -1$, the MDAC's residue is shown in Fig. 2a, if $N[i] = 1$ an offset of half a stage-LSB is introduced as is depicted in Fig. 2b.

If a digital correction scheme with unity redundancy is considered, the nominal inter-stage gain of the MDAC is defined as $G = 2^{r-1}$.

An analysis of the static behaviour of a typical Switched-Capacitor MDAC implementation, allow us to model the amplified residue as a function of the analogue input x, [12],

$$y_n = G(1+e)(x - \tilde{p}_{c_n}) + G\gamma \cdot x + \lambda(c_n) + G\xi_n \cdot N + v_{off} \quad (2)$$

where the function $\tilde{p}_{c_n}$, given by (3), is defined as the potency of the MDAC (see Fig. 2). This magnitude depends on the offset control parameter δ_n,

$$\tilde{p}_{c_n} = qc_n + \delta_n \cdot q \qquad ; \qquad q = 2R/2^r \quad (3)$$

$$\delta_n = \frac{3}{4} + \frac{1}{4} \cdot N[i] \quad (4)$$

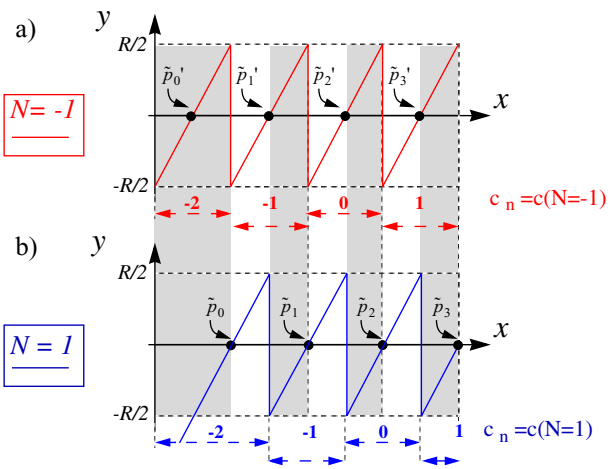

Fig. 2 Stage transfer characteristics (r = 2)

Equation (2) explicitly shows the dependence of the residue on the MDAC error sources. Its parameters are,

e : interstage gain error
γ : input direct path gain error
$\lambda(c_n)$: non-linear errors depending on the sub-code c_n
ξ_n : direct path gain error due to signal $N[i]$
v_{off} : MDAC's offset

Obviously, an offset in the references for the sub-ADC, as a function of the noise signal $N[i]$, must be introduced as is depicted in Fig. 2.

3. Background Calibration Algorithm

Let us consider for simplicity that only the first stage of a Pipeline ADC is going to be calibrated (see Fig. 3 for terms definitions). The back-end stages can be modelled as a converter (ADC_2) with gain and offset errors: α_2 and β_2 respectively. In this conditions, the ADC_2 output code Z_{2n} approximately becomes,

$$Z_{2n} \approx (\alpha_2 y_{2n} + \beta_2)/q_2 \quad (5)$$

Taking into account equations (2) to (5), Z_{2n} can be expressed as a function of the analogue input x,

$$Z_{2n} \approx G_1(1+e_1)\frac{\alpha_2}{q_2} \cdot [x - q_1 c_{1n} - q_1 \delta_{1n}] + \ldots$$
$$\frac{\alpha_2}{q_2} \cdot [G_1\gamma_1 x + \lambda(c_{1n}) + G_1\xi_{1n} \cdot N + v_{off\,1}] + \frac{\beta_2}{q_2} \quad (6)$$

In this equation, we can distinguish three different contributions: a) the ideal subcode $Z_{2n}^* \approx G_1(x - \tilde{p}_{c_n})/q_2$ affected by a gain error $(1+e_1)\alpha_2$; b) an offset term β_2/q_2; c) the rest of terms in (6) depending on the noise signal and the analogue input $D(N, x)$. Hence, (6) can be rewrited as,

$$Z_{2n} \approx (1+e_1)\alpha_2 \cdot Z_{2n}^* + D(N, x) + \beta_2/q_2 \quad (7)$$

A final gain-calibrated output code of the pipeline ADC Z_{cal} can be obtained removing the factor $(1+e_1)\alpha_2$ from Z_{2n} and considering an offset correction code $tcor_n$ that compensates the displacement of the transfer characteristic, as (8) and (9) show. Contribution of $D(N, x)$ will be considered in this work as a second order error.

$$Z_{cal} = c_{1n}2^{(r_2-1)} + Z_{2cal} \quad (8)$$

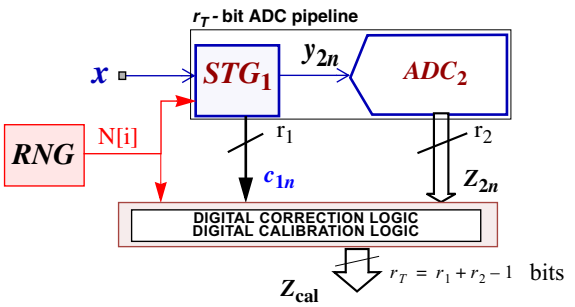

Fig. 3 Simplified Pipeline ADC schematic

$$Z_{2cal} = Z_{2n}/[(1+e_1)\alpha_2] - tcor_n$$
$$tcor_n = -\delta_{1n} \cdot 2^{r_2-1} \quad (9)$$

The residual offset that corresponds to the multiplicative factor on the final term β_2/q_2 does not introduce any distortion, only a global offset.

Let us probe that the mean value of signal σ_2, defined by (10), can produce the magnitude necessary to calibrate the gain errors of Z_{2n}^* under some conditions. In this analysis, we must take into account that in (6) there are one term that depends directly on the signal $N[i]$ (dependence on term ξ_{1n} is considered as second order term) and two terms that depend indirectly on the noise signal, as a function of c_{In} and $\lambda(c_{1n})$.

$$\sigma_2 = Z_{2n} \cdot N[i] \quad (10)$$

If x and $N[i]$ are not correlated, and remembering that $N[i]$ has a zero mean value, the mean value of σ_2 becomes,

$$\overline{\sigma_2} \approx G_1(1+e_1)\frac{\alpha_2}{q_2} \cdot \left[-q_1\overline{c_{1n}N[i]} - \frac{1}{4}q_1\right] + \frac{\alpha_2}{q_2} \cdot \overline{N[i]\lambda(c_{1n})} \quad (11)$$

Equation (11) still maintains a dependence on the noise signal that is going to be studied in Sec. 3.1.

3.1. Sub-code c_{In}. Dependence on $N[i]$

Firstly, we will consider the analogue input x constrained to the *shadow* area in the 2-bit example of Fig. 2, then the sub-code c_{In} is constant in each region.

Let us introduce the digital signal $K[i]$, called *Zone Factor*, whose value is respectively fixed to 1 or -1 depending on if the input signal is constrained into the *shadow* or *light* areas in Fig. 2. Mathematically, this function can be defined considering the sign of Z_{2n} and the value of $N[i]$. In this situation,

$$c_{1n} = c_1 \quad ; \quad K[i] = 1 \quad (12)$$

where c_1 is the sub-code when $N[i] = 1$.

Taking into account (12), the noise component in (11) is averaged to zero.

$$\overline{\sigma_2(K=1)} \approx -G_1(1+e_1)\frac{\alpha_2}{q_2} \cdot \frac{1}{4}q_1 \quad (13)$$

And considering the value of G_1 and q_2, this expression can be simplified as,

$$\overline{\sigma_2(K=1)} \approx -\frac{W}{Z_\alpha} \quad ; \quad W = 2^{r_2-3} \quad (14)$$

where,

$$Z_\alpha = 1/[(1+e_1)\alpha_2] \quad (15)$$

Equation (15) has information about the gain error in both STG_1 and ADC_2. Therefore, a calibration method can be obtained if the output code Z_{2n} of the back-end stages is multiplied by Z_α.

Now, let us consider that the sub-code c_{1n} depends on the signal $N[i]$. In this case, the input x is constrained to the *light* area in the example of Fig. 2 and the sub-code c_{1n} produces two digital outputs in each region. However, there is a relationship between these possible outputs as (16) shows,

$$\left.\begin{array}{ll} N = 1 & c_{1n} = c_1 \\ N = -1 & c_{1n} = c_1 + 1 \end{array}\right\} \quad ; \quad K[i] = -1 \quad (16)$$

Taking into account (16), the noise component in (11) can be evaluated,

$$\overline{c_{1n} \cdot N[i]} = -\frac{1}{2}$$
$$\overline{N[i] \cdot \lambda(c_{1n})} = \frac{1}{2} \cdot [\lambda(c_1) - \lambda(c_1+1)] \quad (17)$$

If non-linear errors in the MDAC are small, contribution of $\overline{N[n] \cdot \lambda(c_{1n})}$ can be ignored, and (11) can be rewritten as,

$$\overline{\sigma_2(K=-1)} \approx \frac{W}{Z_\alpha} \approx -\overline{\sigma_2(K=1)} \quad (18)$$

We have found, excepting for a minus sign, the same relationship between the parameter Z_α and $\overline{\sigma_2}$ for both situations. Notice, that the imposed constrain in $\overline{N[i] \cdot \lambda(c_{1n})}$ does not reduce the applicability of the calibration technique because in the case it does not apply, the samples when $K[i] = -1$ could not be considered.

3.2. Digital Implementation

Two different implementations of the algorithm are presented in this section.

Indirect Method

Figure 4 shows a schematic representation for an *Indirect Implementation*. The mean value of the signal σ_2 is estimated by the *Averaging Logic*. Herein, a new definition of σ_2 has been introduced to take into account the sign difference between (14) and (18) and to maintain its expected value during the complete range.

$$\sigma_2 = Z_{2n} \cdot N[i] \cdot K[i] \quad (19)$$

If there is convergence, the *Averaging Logic* drives the output of the accumulator σ_{2mean} to $\overline{\sigma_2}$. This block only uses an accumulator and a subtractor if the step parameter μ is a factor of 2. A similar technique has been used to calibrate offset mismatch between channels in interleaved ADC [11].

The output code of ADC_2, Z_{2n}, is digitally divided by a scale factor of $\overline{\sigma_2}$ to obtain Z_{2g},

$$Z_{2g} \approx G_1 \cdot \frac{1}{q_2} \cdot [x - q_1c_{1n} - q_1\delta_{1n}] + \frac{1}{q_2 \cdot (1+e_1)} \cdot \ldots$$
$$[G_1\gamma_1 x + \lambda(c_{1n}) + G_1\xi_{1n} \cdot N + v_{off1}] + \frac{\beta_2}{q_2\alpha_2(1+e_1)} \quad (20)$$

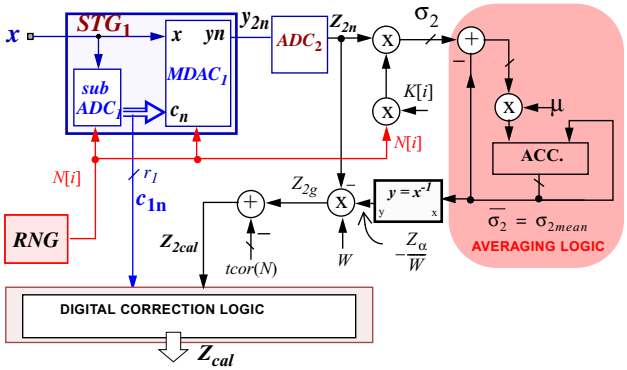

Fig. 4 Calibration System (Indirect implementation)

Finally, to produce the calibrated output Z_{2cal} the offset correction term $tcor_n$ defined in (9) is subtracted as a function of $N[i]$.

Direct Method

The main disadvantage of the above approach is that a digital divider must be implemented with the consequent increment in hardware resources. Other possibility, more interesting, is to perform both averaging and division in a single step using only one digital multiplier.

Figure 5 shows how the estimation and multiplication of Z_α is directly performed from the output code Z_{2n}. A similar implementation of this averaging loop has been reported to correct gain mismatch between channels in interleaved ADC [10].

The algorithm of the averaging logic in Fig. 5 is given respectively by,

$$\begin{aligned} Z_\alpha[i+1] &= Z_\alpha[i] + Z_{2int}[i] \\ Z_{2int}[i] &= \mu \cdot Z_\alpha[i] \cdot \sigma_2[i] + \mu \cdot W \cdot N^2[i] \cdot K^2[i] \end{aligned} \tag{21}$$

If the averaging process is convergent, the accumulator drives $\overline{Z_{2int}}$ to zero, and then in the stationary situation,

$$\overline{Z_\alpha} \approx -W/\overline{\sigma_2} \tag{22}$$

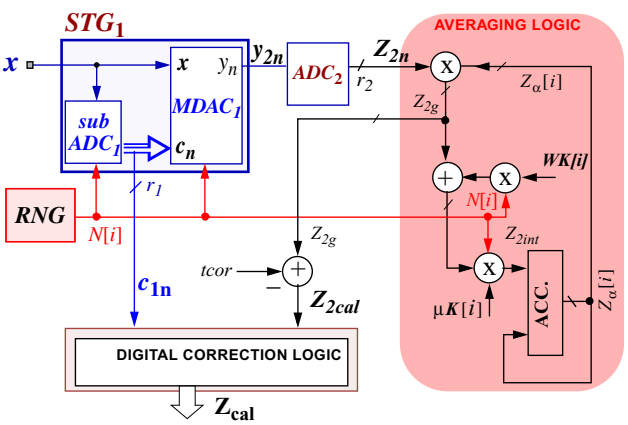

Fig. 5 Calibration System (Direct implementation)

that is exactly the calibration term that was obtained in (14), probing the validity of the developed calibration algorithm.

Thus, after the multiplication by Z_α, it is only needed to include the term $tcor_n$ to suppress the dependence of sub-code c_{1n} on $N[i]$.

4. Simulation Results

In this section, the simulation results of the calibration system are presented. To simplify the analysis, we have considered an ideal sub-ADC. A linear 10-bit converter without offset will play the roll of the ADC_2.

Figures 6a shows simulation results obtained with the *Direct* and *Indirect* methods. The transient evolution of parameter Z_α, as well as the ENOB, are depicted until the algorithm convergence seems to be achieved. The dynamic parameters have been calculated using a sinusoidal input (1024 samples) of amplitude $1.4V_{pp}$ and frequency 0.3 times the sampling frequency f_s, for each step in the calibration (frozen Z_α signal). Notice that both implementations achieve almost the same final performance. In simulations, the algorithm step parameters μ_{dir} and μ_{ind}, for the direct and indirect methods, were respectively fixed to 2^{-28} and 2^{-21}. We have supposed a total gain error of 20% and a reference voltage R of 1V.

If the gain errors are not very big, a simple realisation of the divider in the *Indirect Method* can be implemented. According to Fig. 4 the signal Z_{2g} can be approximated by the second term in (23), where the divider has been suppressed,

$$Z_{2g} = -Z_2 \cdot (W/\overline{\sigma_2}) \approx Z_2 \cdot (\overline{\sigma_2}/W + 2) \tag{23}$$

Figures 6b shows a comparison between two implementations (with the divider and with the above approximation) of the indirect algorithm using the same parameters as in the previous simulation. In this case, a total gain error of 5% has been considered.

5. Non-ideal Effects in Sub-ADCs and Back-end Stages

In the last section, the theoretical analysis has been performed in a general case, with the only exception assumed in (2), i.e., there are not non-linear errors in sub-ADC_1. In addition, some non-ideal effects will affect the generation of the signal $K[i]$. These issues are discussed in details in the following sub-sections, using the example of Fig. 3 as case of study to simplify the description.

5.1. Offset Errors in Back-end Stages

When a non-zero offset is considered in the model (5) and none calibration is applied, no additional distortion appears because an offset in ADC_2 is directly translated to an offset in the complete ADC. However, in the proposed

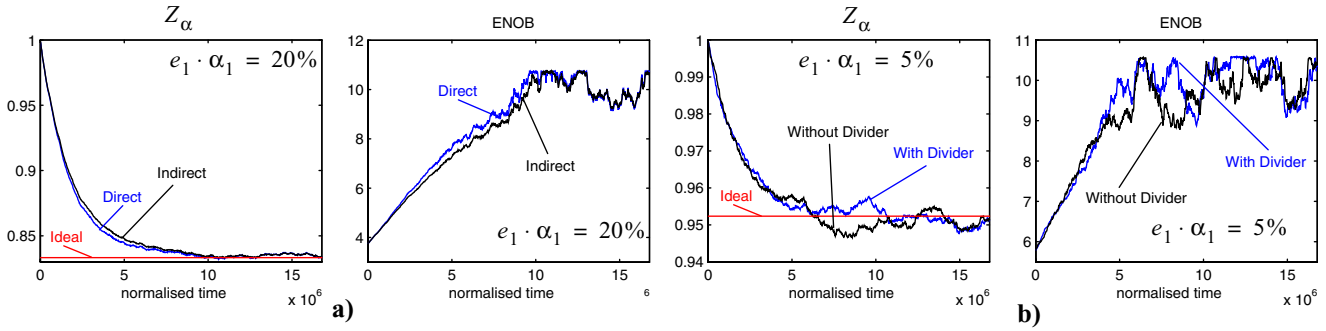

Fig. 6 Simulation Results: a) Direct vs. Indirect Implementations, b) Divider Simplification

background system, distortion appears due to the incorrect definitions of the *shadow-light* areas of Fig. 2. From the mean value of σ_2 with the complete model (5), we verify that the dependence on the offset β_2 is in the *Zone Factor* $K[i]$. The dependence of the new expected value on the *shadow-light* areas generates a non-linear relationship between Z_{2cal} and the input x. The compensation of the offset effects can be realised by: a) calibration, to suppress its effect in the model (5), or b) modification of the *Zone Factor* $K[i]$ definition to assure that the expected value of σ_2 is maintained constants for the complete range of the signal. Both compensation approaches have been studied. Some solutions are described below.

Offset Calibration

One of the explored possibilities is to use a background calibration scheme (see Fig.7) based on a chopper technique [11]. This method is similar to the background calibration algorithm presented in Sec. 3.

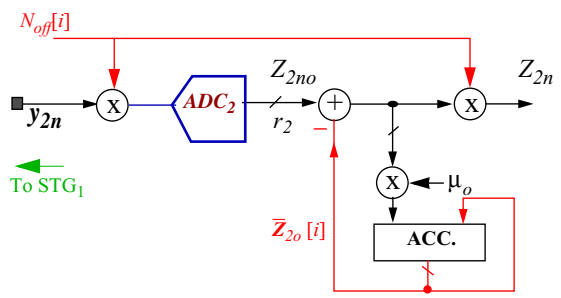

Fig. 7 Chopper offset calibration

The amplified residue y_{2n} is multiplied by a digital noise $N_{off}[i]$, no-correlated with both $N[i]$ and the input signal x signal. After that, it is converted by the ADC$_2$. Then, a digital block using an adaptive approach estimates and removes the offset. This technique also compensates the contribution of β_2 to the global ADC offset .

Zone Factor K[i] Correction

The explored solution to correct the *Zone Factor* consists in detecting if Z_{2n} is within a range of specific values. In these ranges (called *Averaging Windows*), the expected value of the noise signal $(Z_2[i] \cdot N[i])$ must still be maintained constant with respect to the input signal and equal to the absolute value obtained by (13). For values of Z_{2n} inside the *Averaging Windows,* the *Zone Factor* has the same definition, for outside values is zero. Therefore, the samples of the signal that produce Z_{2n} values outside the *Averaging Windows* do not contribute to the adaptive averaging. The *Averaging Windows* are the shadows areas in Fig. 8. They have a maximum width of $q_1/2$ and they are centred just in the middle of two potency points. To determine the real width, the highest value of the offset in ADC$_2$, $Z_{os2} \geq |\beta_2|/q_2$ must be taken into account. Thus, the width is defined as,

$$\Lambda_w = \frac{q_1}{2}\left(1 - \frac{Z_{os2}}{2^{r_2-1}}\right) \tag{24}$$

Figure 9a shows in detail how the *Averaging Windows* are defined. We can observe a zoom of the transfer characteristic of $Z_{2n}(x)$ around an interval of two potencies ($\tilde{p}_k$ and $\tilde{p}_{k+1}$). Three transfer characteristics are plotted to indicate their possible variations with respect to the offset β_2. The detection of the *Averaging Window* can be practically performed comparing the code $Z_{2cal}[i]$ with two thresholds that depends on the selected value of the offset. The threshold values can be updated following the variations of the

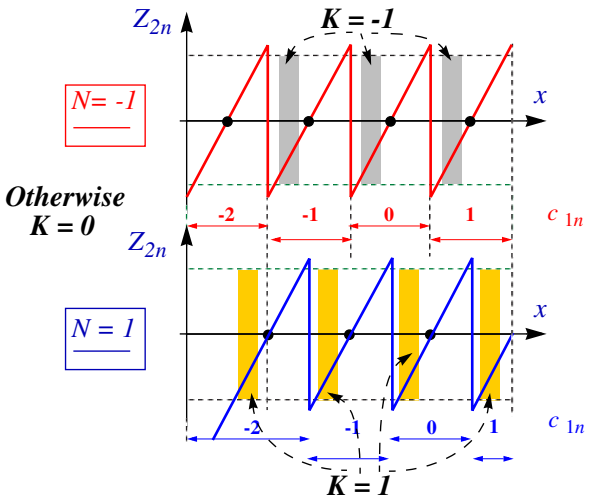

Fig. 8 *Averaging Windows* definition and $K[i]$ Correction

$Z_{2n}(x)$ gain, including them in an adaptive cycle that simultaneously converges to the estimation of the gain error.

5.2. Non-ideal Effects in sub-ADC$_1$

The main consequence of considering a real sub-ADC$_1$ is similar to the analysed at the beginning of the previous section: incorrect definition of the *shadow-light* areas, and therefore, the introduction of distortion due to the error in the estimation of $K[i]$.

In Fig. 9b, a detail of the characteristic of $Z_{2n}(x)$ with variations due to the admissible displacements in the transitions Δ_T of the sub-ADC$_1$ (1-bit redundancy) is shown. Notice that in main practice cases it is possible to define a common window that assure a correct definition of $K[i]$ in the presence of both offset error in ADC$_2$ and non-linear errors in sub-ADC$_1$. Moreover, to increase the width of the window this technique can be used in combination with the ADC$_2$ offset calibration (see Fig.7).

The above approach has been applicated in an example with the same parameters than in Sec. 4, but considering offsets in ADC$_2$ and comparators in sub-ADC$_1$ (input amplitude $1.8V_{pp}$, $\beta_2 = \Delta_{T_{max}} = 40mV$, $e_1 \cdot \alpha_2 = 20\%$). Fig. 9c shows the ENOB evolution. The calibration system uses the *Direct Implementation* ($\mu_{dir} = 2^{-30}$) with an accumulator of 41 bits and a multiplier of 13 bits.

6. Conclusions

This paper has presented a new algorithm to calibrate both the MDAC gain error of the stage under calibration and the global gain error associated to the uncalibrated stages in a background mode. As it uses a noise signal to control the transfer characteristic of a two-residue stage, it does not suppose a reduction of the dynamic rate.

We have proved the validity of the algorithm, studying and solving the problems associated to non-linear errors in sub-ADCs and uncalibrated back-end stages.

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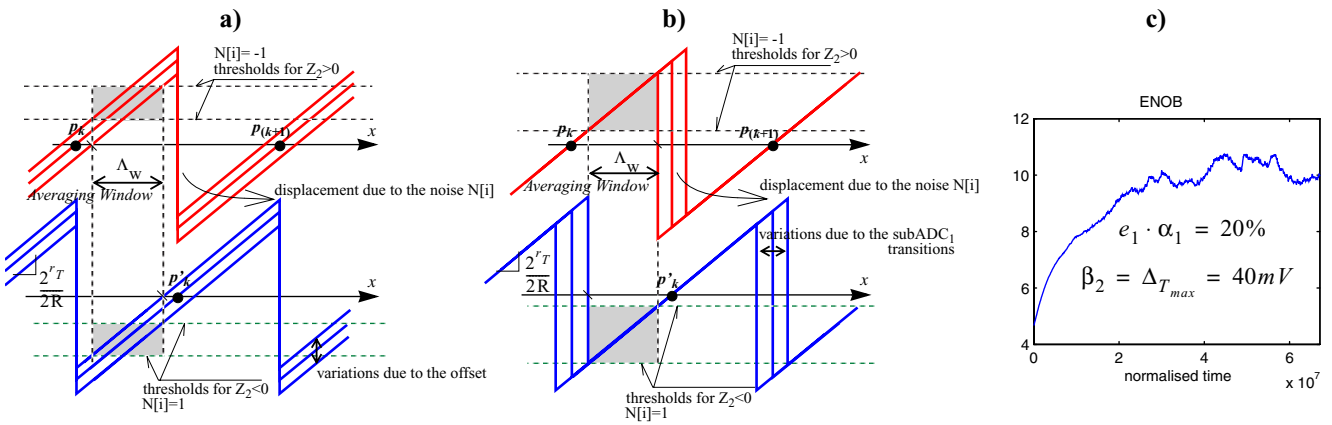

Fig. 9 a) and b): Ilustrating the detection of the *Averaging Windows;*
c) ENOB for a system with chopper offset calibration and *Averaging Windows* technique