A Novel Technique to Improve Noise Immunity of CMOS Dynamic Logic Circuits

Li Ding
University of Michigan, Ann Arbor
lding@eecs.umich.edu

Pinaki Mazumder
University of Michigan, Ann Arbor
mazum@eecs.umich.edu

ABSTRACT

Dynamic CMOS logic circuits are widely employed in high performance VLSI chips in pursuing very high system performance. However, dynamic circuits are inherently less resistant to noises than static CMOS gates. With the increasing stringent noise requirement due to aggressive technology scaling, the noise tolerance of dynamic circuits has to be first improved for the overall reliable operation of VLSI systems. In this paper, we present a novel noise-tolerant design technique using circuitry exhibiting a negative differential resistance effect. We have demonstrated that using the proposed method the noise tolerance of dynamic logic gates can be improved beyond the level of static CMOS logic gates while the performance advantage of dynamic circuits is still retained.

Categories and Subject Descriptors: B.7.3 [Integrated Circuits]: Reliability and Testing; B.8.1 [Performance and Reliability]: Reliability, Testing, and Fault-Tolerance

General Terms: Design, Performance, Reliability.

Keywords: Dynamic circuits, Domino logic style, Noise-tolerant design, Negative differential resistance, Digital integrated circuits

1. INTRODUCTION

Recent years have seen wider use of dynamic CMOS logic circuits in pursuing higher performance of VLSI systems. Circuits designed using dynamic logic styles can be considerably faster and more compact than their static CMOS counterparts. Criticism on dynamic circuits is often related to their relatively poor noise tolerance. The switching threshold voltage of a dynamic logic gate, defined as the input voltage level at which the gate output changes state, is usually the transistor threshold voltage. In comparison, the switching threshold voltage of static CMOS logic gates is about half the power supply voltage. Therefore, dynamic logic gates inherently have less noise immunity than static logic gates and are the weak link in a high performance VLSI chip.

A large number of design techniques have been developed in the literature in an effort to reinforce this weak link. For example, feedback keepers were used to prevent floating nodes; internal nodes were precharged to eliminate charge sharing; and weak complementary pull-up network is used to improve the noise tolerance to the level of skewed static logic gates. However, existing remedial techniques improve dynamic circuit noise tolerance at a significant cost in terms of circuit area, speed, and/or power consumption. It is observed that the amount of overhead increases dramatically when the noise tolerance requirement is increased along with the continuous down-scaling of process technology. Therefore, effective noise-tolerant design techniques that incur little overhead in silicon area, speed and power consumption are highly demanded.

In this paper, we present a novel design method to enhance the noise tolerance of dynamic circuits. We show that dynamic logic gates are not necessarily less noise tolerant if proper noise-aware design techniques are employed. In fact, using the method proposed in this paper, dynamic logic circuits can have higher level of noise-tolerance than static CMOS logic gates while still retaining their advantage in performance.

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2. OVERVIEW OF PREVIOUS WORKS

In this section we present a brief overview and our classification of noise-tolerant design techniques available in the literature.

Employing Keeper: Perhaps the simplest way to enhance the noise tolerance of dynamic CMOS logic gates is to employ a weak pull-up transistor, known as keeper [9], [13]. As shown in Fig. 1(a), the keeper supplies a small current to the dynamic node so that the charge stored is maintained. Recently, more advanced keeper designs have been developed which temporarily disable itself during the time window when the gate switches to allow faster discharging (see, e.g., Fig. 1(b)). Those techniques are very effective against gate internal noises like leakage noise. However, dynamic gates with those keepers are still susceptible to external noise glitches because they are not adequately protected during switching.

Precharging Internal Nodes: In complex dynamic logic gates with large pull-down network, charge sharing between the dynamic node and the internal nodes in the pull-down network may result in false gate switching. A simple yet effective way to prevent the charge sharing problem is to precharge the internal nodes in the pull-down network along with precharging the dynamic node [10], [14], as illustrated in Fig. 1(c). It is noted that techniques based on precharging internal nodes alone are not very effective against external noises like noises injected at gate inputs.

Raising Source Voltage: An effective way to improve noise tolerance against both internal and external noises is to increase the source voltage of the transistors in the pull-down network [2], [7], [15], [16]. Since the gate voltage has to be greater than the sum of the source voltage and the transistor threshold voltage when a transistor is turned on, higher source voltage directly and indirectly (through threshold voltage body effect) leads to increased gate turn-on voltage. An example circuit implementation is illustrated in

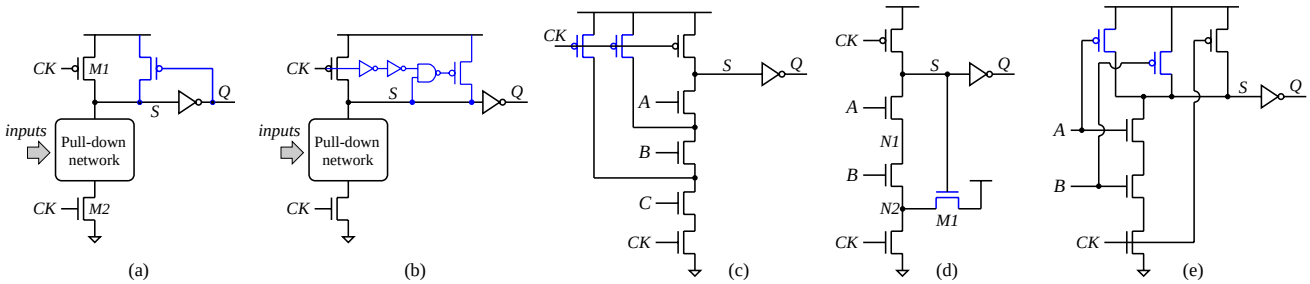

Figure 1: (a) Conventional feedback keeper [13]. (b) Conditional feedback keeper [1]. (c) Precharging internal nodes [10]. (d) Raising source voltage [15]. (e) Constructing complementary p-network [11].

Fig. 1(d), where the NMOS transistor *M1* is used to pull-up the voltage at node *N2*. The feedback design allows the pull-up transistor to be shut off when the voltage of the dynamic node goes low. It is noted that there is potential DC power consumption in the resistive voltage divider. In fact, extra circuitry is always necessary for techniques in this category to eliminate the DC conducting problem, which may lead to increased cost and reduced performance.

Constructing Complementary p-Network: A weak complementary p-network can also be constructed to prevent the dynamic node from floating [3], [5], [8], [11]. One such technique [11] is illustrated in Fig. 1(e). The gate operates in a similar way as a normal domino gate in the precharge phase. In the evaluation phase, the logic gate behaves as a skewed CMOS logic gate. Therefore, the switching threshold voltage of the dynamic logic gate is improved. In additional to the silicon area overhead of the pull-up network, a major drawback of this technique is its ineffectiveness in dealing with very wide logic gates, where dynamic logic styles really outshine static CMOS logic gates in performance. Similarly, noise-tolerant design techniques in this category require considerably more silicon area.

A desirable noise-tolerant design technique should meet the following requirements. 1) It improves gate noise tolerance against all types of noises; 2) is suitable for all logic functions; 3) has minimal circuit area overhead; 4) has minimal circuit speed overhead; and 5) consumes no DC power and has minimal AC power overhead. It is observed that few existing techniques meet all above requirements. Some techniques, for example, employing conditional feedback keeper or precharging internal nodes, only improve gate noise immunity against certain types of noises. Other techniques, like constructing complementary p-network based techniques or raising source voltage based techniques that have no DC power consumption, require significantly larger silicon area and may result to slower circuits. In fact, the simple feedback keeper technique is perhaps the only general-purpose technique that improve dynamic logic gate noise immunity against all types of noise without significant increase in area, speed, or power consumption.

3. PROPOSED DESIGN TECHNIQUE

The simple feedback keeper technique is effective and easy to design. However, choosing the right size of the keeper is a dilemma. On one hand, a strong keeper is required to achieve high gate noise tolerance. On the other hand, large keeper leads to significant contention during normal gate switching, therefore deteriorates gate performance. The conditional keeper technique [1] temporarily disables the keeper to alleviate the contention problem. But it is not effective against gate input noises because the gate is not adequately protected during the switching time window.

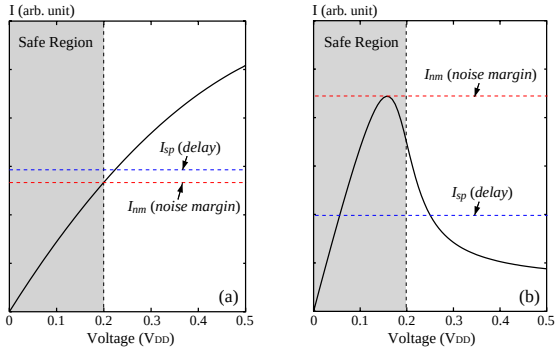

Figure 2: Comparing keeper strengths for noise margin and for gate speed purposes. (a) Field-effect transistor. (b) NDR device.

Noise immunity against input noises is very difficult to improve without significant sacrifice in circuit performance because the gate should not act before it identifies whether the input is noise or real signal. This inevitable time needed to distinguish noise from real signal is a main cause of circuit performance degradation. This performance overhead cannot be completely eliminated. However, it can be reduced to a large extent. Our proposed technique enhances dynamic gate noise immunity against all types of noises including the input noise and at the same time it incurs very little cost in performance.

3.1 Basic Principle

First, let us carefully re-examine the noise tolerance versus speed conundrum. It may be observed that there is an ambiguity in the definition of the strength of the keeper. The keeper strength that determines gate noise tolerance is not necessarily the same as the keeper strength that governs the gate performance. Let us measure the keeper strength in terms of the current supplied by the keeper.

- Keeper strength that determines gate speed is approximately the *average* current given by

$$I_{sp} \simeq \frac{2}{V_{DD}} \int_0^{V_{DD}/2} I(V)dV. \quad (1)$$

- Keeper strength that determines gate noise robustness is the small-signal *maximum* current, defined as

$$I_{nm} = \max_{0 \le V \le V_D} (I(V)), \quad (2)$$

where V_D is the maximum allowed voltage deviation at the dynamic node and it is often much smaller than $V_{DD}/2$.

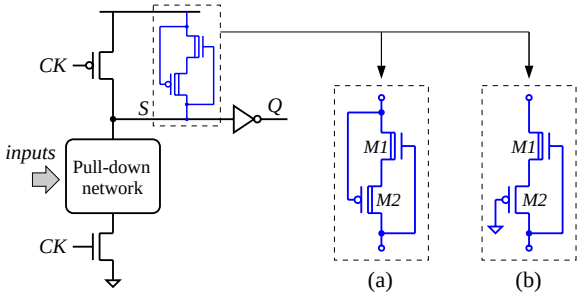

Figure 3: MOSFET-based smart keepers.

It is the difference between keeper strength for gate performance and keeper strength for gate noise immunity that makes it possible to enhance the noise tolerance of a dynamic logic gate while still retaining its performance. We will hereafter call a keeper that aggressively explore this difference a *smart keeper*.

The goal of circuit designers is, therefore, to find a keeper that has a large I_{nm} and, at the same time, a small I_{sp}. However, this goal is not able to be materialized using a single field-effect transistor. It can be shown that I_{sp}/I_{nm} has a lower bound of $1-V_D/V_{DD}$ for MOS keepers with a monotonic and concave I-V characteristic [6]. In reality, the delay keeper strength I_{sp} is often comparable to, if not greater than, the noise keeper strength I_{nm}, as shown in Fig. 2(a).

On the other hand, if the I-V characteristic of a keeper is not monotonic, i.e., it has one or more negative differential resistance (NDR) regions, I_{sp} can be significantly smaller than I_{nm}, as illustrated in Fig. 2(b). This suggests that noise margin of dynamic logic gates can be greatly improved with little performance overhead if the keeper has the NDR property. It is noted that the NDR region has to appear before the voltage across the keeper to reach $V_{DD}/2$ for the benefit of the NDR property to be fully appreciated.

3.2 MOSFETs Based Smart Keepers

Circuits designed using MOSFET devices that exhibit the NDR property have been studied in the literature [4]. Those existing NDR circuits constitute a pool of potential MOSFET-based smart keepers. Here we will demonstrate how those NDR circuits can be employed in the keeper network by using one of the simplest of those NDR circuits, as shown in Fig. 3. This keeper consists of cross-coupled depletion-mode transistors *M1* and *M2*. Since the gate of *M1* is connected to the dynamic node *S*, the current through the keeper will be cut off immediately when the voltage at *S* drops to the turn-off voltage of *M1*. It is noted that we can alternatively use an enhancement-mode PMOS transistor to replace the depletion-mode transistor *M2*, as shown in Fig. 3(b).

3.3 NDR Devices Based Smart Keepers

Smart keepers can also be realized using devices that intrinsically have the folded-back I-V characteristic. The keeper can be either a three-terminal NDR device or series connected two-terminal NDR device and a feedback controlled MOS transistor, as illustrated in Fig. 4. Common semiconductor NDR devices include tunnel diodes, resonant tunneling diodes (RTD), resonant interband tunneling diodes, resonant tunneling transistors, etc. An extensive overview of semiconductor devices including those having the NDR property can be found in [12]. In this paper, we will take the RTD+FET implementation as an example. The I-V characteristic of a typical RTD is shown in Fig. 4.

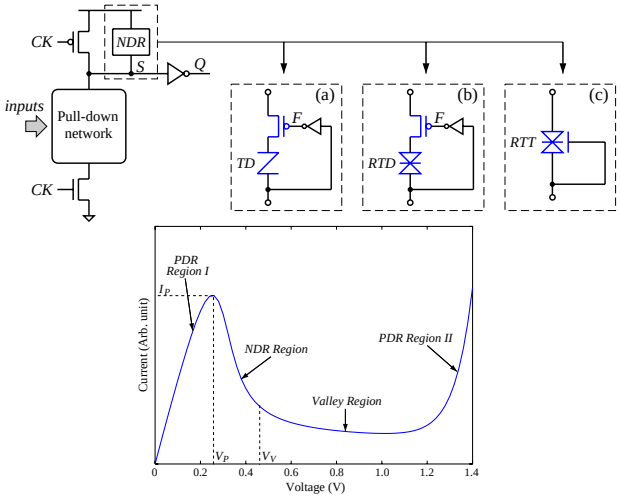

Figure 4: Smart keepers designed using intrinsic NDR devices and typical I-V characteristic of RTDs.

4. EXPERIMENTAL RESULTS

In this section, we describe the simulation results for a number of wide domino logic gates with the conventional keeper and with the proposed smart keepers. The circuits are designed using a 0.18-μm process technology and the simulation is carried out using HSPICE at 1.6 V supply voltage and at a temperature of 55^{o}C.

We first study how gate delay rises when the gate noise tolerance level is increased. An 8-input domino OR gate is used as the test vehicle in this study. The load capacitance of the gate is 50 fF and the clock frequency used in the simulation is 500 MHz. The comparisons are shown in Fig. 5(a), where *FBK* denotes feedback keeper, *SK1* denotes MOSFET-based smart keeper, and *SK2* is the RTD+FET-based smart keeper. Domino logic gates with proposed smart keepers have significantly reduced performance overhead in comparing with the conventional feedback keeper based design. The performance benefit of using the proposed keepers is even greater when the noise-tolerant requirement is high. It is also observed that the intrinsic NDR device based keeper is managed to offer the best in performance among the three designs.

Dynamic noise rejection curves of domino gates with different keepers are compared in Fig. 5(b). The rejection curves of the proposed keepers are always higher than that of the feedback keeper meaning that they have higher noise immunity. It is also observed that the difference in dynamic noise immunity among the keepers are reduced when the input noise duration is extremely small. This is essential for the high performance operation of dynamic logic gates employing the proposed keepers [6].

The transient waveforms are compared in Fig. 5(b), where we have sized the keepers such that they provide same gate noise tolerance level. It is observed that the dynamic nodes discharge approximately at the same rate initially, but S_{SK1} and S_{SK2} have an accelerated discharge process due to the reduced keeper current. Overall, dynamic logic gates using the proposed keepers switch considerably faster than gates using the conventional feedback keeper.

We have further compared performance of dynamic logic gates with different keepers by designing a set of wide fan-in multiplexers (MUXes). The results are shown in Table 1. Overall, the proposed keepers are consistently and significantly better than the conventional feedback keeper in preserving the performance of dynamic logic gates when gate noise tolerance is tuned up. Further-

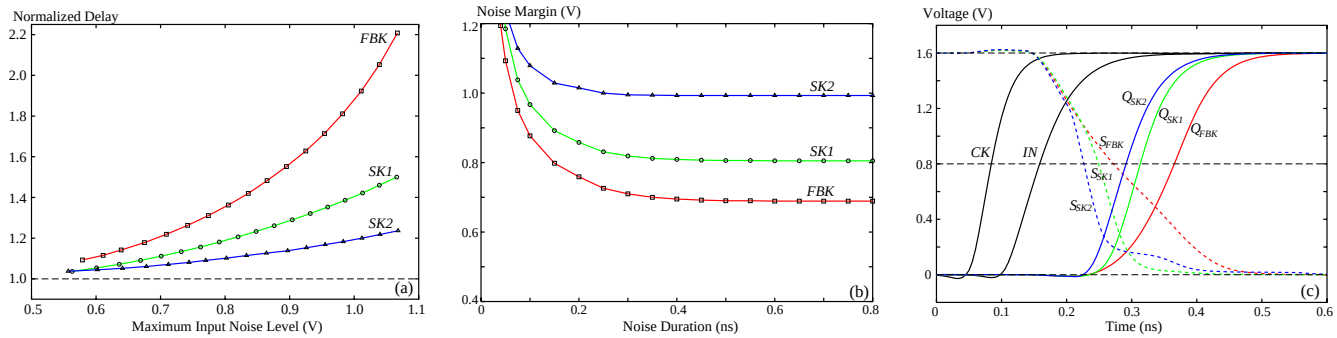

Figure 5: (a) Gate delay versus input noise tolerance level. (b) Dynamic noise rejection curves. (c) Transient waveforms.

Table 1: Performance Comparison for MUXes at Same Noise Tolerance Level

Noise Level (V)	MUX (bit)	Feedback Keeper (FBK)		Smart Keeper 1 (SK1)		Smart Keeper 2 (SK2)	
		Delay (ps)	Power (μW)	Delay (ps)	Power (μW)	Delay (ps)	Power (μW)
0.6	8	136.7 (11.7%)	145.8	128.3 (4.8%)	137.2	127.1 (3.8%)	147.4
	16	159.5 (10.1%)	160.9	151.5 (4.6%)	151.2	150.0 (3.5%)	161.5
	32	203.1 (9.4%)	192.7	194.1 (4.6%)	181.3	191.6 (3.2%)	191.4
0.7	8	150.5 (23.0%)	156.0	136.2 (11.3%)	140.9	129.9 (6.1%)	153.8
	16	176.2 (21.6%)	172.5	159.3 (9.9%)	155.0	153.2 (5.7%)	168.0
	32	223.9 (20.6%)	206.9	204.5 (10.2%)	186.2	196.0 (5.6%)	197.9
0.8	8	175.6 (43.5%)	173.4	147.6 (20.6%)	146.4	134.3 (9.7%)	161.9
	16	204.4 (41.1%)	192.3	170.6 (17.7%)	160.5	158.3 (9.2%)	176.4
	32	258.7 (39.4%)	231.6	218.9 (17.9%)	193.3	202.9 (9.3%)	206.5
0.9	8	220.2 (79.9%)	204.2	163.4 (33.5%)	154.1	139.6 (14.1%)	177.4
	16	254.6 (75.7%)	227.6	185.8 (28.2%)	167.9	164.3 (13.4%)	182.2
	32	320.9 (72.9%)	275.9	238.5 (28.5%)	203.1	210.6 (13.5%)	222.8
1.0	8	333.7 (172.6%)	282.6	185.4 (51.5%)	164.8	146.8 (19.9%)	196.6
	16	383.1 (164.4%)	318.4	205.7 (42.0%)	177.8	172.4 (19.0%)	211.5
	32	479.6 (158.4%)	392.2	264.6 (42.6%)	216.3	221.4 (19.3%)	242.7

more, it can also be observed from the table that the advantage of the proposed keeper is more evident when the gate noise robustness requirement is high. This suggests that it will be more rewarding to use the proposed technique as the process technology continues to scale down aggressively and the noise problem assumes more prominence in noise-aware design methodologies. Finally, experimental results also support that the noise tolerance of dynamic logic gates can be improved beyond the level of static CMOS logic gates while their advantage in performance is still retained.

5. CONCLUSIONS

The main contributions of this paper are as follows. First, we have identified the difference between keeper strength for noise immunity and keeper strength for speed, which opens the possibility for circuit noise immunity improvement without a proportional increase in delay. Second, we have proposed to use a class of circuits having the NDR property to explore the difference in keeper strength for speed and for noise immunity. And third, we have proposed two circuit realizations of the NDR keeper and have demonstrated the potential benefit of the proposed technique.

The proposed technique is not limited to domino logic gates. It can also be applied to other combinational dynamic logic circuits as well as sequential circuits like latches and flip-flops that have internal precharged nodes. This constitutes one direction of future researches. In the other direction, we will also search for other suitable circuit implementations that aggressively explore the benefit of the noise-tolerant design principle described in this paper.

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