CHIME: Coupled Hierarchical Inductance Model Evaluation

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Abstract

Modeling inductive effects accurately *and* efficiently is a critical necessity for design verification of high performance integrated systems. While several techniques have been suggested to address this problem, they are mostly based on sparsification schemes for the L or L-inverse matrix. In this paper, we introduce CHIME, a methodology for non-local inductance modeling and simulation. CHIME is based on a hierarchical model of inductance that accounts for all inductive couplings at a linear cost, *without* requiring any window size assumptions for sparsification. The efficacy of our approach stems from representing the mutual inductive couplings at various levels of hierarchy, rather than discarding some of them. A prototype implementation demonstrates orders of magnitude speedup over a full, flat model and significant accuracy improvements over a truncated model. Importantly, this hierarchical circuit simulation capability produces a solution that is as accurate as the hierarchically extracted circuits, thereby providing a "golden standard" against which simpler truncation based models can be validated.

Categories and Subject Descriptors: I.6.5: Model development; B.7.2: Simulation

General Terms: Algorithms, Verification

Keywords: Inductance modeling, Circuit simulation

1. INTRODUCTION

The continual increase in operating frequencies and the presence of longer length wires (long data buses, for example) make inductive modeling a crucial factor for design verification of today's integrated systems. This is especially the case for System in a Package (SiP) solutions which are becoming more economically attractive. For SiPs, multiple chips are integrated in a single package substrate, and the mutual inductance modeling problem becomes overwhelming due to the conductance and lengths of the metal interconnects. Unlike capacitive coupling, inductive coupling is a more challenging modeling problem since inductance is inherently non-local and an arbitrary truncation of "far-away" mutual inductances can lead to significant errors or even model instability [1]. Numerically this is explained by the inductance matrix which is positive definite but *not* diagonally dominant. Therefore, discarding small off-diagonal elements without a measure of the resulting impact on its positive definiteness can easily make the sparsified inductance matrix unstable.

A number of approaches have been suggested to render different truncated approximations of the inductance matrix positive definite [1], [2] for circuit simulation. Other schemes are based on the inverted inductance matrix which, like the capacitance matrix, is amenable to truncation [3]. While all of these techniques lead to a stable truncation of the full, flat inductance matrix, they ignore the far-away coupling effects outside a certain window of influence. The significance of the error incurred due to the truncation approximation can be judged only by checking the results against those of the full, flat simulation model, which is often an intractable simulation problem. Clearly, it is desirable to have a feasible "golden standard" model which includes the aggregate impact of the far-away inductance effects so that the approximate models can be evaluated in terms of accuracy.

To this end, wavelet based non-local inductance models were introduced in [4]. A zero-th order wavelet current and voltage basis was constructed for each group of conductors and an average group-to-group mutual inductance value was derived by combining individual conductor-to-conductor mutual inductances under the assumption of uniform current flow through all conductors in a group. While it is possible to improve the accuracy of this approach by going to higher orders in the wavelet basis, the irregular nature of current distribution will make inclusion of many high order terms necessary for increased accuracy. The problem is made more acute by the time-varying pattern of currents in the conductors which might change the required order of approximation (for a certain fixed accuracy) with time. A non-local model based on factors independent of the current/voltage patterns is certainly more desirable. Taking a different approach, in [5], a vector potential based resistive model was introduced to capture the non-local effects. However, extraction of the resulting resistor values is difficult and subsequent work [6] showed that an accurate extraction of these resistances requires inversion of the partial inductance matrix, which, in turn, implies some form of sparsification or windowing before matrix inversion for any realistic system size.

In this paper we describe CHIME, a methodology for hierarchical modelling and efficient spice-level simulation of inductive couplings. CHIME accounts for the far-away inductance effects at a linear (in the number of conductors present) cost *without* any sparsification requirement or assumption regarding current/voltage patterns. Fig. 1 represents the hierarchical inductive coupling model proposed in CHIME pictorially. The aim of this model is to represent

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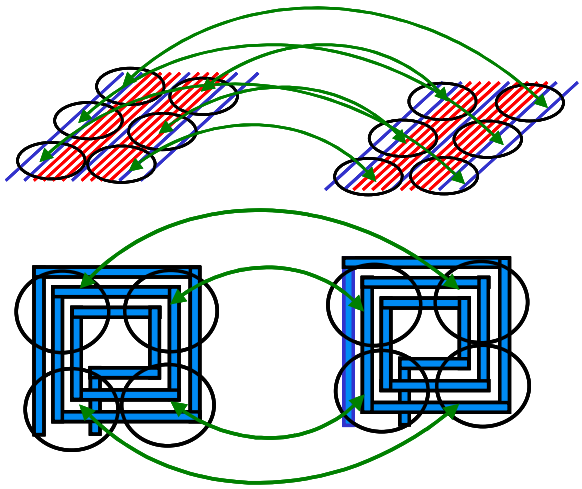

Figure 1. Hierarchical coupling between groups of conductors. Two example domains are shown: long bus lines and spiral inductors. For simplicity, not all couplings are shown.

couplings at group-to-group level with a rigorous footing. Based on the multipole expansion of potentials, the hierarchical model extends the efficiency of 1/r potential evaluation utilized in hierarchical inductance extractors [7], [8] to the circuit representation and simulation domain, while providing quantitative bounds on the modeling error compared to a fully coupled, flat circuit representation. It is shown that when two conductors are spaced far away from each other, the mutual inductance between them is, within an error bound, equivalent to the product of the lengths of the conductors and the 1/r part of the vector potential evaluated between any two points within the volumes of those conductors. This agrees with our intuition that, in determining the mutual inductance between two conductors, the geometrical details of each conductor should become decreasingly important as the distance between conductors increases.

To evaluate the 1/r part of the vector potential we apply the fast multipole algorithm [9]. Combining our vector potential based approximation of mutual inductance and the multipole algorithm, we then derive a circuit level hierarchical representation of inductive couplings for the entire system. A prototype simulator based on spice3f5 has been developed to simulate such hierarchical circuits. The prototype implementation has a 2-stage approach: 1) perform hierarchical extraction to produce a hierarchical equivalent circuit representation; and 2) simulate the hierarchically extracted model directly to generate output waveforms of interest. As our simulator can handle hierarchical models directly, the typical process of flattening the hierarchically (e.g. multipole-based) extracted circuit is not required.

The paper is organized as follows: in Section 2 we introduce the point-to-point mutual inductance approximation for far-away conductors and determine an upper bound on the error due to this approximation. In Section 3 we derive the hierarchical equivalent circuit model by combining the point-to-point mutual inductance approximation from Section 2 and the multipole algorithm structure for evaluating 1/r potentials. Section 4 presents our simulation results. We finally conclude in Section 5.

2. APPROXIMATING MUTUAL INDUCTANCE

Starting from Maxwell's equations we can derive the following expressions for inductive voltage drop after neglecting the displacement current term (which is small compared to the current density term in our frequency range of operation [10]) from the curl-B equation:

$$V_{ind}^{loop} = \frac{\mu_0}{4\pi}\frac{\partial}{\partial t}\left(\oint_{loop}\int_{vol} \frac{\overrightarrow{J(\vec{r}')} \bullet \vec{dl}}{|\vec{r}-\vec{r}'|} dv' \right)$$
$$V_{ind}^{partial} = \frac{\mu_0}{4\pi}\frac{\partial}{\partial t}\left(\int_{partial}\int_{vol} \frac{\overrightarrow{J(\vec{r}')} \bullet \vec{dl}}{|\vec{r}-\vec{r}'|} dv' \right) \quad (1)$$

where, V_{ind}^{loop} and $V_{ind}^{partial}$ are the inductive voltage drops along a closed loop and part of the closed loop respectively and J(r) is the current density.

The above equation can be split into three sets of equations; one for each current direction: x, y and z. As the forms of these equations in all three directions are similar, we can consider only one direction (say x) without any loss of generality. Discretizing our system into rectangular filaments and evaluating the (partial) inductive voltage drop over one such filament:

$$V_{x,partial}^{m} = \sum_{k=1}^{K}\sum_{n=1}^{n_k} L_{x,partial}^{m,n}\frac{\partial I_n}{\partial t}$$
$$L_{x,partial}^{m,n} = \frac{\mu_0}{4\pi}\frac{1}{a_m}\frac{1}{a_n}\int_V\int_{V'}\frac{1}{|\vec{r}-\vec{r}'|}dv'dv \quad (2)$$

Where $V_{x,partial}^{m}$ is the partial inductive voltage drop along the m-th segment, $L_{x,partial}^{m,n}$ is the x-direction mutual partial inductance between volume filaments *m* and *n* [11], and I_n is the current through the n-th segment. The subscript *x* in all these expressions refers to current flowing in the x-direction. We assume that there are *K* conductors in the system and that the *k*-th conductor is split into n_k filaments. The double volume integrals in the expression for $L_{x,partial}^{m,n}$ are evaluated over the volumes of filaments *m* and *n*. There exist closed form formulas for this double integral [12], but as we show below, it is possible to derive very simple approximations of this expression for mutual inductance between far-away rectangular conductors.

Given any two conductors *m* and *n*, the integration kernel in the expression for mutual inductance between them is upper and lower bounded by the inverse of the minimum and the maximum point-to-point distances between conductors *m* and *n* ($1/r_{min}$ and $1/r_{max}$ respectively). Using this in (2), we have:

$$\frac{\mu_0}{4\pi}\frac{1}{a_m}\frac{1}{a_n}\frac{1}{r_{min}^{m,n}}\int_V\int_{V'}dv'dv \geq L_{x,partial}^{m,n} \geq \frac{\mu_0}{4\pi}\frac{1}{a_m}\frac{1}{a_n}\frac{1}{r_{max}^{m,n}}\int_V\int_{V'}dv'dv$$
$$or \quad (3)$$
$$\frac{\mu_0}{4\pi}\frac{1}{r_{min}^{m,n}}l_m l_n \geq L_{x,partial}^{m,n} \geq \frac{\mu_0}{4\pi}\frac{1}{r_{max}^{m,n}}l_m l_n$$

Here $l_{m(n)}$ refers to the length along current direction of the *m (n)*-th conductor and $r_{min(max)}^{m,n}$ refers to the min (max) distance between conductor pair *m* and *n*. We approximate $L_{x,partial}^{m,n}$ as:

$$L_{x,\,partial}^{m,\,n,\,approx} = \frac{\mu_0}{4\pi}\frac{1}{r_{min}^{m,\,n}} l_m l_n \qquad (4)$$

Using (3) and (4) results in:

$$\frac{\mu_0}{4\pi}\left(\frac{1}{r_{min}^{m,\,n}} - \frac{1}{r_{max}^{m,\,n}}\right) l_m l_n \geq \left| L_{x,\,partial}^{m,\,n} - L_{x,\,partial}^{m,\,n,\,approx} \right| \qquad (5)$$

This establishes an upper bound on the absolute error in approximating the inductance. We can derive an upper bound on the relative error using (3) and (5):

$$\frac{\left(\frac{1}{r_{min}^{m,\,n}} - \frac{1}{r_{max}^{m,\,n}}\right)}{\frac{1}{r_{max}^{m,\,n}}} \geq \varepsilon(m,n) \qquad (6)$$

Where $\varepsilon(m,n)$ is the relative error in estimating the mutual inductance between conductors m and n using expression (4).

To evaluate the actual errors incurred with expression (4), we compared it to the closed-form expressions from [12] for the case of mutual inductance between two parallel rectangular conductors each of which are 10 μm long along current direction and 0.9 μm wide and 0.72 μm thick. The results for different spacings between these conductors are summarized in Table 1

Table 1. Inductance approximation error

Spacing (μm)	Accurate L (pH)[12]	Approx. L (pH)(4)	Relative error	Error bound (6)
20	0.47	0.5	6.4%	16.65%
40	0.243	0.25	2.75%	6.95%
60	0.164	0.167	1.73%	4.17%
80	0.123	0.125	1.25%	2.93%
100	0.099	0.1	0.98%	2.24%
120	0.0827	0.0833	0.81%	1.81%
140	0.0709	0.0714	0.69%	1.52%

These results confirm that for distances that are large compared to the size of the conductors involved, (4) provides a good approximation to the actual mutual inductance value. This enables us to split the partial inductive voltage drop in (2) into two parts: one due to the nearby conductors where the inductance has to be evaluated using the closed form expressions in [12], and the other due to the far-away conductors which can be approximated by (4) (the error due to the approximation being bounded by (5) and (6)). In other words,

$$V_{x,\,p}^{m} \approx \sum_{k=1}^{K_1}\sum_{n=1}^{n_k} L_{x,\,p}^{m,\,n}\frac{\partial I_n}{\partial t} + \sum_{k=K_1+1}^{K_2}\sum_{n=1}^{n_k} L_{x,\,p,\,app}^{m,\,n}\frac{\partial I_n}{\partial t} \qquad (7)$$

In (7) we approximate the far-away inductance $L_{x,\,p,\,app}^{m,\,n}$ by (4). We can interpret the far-away term in the expression for $V_{x,\,p}^{m}$ in (7) as the contribution from ideal point-like current sources placed at far-away point locations in space. The mutual inductance due to these far-away point sources is seen to be just the point-to-point 1/r kernel of the vector potential due to the point current sources multiplied by the lengths of the conductors.

Now let us consider two groups of conductors that are far apart. We want to approximate the inductive influence of one group on the other. Using (4) in the second term of the right-hand side of (7) yields the following expression for the partial inductive voltage drop across a group of *q* victim segments due to a far away group of *s* aggressor segments:

$$\begin{bmatrix} v_{p,\,n}^{m1} \\ v_{p,\,n}^{m2} \\ \dots \\ v_{p,\,n}^{mq} \end{bmatrix} = \frac{\mu_0}{4\pi}\begin{bmatrix} l_{m1} & 0 & \dots & 0 \\ 0 & l_{m2} & \dots & 0 \\ \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & l_{mq} \end{bmatrix}\left[\frac{1}{r}\right]_{qxs}\begin{bmatrix} l_{n1} & 0 & \dots & 0 \\ 0 & l_{n2} & \dots & 0 \\ \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & l_{ns} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{n1} \\ i_{n2} \\ \dots \\ i_{ns} \end{bmatrix} \qquad (8)$$

$$\underbrace{\left[v_{p,\,n}^{m}\right]}_{qx1} = \frac{\mu_0}{4\pi}\left(\underbrace{\left[l_m\right]}_{qxq}\right)\left(\underbrace{\left[\frac{1}{r}\right]}_{qxs}\right)\left(\underbrace{\left[l_n\right]}_{sxs}\right)\frac{d}{dt}\left(\underbrace{\left[i_n\right]}_{sx1}\right)$$

In (8), $v_{p,\,n}^{m1}$ is the partial inductive voltage induced on the first conductor in group *m* due to all the conductors in group *n*, l_{m1} is the length of the first conductor in group *m* and i_{n1} is the current through the first conductor in group *n*. $\left[v_{p,\,n}^{m}\right]$ is the vector of induced voltages on the conductors in group *m* due to the conductors in group *n*, $\left[l_m\right]$ is a diagonal matrix whose diagonal entries are the lengths of the conductors in group *m*, $\left[1/r\right]$ is a matrix whose elements are the 1/r distances between each conductor in group *m* and each conductor in group *n* and $\left[i_n\right]$ is the vector of currents in aggressor conductors. From the matrix equation in (8), we can see that an efficient representation of the $\left[1/r\right]$ matrix will lead to an efficient representation of the far away mutual inductances.

3. HIERARCHICAL CIRCUIT MODEL

Fortunately, there exists an efficient way to evaluate the 1/r potential between far-away points; namely, the fast multipole method [9]. It has been applied in both capacitance and loop inductance extraction [13], [7] to accelerate the matrix vector multiplications required in iterative matrix inversion techniques. Here we demonstrate how the multipole algorithm can be mapped into a circuit representation that approximates the impact of the far-away inductances with linear cost.

In the multipole algorithm [9], the volume consisting of a collection of point charges is partitioned into a hierarchical tree of cubes. At the lowest level of this tree, each of the leaf level cubes contains at most a pre-specified number of point charges. Each leaf level cube is abstracted by two sets of numbers: one set which captures the impact of the point charges contained in the cube on other far-away point charges (known as the multipole expansion coefficients or the multipole moments) and another set which captures the net impact of all far-away point charges on the point charges contained in the cube (known as the local expansion coefficients). The vector of multipole moments corresponding to a leaf level cube can be multiplied with a transformation matrix to generate a new set of moments that correspond to the parent of this leaf level cube. This process of generating new moment sets will be henceforth referred to as "shifting moments" in the rest of this paper. The moments can thus be

"shifted upwards" in the hierarchy till we reach the root (i.e. till we have a moment vector corresponding to the root).

The multipole moments of an aggressor cube can also be transformed into the local expansion coefficients of a victim cube. And just as the multipole moments can be shifted upwards till we reach the root, the local expansion coefficients can be shifted downwards starting from the root till we reach the leaf level cubes. Following the terminology in [13], we will refer to each of these different phases of the multipole algorithm as: Q2M (charge to multipole transformation), M2M (multipole to multipole shift), M2L (multipole to local shift), L2L (local to local shift) and finally, L2P (local to potential shift). We note that with each of these phases there is a transformation matrix involved which takes one set of moments/coefficients as input and produces the next set of moments/coefficients as output. With this notation, the multipole evaluation scheme becomes:

$$\left[\frac{1}{r}\right] = \left[L2P\right]\left[L2L\right]\cdots\left[M2L\right]\cdots\left[M2M\right]\left[Q2M\right] + \left[\varepsilon_{MP}\right] \quad (9)$$

We have left out the source (charge or current) component in (9) since our purpose is to show how the multipole algorithm evaluates the 1/r part of the potential. We should note that in (9), $\left[1/r\right]$ is the matrix of 1/r distances between points in the aggressor and the victim group. The matrices in the right-hand side (rhs) are the matrices associated with different phases of the multipole algorithm and $\left[\varepsilon_{MP}\right]$ is the error matrix due to the truncation of terms in the multipole expansion. Expressions for evaluating each element of this matrix are given in [9].

Using the first term in the rhs of (9) in (8), we obtain an approximation of the inductive voltage drop across a group of conductors due to a far-away group as:

$$\left[v^{m}_{p,n}\right] = \left[l_m\right]\left[L2P\right]\left[L2L\right]\cdots\left[M2L\right]\cdots\left[M2M\right]\left[Q2M\right]\left[l_n\right]\frac{d}{dt}\left[i_n\right] \quad (10)$$

Here $\left[l_m\right]$ and $\left[l_n\right]$ are the diagonal matrices (with filament lengths being the diagonal elements) defined in (8). As the current vector $\left[i_n\right]$ is the only time-dependent term in the rhs of (10), we can move the d/dt operator further ahead to cast (10) in the form:

$$\left[v^{m}_{p,n}\right] = \left[l_m\right]\left[L2P\right]\left[L2L\right]\cdots\left[M2L\right]\frac{d}{dt}\left(\left[M2M\right]\cdots\left[Q2M\right]\left[l_n\right]\left[i_n\right]\right) \quad (11)$$

From the point of view of circuit representation, (11) can be interpreted in the following manner: $\left[i_n\right]$ represents the vector of currents through the conductor branches of the aggressor group. The $\left[i_n\right]$ vector is multiplied with a sequence of matrices (from $\left[Q2M\right]\left[l_n\right]$ to $\left[M2M\right]$). Each of these multiplications is equivalent to linear time invariant current controlled current sources acting on a set of low level branch currents to generate a new higher level set of branch currents (e.g. current controlled current sources defined by the matrix $\left[Q2M\right]\left[l_n\right]$ multiplies the aggressor branch currents $\left[i_n\right]$ to generate a new set of *higher level* branch currents, say, $\left[i_{n'}\right]$). It is important to note that these higher level branches do not exist in the physical circuit, rather they are a modeling abstraction for our far-away inductance representation. Each matrix multiplication defines one new higher level of branches in our circuit representation. Once we have reached a level for which the next step from (11) will be the application of the d/dt operator followed by multiplication with $\left[M2L\right]$, we can interpret d/dt as the time derivative acting on the currents of the higher level branches. It follows then that the $\left[M2L\right]$ matrix can be interpreted as a matrix of mutual inductances which multiplies the di_{high}/dt term to generate induced voltages on the various higher level branches. This induced voltage is then passed downwards to the leaf-level victim conductors by means of multiplications with the $\left[L2L\right]$ and $\left[L2P\right]$ matrices in succession. This phase of matrix multiplications is equivalent to linear time invariant voltage controlled voltage sources acting on induced voltages on higher level branches to generate induced voltages on lower level branches. The process of distributing induced voltages downwards continues until we reach the leaf level segments. Due to the hierarchical structure, given a system of n conductors, the total number of mutual couplings considered in this model is $O(n)$ as opposed to $O(n^2)$ in a flat model. This can be proved following techniques similar to those used in the complexity analysis of the multipole algorithm in [9].

In summary, the hierarchical circuit can be viewed as a mapping of the multipole algorithm to an electrical circuit where currents from the far-away aggressor groups are accumulated upwards by current controlled current sources, accumulated currents at higher level branches induce voltages on other branches at the same level by means of mutual inductances and finally the induced voltages on higher level branches are distributed downwards to the lowest level conductors by voltage controlled voltage sources. As mentioned earlier, the coefficients of these controlled sources are given by the entries in the various transformation matrices involved in the multipole algorithm and the higher level mutual inductances are defined by the entries in the $\left[M2L\right]$ matrix. This circuit level representation of the hierarchical inductance model can be simulated by a spice-like circuit simulator. We have developed a version of spice3f5 to accommodate these hierarchical circuits. The results are presented in the following section.

4. CIRCUIT EXAMPLES

Accurate modeling of inductance effects is especially crucial for large signal buses and spiral inductors. We chose three examples to demonstrate the applicability of our hierarchical circuit model in these application domains. The first example shows the accuracy and efficiency of the hierarchical model compared to the full, flat model and the truncated model. The second example illustrates the use of hierarchical model to quickly optimize and design a shielding structure for data buses. Using a flat model to design and optimize the shielding structure would be orders of magnitude slower, if not infeasible. Finally, the third example shows how the hierarchical model can be used to capture inter-turn couplings in spiral inductors.

We first consider an 8 bit bus with "local" shielding lines in the middle and on the sides. In addition there are two fat shielding lines that surround the entire 8-bit bus consisting of signal and local shielding lines. The signal and local shielding lines are 0.9 μm wide and the fat shielding lines are 5 μm wide. All lines are 0.72 μm thick and 2000 μm long. We excite the 8-bit bus with a 1V ramp having a rise time of 50 ps and observe the noise impact of this bus switching on a single quiet victim line of width 0.3 μm spaced 150 μm away. All lines are split into 64 segments along the direction of current. The noise waveforms at the far end of the victim line are shown in Fig. 2. We compare three cases: full, flat extracted model, hierarchical model based on 0-th order multipole and a truncated model

where all couplings outside a window of 180 µm are ignored. The hierarchical model includes individual conductor-to-conductor couplings within a window size of 30 µm, the impact due to conductors outside this window being modelled by higher level hierarchical inductors as explained in Section 3.

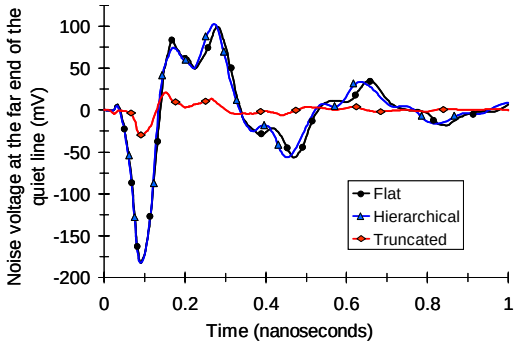

Figure 2. Noise waveform at the far end of a quiet victim line when all lines in an 8-bit aggressor bus are switching.

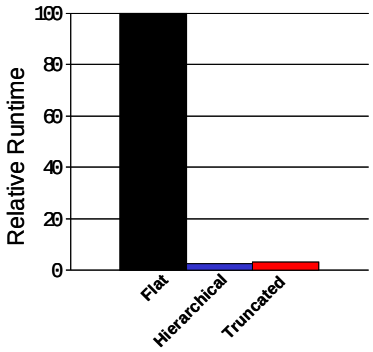

Figure 3. Relative run-time comparison for the 8-bit example

Fig. 3 shows the relative run-time comparison among flat, hierarchical and truncated models for this bus example. The hierarchical model matches the full, flat model quite well with a run-time speedup of about 40X (to give a feel for the absolute run-times, the truncated model took about 2 minutes to run on a 1.7 GHz linux machine). Truncated models with the same or marginally larger window size (6 times larger than the hierarchical case in this particular example) perform poorly in capturing the far-away noise. The accuracy of the truncated case can be improved further by increasing the window size, but that will make its runtime more and more prohibitive. Also, it is important to note that with the $O(n^2)$ vs. $O(n)$ speed difference between the flat and the hierarchical models, for larger examples, the speedup of the hierarchical model over flat will be even more substantial. To illustrate, for an example that is about 4 times larger (measured by the number of segments) than our 8-bit case, the hierarchical model will be about 160X faster than flat in a single stand-alone run. Now if we use this hierarchical model in the inner loop of a shielding structure optimization methodology, the net speedup compared to a flat model should easily reach 1000X over multiple runs. This is confirmed by our second experiment.

In this experiment, we consider a 32-bit bus structure with the same geometric features as our 8-bit bus example above (2000 µm long lines with 0.72 µm thickness and 0.9 µm width). We observe the noise impact of this bus in the worst case (all 32 lines switching at the same time under a 50 ps rise time, 1V ramp input) at a far-away (150 µm apart) quiet 4-bit bus. All lines have a load capacitance of 2 fF. The objective is to design a shielding structure for this aggressor bus that minimizes the worst case noise impact on the far-away victim bus. We use our hierarchical circuit model as the inner engine of this shielding structure optimization exercise. Our goal is to determine the number of shielding lines needed inside the aggressor bus to reduce the noise at the victim bus. Fig. 4 shows the result of our experiment.

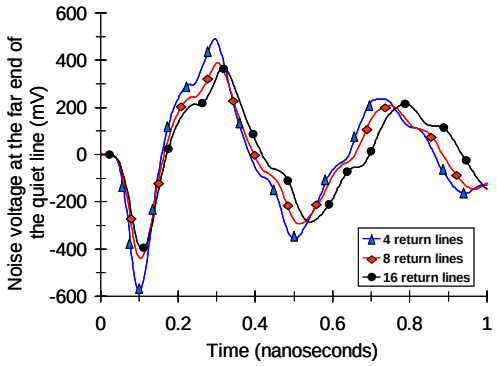

Figure 4. Noise waveform at the far end of a quiet victim line with different number of return (shielding) lines inside a 32-bit aggressor bus (all lines switching).

As we observe from the plotted results, going from 4 inner shielding lines in the 32-bit bus to 16 inner shielding lines reduces the noise voltage by about 200 mV. Further reductions in the noise voltage can be obtained by putting extra shielding lines between the 32 bit structure and the 4 bit victim bus and/or increasing the width of the shielding lines. This example demonstrates the feasibility of the hierarchical model as an inner loop evaluation engine in the design of shielding structures. The entire extraction and simulation process in this exercise took about 6 hours in a 1.7 GHz linux PC with 256 MB of main memory. The largest netlist generated during this optimization process was 8.2 MB in size (it is interesting to note that the truncated netlist with the same window size was 7.9 MB, indicating that for larger systems, the hierarchical representation becomes very close to a simple truncated representation in terms of cost. Waveforms for the truncated case are not shown here, but in terms of accuracy, the hierarchical model is significantly better than the truncated model). The full, flat netlist in this case was 96 MB in size and it took more than a day to parse the netlist before we stopped the simulation. Clearly this is a case where given the computing resources, the hierarchical model makes a previously intractable problem solvable. With increased computing resources the flat model will probably be feasible (while still being orders of magnitude slower than the hierarchical model) for this particular example, but it ultimately will become infeasible for still larger systems. The

hierarchical model, in all these cases, pushes the manageable system size much further.

As a final example, we use the hierarchical model to evaluate the coupling between two spiral inductors (500 µm x 500 µm, 600 µm center-to-center spacing and 3 turns). This is an example of a transformer where the two inductors act as primary and secondary respectively, and the coupling between them is used to modulate the net L and Q seen at the primary. For both the inductors, each turn is split into 8 segments. The substrate is modelled by a lumped 1K resistance and 0.1 pF capacitance. We use the hierarchical model to evaluate the L and the inductor Q in three cases: when the input to the two inductors are in phase (this leads to a higher net self inductance value as the self and mutual Ls aid one another), when only one inductor is activated (the net self L of that inductor) and when the two inductors have inputs with opposite phase (this leads to a lower net self inductance value as the self and mutual Ls oppose one another). Figs. 5 and 6 show the L and Q variation respectively, as captured by the hierarchical model.

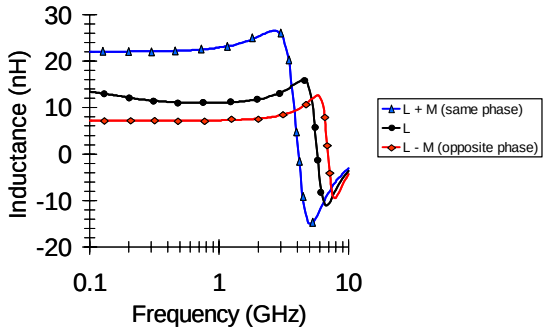

Figure 5. Inductance modulation at the primary of a transformer due to mutual coupling from the secondary.

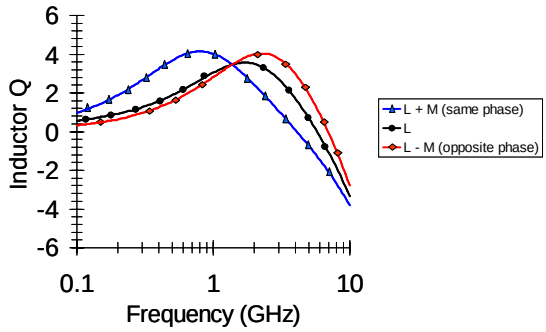

Figure 6. Inductor Q modulation at the primary of a transformer due to mutual coupling from the secondary.

5. CONCLUSIONS

Aggressive scaling of feature sizes, increasing die sizes and higher operating frequencies render a conventional full, flat modeling of inductance intractable for many integrated electronic systems. In this paper we introduce CHIME, a hierarchical inductance modelling and simulation methodology that includes the effect of the far-away inductances at a linear cost. The inductance model used in CHIME incorporates *a priori* error bounds relative to the full, flat extraction. Such a model can provide a fast but acceptably accurate "golden standard" that can effectively complement the simple localization-based inductance models used today without error control. As our experimental results demonstrate, the hierarchical model can achieve orders of magnitude speedup over a full, flat model and significant accuracy improvements over a truncated model.

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