

Trends in the Use of Re-Configurable Platforms

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Designers can create completely new processors with custom instruction set architectures (ISA), using various methods involving configurable logic. Configurable technologies also enable designers to enhance the basic ISA of standard processors or the ISA of a proprietary processor to execute at speed workloads for which the processor has not been initially conceived. Contrary to some early beliefs, the idea behind creating a custom instruction is not to compress several existing ISA instructions in one cycle; it is to execute loops requiring hundreds or thousands of iterations, faster than in a single machine, even if it were clocked at the top frequency afforded by state-of-the-art semiconductor speeds and temperature limitations.

To achieve high performance, most configurable platforms execute loop iterations in parallel; operating on multiple data in one cycle can make up for engine frequency and power limitations. Aimed at implementations in ASIC technologies, configurable platforms can be defined as designer-created mostly hardwired logic interfaced via ISA instruction enhancements

Re-configurable platforms were introduced only recently. Architectures employing FPGA-like structures instead of hardwired logic offer flexibility useful in addressing a broader range of applications and tracking evolving standards. The presentation surveys configurable and re-configurable structures including fabrics of processors, evolving trends, and the impact of soft-hardware development tools.

Fabrics of processors were initially aimed at very high performance tasks in communications. This type of architecture is also beginning to be employed in low power applications where it can offer a ratio of performance-to-power exceeding that of an implementation using one or more general-purpose processors. Several emerging fabric configurations will be described and compared: base cores using a processor element (PE) and private memory for instructions and data, PEs using local instructions' memory and communicating data, PEs that can change processing capabilities depending on the function to be executed, heterogeneous PEs and others. Software development tools' issues have kept processor fabrics from being adopted by more designers: iterative optimal routing between PEs and assignment of functions have become additional burdens on the C/C++ language programmer. None of the proposed products has acquired enough traction to justify acceptance as a standard architecture. The key to a wider adoption of re-configurable engines will be found in the soft-hardware tools offered to the programmer: two types of soft-hardware tools will be described, one using program and explicit routing, the other employing hints that can generate program and routing.