Forest vs. Trees: Where's the Slack?

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Timing closure has been a headache, is still a headache, and always will be a headache.

The fast - track evolution of consumer electronics (especially) acts to keep our pain level high: if timing closure isn't currently painful, the push for quality of result (QOR) will soon make it painful again. All of the metrics below can be traded off against each other:

QOR Metrics
- faster silicon (more capable product)
- cheaper (e.g. smaller die area, fewer metal layers)
- lower power (for cheaper cooling or for battery life)
- manufacturable (yield at reasonable cost)
- time-to-market (total project delay as well as schedule predictability)

Timing closure has to be discussed in the context of the simultaneous design closure issues today.

Point tools (The "Trees") will always evolve to help relieve the timing closure headache, however, this presentation will focus on chip level optimizations and build
methodologies ("The Forest") that go beyond block "P&R" point tools. Full-chip design approaches can harvest large improvements on all of the metrics and we shall show how exploiting "full-chip design slack" in one area can be used to ease timing closure.

In the past, there have been many heated arguments have been fought over the relative benefits and dangers of hierarchical physical design. In 2004, we find that most SoCs are being built hierarchically. Using hierarchical design creates boundaries that normally limit cross-block optimization. Typically, design teams do "over-design" or "guard-banding" on individual blocks to insure good probability of design closure. This "over-design" has varying negative effects on the full-chip QOR in the worst case even the system architecture can suffer.

Rather than sacrifice QOR, we will show chip-level automatic optimization results. Optimizations in wire length, repeaters, timing budgets, routeability and power distribution all translate into timing closure improvements. This tool uses bottom-up feedback from previously built versions of the design to achieve "as-if-flat" QOR in all the metrics listed.

With automatic high quality block optimization now available, we can then harvest the true power of hierarchy: fast full chip builds. Fast builds enable design teams to explore and verify many more design choices,. Obviously the highest leverage improvements come from exploring chip architecture alternatives assuming they can be verified with fast and accurate what-if builds. In addition, hierarchy with its inherent compartmentalized changes to the design, overcomes the chaotic behavior of P&R tools, to as much determinism and replayability as possible.

Fast builds using the actual production tools, in a synergistic way, enable the continuous bottom-up feedback optimization, with testing and 'lock-in' of solutions to the timing (and other) closure requirements of the design. The result is very smooth path from final netlist (and other deliverables) to tapeout.

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