Efficient Power/Ground Network Analysis for Power Integrity-Driven Design Methodology *

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Abstract

As technology advances, the metal width is decreasing with the length increasing, making the resistance along the power line increase substantially. Together with the nonlinear scaling of the threshold voltage that makes the ratio of the threshold voltage to the supply voltage rise, the voltage (IR) drop become a serious problem in modern VLSI design. Traditional power/ground (P/G) network analysis methods are typically very computationally expensive and thus not feasible to be integrated into floorplanning. To make the integration of the P/G analysis with floorplanning feasible, we need a very efficient, yet sufficiently accurate analysis method. In this paper, we present the methods for the fast analysis of the P/G networks at the floorplanning stage and integrate our analyzer into a commercial tool to develop a power integrity (IR drop) driven design methodology. Experimental results based on three real-world circuit designs show that our P/G network analyzer is accurate enough and very efficient. In particular, with our floorplan-based P/G network analyzer, the power integrity-driven design flow successfully fixed the IR-drop errors earlier at the floorplanning stage and thus enabled the single-pass design methodology.

Categories and Subject Descriptors: B. 7.2 [**Integrated Circuits**]: Design Aids—Layout & Simulation; J.6 [**Computer Applications**]: Computer-Aided Engineering—Computer-Aided Design

General Terms: Algorithms, Measurement, Design, Performance

Keywords: Floorplanning, Power/Ground Network

1 Introduction

Due to the continued technology shrinking, the metal width is decreasing with the length increasing. This trend makes the resistance along the power line increas substantially. Further, the supply voltage reduces at a faster pace than the threshold voltage. All these technology trends make voltage (IR) drop a serious problem in modern VLSI design. Due to the IR drop, supply voltage in logic may not be an ideal reference. This effect may weaken the driving capability of logic gates, reduce circuit performance, slow down slew rate (and thus increase power consumption), and lower noise margin [12].

Figure 1(a) shows a chip floorplan of three hard macros (HM_1, HM_2, and HM_3) and two soft macros (SM_1 and SM_2), and the power/ground (P/G) network. As shown in the figure, we refer to a pad feeding supply voltage into the chip as a *power pad*, the power line enclosing the floorplan as a *core ring*, a power line branching from a core ring into macros inside as a *power trunk*, and a pin in a macro that absorbs current (connects to a core ring or a power trunk) as an *absorb pin*. To ensure correct and reliable logic operation, we shall minimize the IR drops from the power pad to the absorb pins in a P/G network. Figure 1(a) shows an instance of voltage drop in the power supply line, in which the voltage drops by almost 30% at the absorb pin feeding into the macro HM_1. As [12] pointed out that 5% drop in supply voltage may slow down circuit performance by as much as 15% or more. Further, it is typical to limit the voltage drop within 10% of the supply voltage to guarantee proper circuit operation [2]. Therefore, IR drop is a first-order effect and can no longer be ignored during the design process, and it is of particular importance to consider the P/G network synthesis for reliable circuit operation.

1.1 Previous Work

The problem of power/ground (P/G) network synthesis has been studied extensively in the literature [1, 2, 3, 6, 7, 8, 9, 10, 11, 12]. An important problem of P/G network synthesis is to use the minimum amount of silicon area for wiring P/G network under the constraint of potential reliability such as IR drops and electromigration. There are two major tasks for the synthesis: wiring topology planning ([4, 6], etc) and wire width determination ([1, 3, 10, 11], etc).

As the design complexity increases dramatically, it is necessary to handle the IR drop problem earlier in the design cycle for better design convergence. Most existing commercial tools deal with the IR drop problem at the post-layout stage when entire chip design is completed and detailed layout and current information are known (see Figure 2(a) for the traditional design flow). However, it is often very difficult and computationally expensive to fix the P/G network at the post-layout stage. Therefore, researchers start to consider the P/G network design at the floorplanning stage [5, 12]. Liu et al. proposed an optimal power-supply-friendly algorithm based on network flow to shorten the current paths from power bumps to local power supply wiring [5]. Yim, Bae, and Kyung in [12] presented a floorplan-based planning methodology for P/G distribution for ASIC applications.

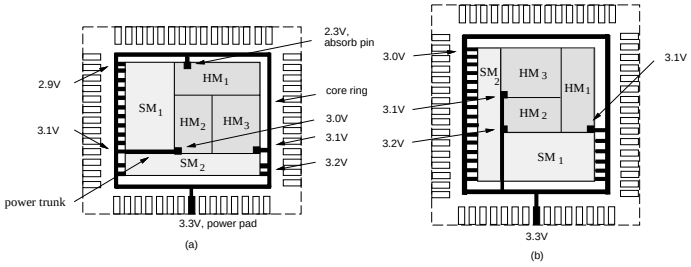

Figure 1: (a) An instance of floorplan and its P/G network structure. The worst-case voltage at absorb pins is about 30% of the supply voltage. (b) A floorplan with smaller worst-case voltage drops. The worst-case voltage is about 9%.

1.2 Our Contributions

Traditional P/G network analysis methods are typically very computationally expensive and thus not feasible to be integrated into floorplanning. To make the integration of the P/G analysis with floorplanning feasible, we need a very efficient, yet sufficiently accurate analysis method (i.e., traditional sophisticated P/G analysis and simulation do not fit our purpose for the design methodology change). In this paper, we address an efficient analysis of the P/G networks at the floorplanning stage and integrate our analyzer into commercial tools to develop a IR-drop driven design flow for real-world applications. After floorplanning, we can obtain the information about the geometries of power trunks and core rings, estimate the power consumption of each macro-cell, and build the resistor networks corresponding to the power trunks and current sources for the P/G network. Therefore, the IR drop for each macro (block) in the chip can be computed. The analysis results can then be used to guide the design of a new floorplan to generate a better P/G network. (See Figure 1(b) for a better floorplan, in which the worst-case IR drop reduces from 30% to only 9% of the supply voltage.) The iteration of floorplanning and P/G network analysis continues until the IR drop is within the given budget. Similar to [12], we presented a power integrity-driven design flow to handle the IR-drop problem earlier at the floorplanning stage. See Figure 2(b) for an illustration. Experimental results based on three real-world circuit designs show that our P/G network analyzer is very accurate and efficient. For example, the average (maximum) error for DC voltage-drop analysis obtained at the floorplanning stage is only 3.94% (8.41%), compared to the post-layout power simulation results using Synopsys/PowerMill. In particular, with our floorplan-based P/G network analyzer, the power integrity-driven design flow successfully fixed the IR-drop errors earlier at the floorplanning stage and thus enabled the single-pass design methodology, while the traditional flow needed very time-consuming and expensive iterations for all of the three designs.

The remainder of this paper is organized as follows. Section 2 formulates the power/ground (P/G) distribution network problem. Section 3 introduces the P/G network analysis. Section 4 describes the IR drop-driven design flow. Experimental results are reported in Section 5. Finally, we give conclusions in Section 6.

2 Preliminaries

There are two major tasks for our work: (1) fast P/G network analysis, and (2) integration of the analysis into the IR-drop driven design flow. Given a floorplan of a set of m rectangular macros, the locations of power pads for the whole chip and for the macros, and the cell library information (power consumption and current for cells, etc), we can generate a corresponding P/G network and compute the IR drops for all pads. If there is any IR drop violation, we can feed back the analysis results and adjust the existing floorplan and/or the

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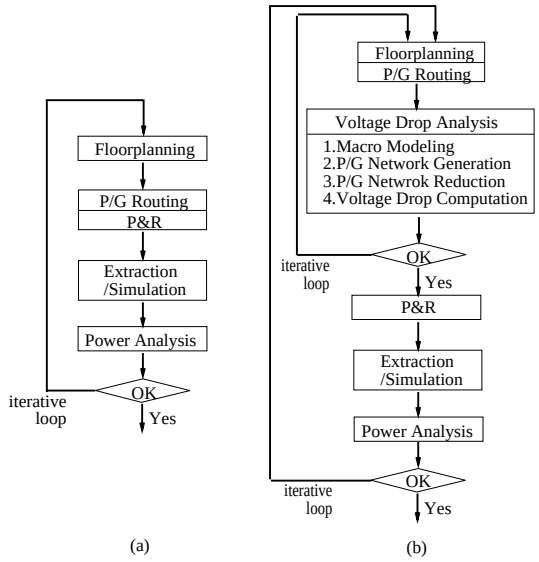

Figure 2: (a) The traditional design flow. (b) The IR drop-driven design flow.

P/G network to fix the violation. Iterations between the P/G network analysis and floorplanning (P/G network adjustment) continue until no violations occur.

We follow the notation used in [11]. Let $G = \{N, B\}$ be a P/G network with n nodes $N = \{1, 2, \ldots, n\}$ and b branches $B = \{1, 2, \ldots, b\}$. Each branch i in B connects two nodes: i_1 and i_2 with current flowing from i_1 to i_2. Let l_i and w_i be the length and width of branch i, respectively. Let ρ be the sheet resistivity, and V_i (I_i) be the voltage (current) at node i. Then the resistance r_i of branch i is $r_i = (V_{i_1} - V_{i_2})/I_i = \rho l_i / w_i$.

To ensure the correct and reliable logic operation, some constraints (e.g., IR drops, minimum widths, electromigration, etc) need to be satisfied. Here give the definitions of three major ones:

- **The IR drop constraints:** For every absorb pin i, its corresponding voltage V_i must satisfy the following constraints:
$$V_i \geq V_{min} \text{ for power networks,}$$
$$V_i \leq V_{max} \text{ for ground networks,}$$
where $V_{min}(V_{max})$ is the minimum (maximum) voltage required at the injection point of a P/G network.
- **The minimum width constraints:** The widths of the P/G lines must be greater than the minimum width allowed in the given technology. The constraint is given by
$$w_i = \frac{\rho l_i I_i}{V_{i_1} - V_{i_2}} \geq w_{i,min}, \quad (1)$$
where $w_{i,min}$ is the given constraint.
- **The electromigration constraints:** $|V_{i_1} - V_{i_2}| \leq \rho l_i \sigma$ (i.e., $I_i/w_i \leq \sigma$), where σ is a constant for a particular routing layer with a fixed thickness.

Given an initial floorplan with power pads, absorb pins, and a cell library, our objective is to obtain a feasible floorplan such that the generated P/G network satisfies the aforementioned constraints. Also, we intend to integrate the iteration between floorplanning and P/G network analysis into an existing design flow for real-world applications. To achieve this objective, we first consider P/G network analysis.

3 P/G Network Analysis

The objective of our P/G network analysis is to compute the IR drops at absorb pins in a very efficient way so that the analysis can be integrated into floorplanning. For this purpose, we need to do the following: (1) macro modeling: model macro cells as *simple* equivalent circuits, (2) P/G network generation: construct the P/G network that connect all absorb pins, (3) P/G network reduction: reduce the complexity of the generated P/G network, and (4) IR drop computation: compute the IR drops at the absorb pins.

3.1 Macro Modeling

As the example shown in Figure 1(a), the chip is composed of three hard macros and two soft macros, and is divided by the power trucks. A soft macro consists of several cell rows. For all cells in a row, we call it a unit placement row. We can model a P/G network by transforming a core ring, a power trunk, or a unit placement row into pieces of resistors and current sources. In a soft macro, there may exist several absorb pins to supply power for all cells in the macro; in contrast, each hard macro contains only one absorb pin. Therefore, the P/G networks of soft macros and hard macros are represented by different models. For instance, the P/G network of Figure 1(a) can be modeled as the equivalent circuit shown in Figure 3(a). The power consumption of a cell can be obtained from either the vendor library or a power calculator. Once the power consumption for each cell is known, we can obtained the power consumption of the soft macro P by summing up the power consumption of all cells in the macro. Then, the current I is approximated by P/V_{DD}, where V_{DD} is the supply voltage. For a soft macro with multiple absorb pins, its current can be computed by summing the current in every absorb pin in the macro. Therefore, we can further simplify the modeling of all unit placement rows as shown in Figure 3(b). The power consumption of a hard macro can be estimated by a dynamic transistor-level power simulator. *It should be noted that we use only resistors to model the circuits for the purpose of fast P/G network analysis. Other more sophisticated modelings with also capacitors and even inductors would definitely lead to more accurate analysis, but they are too computationally expensive to be incorporated into floorplanning.*

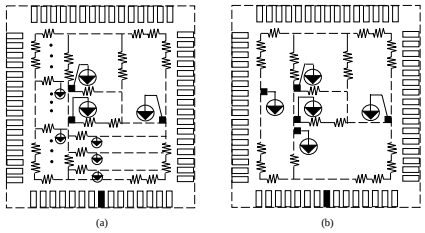

Figure 3: (a) The equivalent current source model of the P/G network shown in Figure 1(a). (b) The reduced model of (a).

3.2 P/G Network Generation

Analyzing a tree-based P/G network is relatively simpler than the mesh-based one: start at the tree leaves, and then sum up currents toward the root. This suggests a method for approaching the problem of the mesh-based network. Stark and Horowitz in [7] analyzed power supply networks using a tree-link method (see Section 3.4 for detail). They viewed power networks as trees, with an occasional loop created when the designer adds cross-links between tree nodes. Their approach provides an insight into an efficient approximation of the P/G network, which is suitable for early P/G network analysis at the floorplanning stage. Note that instead of using the very time-consuming full-mesh power analysis, what we really need here for the power integrity-driven design methodology is a very efficient yet reasonably accurate power approximation scheme.

We first consider the tree-based P/G network in this subsection. We will show in Section 3.4 how to improve the analysis accuracy by fixing the current for non-tree cases. Generating a tree-based P/G network from a floorplan consists of the following three steps: (1) traversing, (2) merging, and (3) rooting. In the traversing step, we first construct an initial network from a floorplan. Given a floorplan with several power pads, we perform a breath-first search from each pad, which is equivalent to traversing the routes of current flows. These routes constitute a network. Then, we divide the network into several subnetworks at those points where currents collapse. For example, Figures 4(a) and (c) show two floorplans with two modules and two power pads each. The respective P/G networks are given in Figures 4(b) and (d). The arrows in Figures 4(b) and (d) show the directions of currents. The points where two currents collapse are referred by dotted lines. We can further partition each network into two subnetworks from these points. (To consider the current flowing from the other power pad, we can apply the tree-link method to be discussed in Section 3.4 to fix the deficiency of the straightforward network partitioning.)

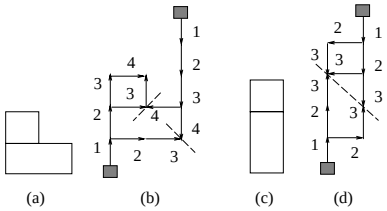

Figure 4: (a) and (c): Floorplans of two modules. (b)(d): The topologies of the P/G networks for the floorplans of (a) and (b). The network is divided into two subnetworks at the points where two currents collapse (referred by dotted lines).

After traversing, we obtain a set of subnetworks; each subnetwork consists of paths with edges and loops. In the merging step, we merge those consecutive edges without branches into one. The resistor of the new edge is the summation of the resistors in the original edges. Also, if there are two routes from point a to point b in the network, we keep only one route, and update its resistance accordingly. For instance, Figure 5(a) shows the resulting subnetwork obtained from that in Figure 4(b) after it is divided. Since the three edges from points s_1 to d_0 in Figure 5(a) do not have any branch, we can merge these edges into one with the resistance equal to the summation of those in the original edge $(3 = 1 + 1 + 1)$ (see Figure 5(b) for an illustration). In contrast, there are two

parallel routes between d_4 and d_5 of Figure 5(a), we keep only one edge with the resistance equal to one (two parallel resistors of 2 unit Ω each).

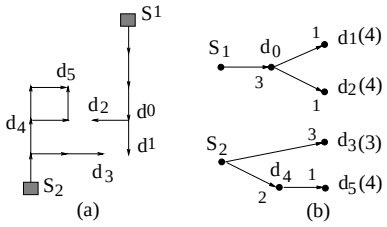

Figure 5: (a): The subnetwork after partitioning the network of Figure 4(c). (b): The merging result of (a).

At the rooting step, we transform a network into binary trees by rooting the power pad in each subnetwork. Figures 6(a) shows a network after the merging step. If we root the network from the power pad shown in the floorplan, the corresponding binary tree is given in Figure 6(b).

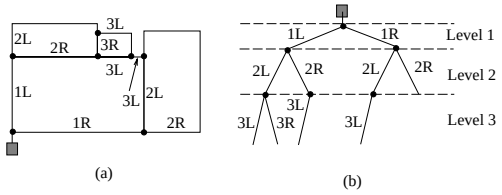

Figure 6: The P/G networks and their corresponding trees.

3.3 P/G Network Reduction

To further reduce the complexity, we can apply the techniques presented in [8, 11] to further reduce the P/G network. Consider a series of resistors as shown Figure 7(a). There exists voltage V_s between the two series ends, N_1 and N_n. Suppose that the current flows across resistor R_i is from N_i to N_{i+1}. Such a series of resistors can be modeled by an equivalent circuit shown in Figure 7(b) [8], where the current flows from N_1 to N_n. The equivalent resistor R_s is the sum of all the series resistance:

$$R_S = \sum_{i=1}^{n-1} R_i \quad (2)$$

By superposition, the equivalent currents I_{e_1} and I_{e_n} are given by

$$I_{e_1} = \sum_{i=1}^{n-2} \frac{\sum_{j=i+1}^{n-1} R_j}{R_S} I_i, \quad (3)$$

$$I_{e_n} = \sum_{i=1}^{n-2} \frac{\sum_{j=1}^{i} R_j}{R_S} I_i. \quad (4)$$

Based on superposition, the voltages at the intermediate nodes are given by

$$V_{i+1} = V_i - \frac{R_i V_s}{R_s} - R_i I_{e_i}, \quad (5)$$

$$I_{e_{i+1}} = I_{e_i} - I_i. \quad (6)$$

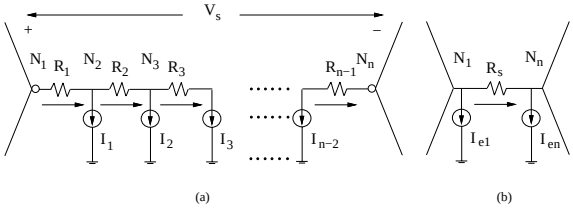

Figure 7: (a) A series resistor chain. (b) An equivalent circuit of (a).

3.4 IR Drop Computation

After constructing the binary trees corresponding to a P/G network (and possibly also reducing the network), we can compute the IR drop at each absorb pin. For this objective, we need to traverse the tree twice from leaves to the root (bottom-up) and from the root to leaves (top-down).

First, we start from the leaves of a tree. The current of the edge connecting to a leaf equals the current of the leaf, which comes from a macro. The current of other edges equals the sum of the currents in its succeeding edges. Figure 8(a) shows a tree in a P/G network. Suppose that the resistor of each branch in the tree is 1 Ω. Figure 8(b) gives the current of each node in the tree after we sum up the currents of its succeeding edges. Obtaining the current of each node, we can compute the IR drop of each edge by multiplying its current and resistor from the root to all leaves. The IR drop of each node equals the sum of the IR drops from the root. Figure 8(c) shows the IR drop for each node.

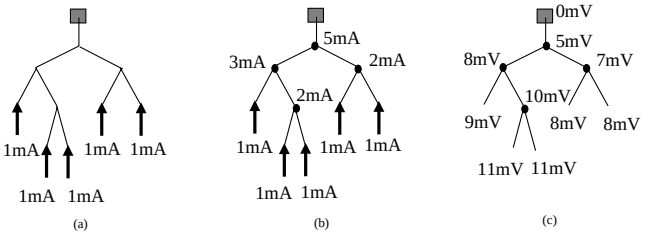

Figure 8: Computing the IR drop by traversing the tree. (a) An initial configuration. Each segment has the resistance of 1 Ω. (b) Summing up the current bottom-up. (c) Computing the voltage top-down.

For a P/G network with multiple power pads, We might need to consider tree links (i.e., a network with non-tree loops) for the current flowing from the other power pad to modify the aforementioned computation. If the P/G network consists of only one loop formed by the resistors, we can decompose the single-link network into a tree and a resistor link. Figure 9(a) shows a tree with a loop formed by the link resistor R_{link}. The link resistor takes some amount of current from one branch of the tree and redistributes it to the other. The current is affected only in the loop formed by the link and the two sides of the tree connecting to it while the current above the top node N_0, where the two branches merge, is unchanged. We can fix the voltage computation as follows:

1. Form a spanning tree for the network, as shown in Figure 9(a).
2. Solve the tree network, ignoring all non-tree resistors (see Figure 9(b)).
3. Calculate the perturbations in the current distribution caused by the link (non-tree) resistors. The step can be done by applying Kirchoff's voltage law to the loop formed by the link resistor and the spanning tree. Some current must flow through the link so that the sum of the voltage drop across all the resistors in the loop equals zero. The voltage at each node is initially calculated without the link resistors being present using the aforementioned tree algorithm shown in Figure 9(b). As the example shown in Figure 9(b), each unit of current flowing through the link resistor reduces the voltage drop between the nodes N_1 and N_0 by $I_{link}R_1$, and increases the voltage drop between nodes N_4 and N_0 by $I_{link}(R_2 + R_4)$. Given the voltage distribution calculated for the tree part of the network, the current flowing through the link resistor is
$$I_{link} = \frac{V_{link}}{\sum R_{loop}} = \frac{-2V}{4k\Omega} = -0.5mA, \quad (7)$$
where R_{loop} is the sum of resistors forming the loop, and V_{link} is the initial voltage drop across the link resistor. In Figure 9(b), $V_{link} = V_{N_1} - V_{N_4} = 5V - 7V = -2V$, and $R_{loop} = 4K\Omega$ since the loop $< N_0, N_1, N_4, N_2, N_0 >$ consists of four 1 $K\Omega$ resistors and $I_{link} = -0.5mA$.
4. Solve the network again using the revised current distribution, as shown in Figure 9. Once I_{link} is known, the tree portion of the network can be solved with the modified current distribution (see Figure 9(c)), resulting in more accurate node voltages.

For a multiple-link network, we can use the aforementioned approach to the loops individually by applying Kirchoff's voltage law, which will result in a linear system. Solving the linear system, we can obtain the current flowing through each link. Thus we can further modify the voltage at each node by using the updated current distribution.

4 IR Drop-Driven Design Flow

In this section, we describe our IR drop-driven design flow. We first read in an RTL design description and its design constraints, use a commercial synthesis tool to synthesize the design, and generate a design data. Then, we generate an initial floorplan based on the data which contains both gate-level netlist and timing constraints. After constructing the initial floorplan, we perform P/G network analysis. As mentioned earlier, there are four parts in our P/G network analysis: (1) macro modeling: soft-macro power calculation and hard-macro power calculation, (2) P/G network generation, (3) P/G network reduction, and (4) IR drop computation. If any IR constraint is violated, we adjust the chip floorplan according to the analysis results. This can be done by adjusting the macro placement, power pads' locations, and the power widths to reduce the worst-case IR drop. The iteration continues until all IR constraints are satisfied. After the IR drop constraints are satisfied for all absorb pins, we can perform placement and routing, RC parasitic extraction and post-layout power analysis.

			IR drop computed at the floorplanning stage		IR drop measured at post-layout simulation		Error	
	Block name	Area ratio	DC (mV)	Transient (mV)	DC (mV)	Transisent (mV)	DC (%)	Transient (%)
CKT-1	OSC	3.12%	63	271	66	284	-4.54%	-4.57%
	Analog	6.50%	172	205	176	233	-2.27%	-12.01%
	Digital	22.39%	93	170	87	155	6.89%	9.67%
	Memory	66.27%	98.5	268.75	99	273	-0.50%	-1.55%
	IO	1.72%	33	95	34	104	-2.94%	-8.65%
	Total Runtime/Absolute average		270 sec		158404 sec		3.43%	7.29%
CKT-2	Servo	24.38%	116	440	107	382	8.41%	15.18%
	ESP	7.53%	78	163	72	145	8.33%	12.41%
	AudioDAC	6.50%	65	192	67	201	-2.98%	-4.47%
	Decoder	1.82%	46	85	43	77	6.97%	10.38%
	Memory	50.27%	98.5	268.75	100.25	274	-1.74%	-1.74%
	IO	7.53%	33	95	35	106	-5.71%	-10.37%
	Total runtime/Absolute average		420 sec		5364150 sec		5.69%	7.75%
CKT-3	DCT/IDCT	65.23%	678	818	691	846	-1.88%	-3.30%
	Quantiation	13.75%	187	374	179	358	4.46%	4.46%
	ZZ-scan	9.14%	143	239	139	275	2.87%	13.09%
	Haff-Encoder	5.21%	100	221	97	201	3.09%	9.95%
	Haff-Decoder	6.67%	82	176	81	159	1.23%	10.69%
	Total runtime/Absolute average		375 sec		442830 sec		2.71%	8.30%

Table 1: Comparisons of the IR drops computed by our analyzer at the floorplanning stage and those measured by the post-layout simulator (PowerMill).

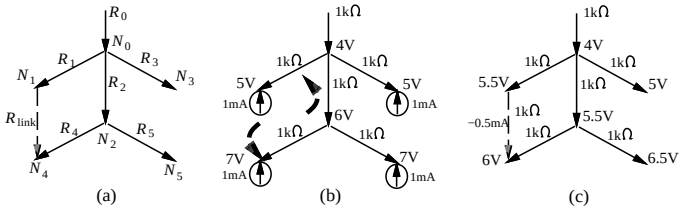

Figure 9: A single-link resistor in a tree. (a) A tree with a link between N_1 and N_4. (b) Compute the voltages by the method shown in Figure 8. (c) Fix the voltages of nodes N_2, N_4, and N_5 by the tree-link method.

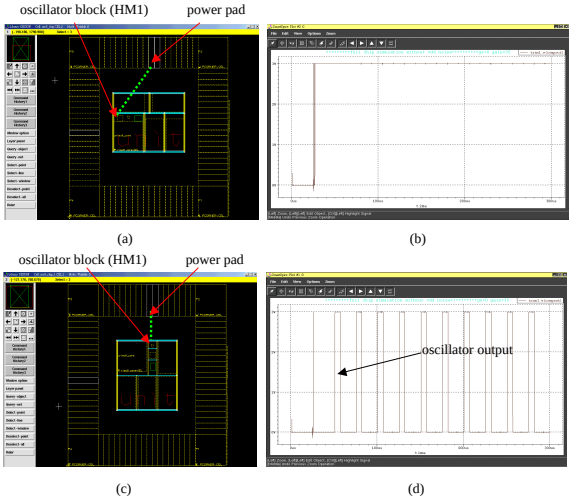

Figure 10: (a) An initial floorplan. (b) An incorrect waveform due to IR-drop errors obtained at the post-layout simulation. (c) A flooplan satisfying the IR-drop constraints. (d) A correct waveform for the oscillator circuit.

5 Experimental Results

The proposed analysis algorithms have been implemented in two perl scripts and integrated into the proposed design flow shown in Figure 2(b) on a Sun Ultra-60 Workstation. Three real designs, CKT-1, CKT-2, and CKT-3, were used to test the effectiveness of the proposed approaches. CKT-1 is a CD-MP3 core kernel running at 2.4 V–3.3 V/40 MHZ; CKT-2 is a full CD-MP3 chip at 2.4 V–3.3 V/40 MHZ; CKT-3 is an MP3 circuit at 2.4 V–3.3 V/50 MHZ. We used the Artisan 0.25 um 1P5M CMOS cell library for the three designs.

In the first experiment, we tested the effect of IR drop on the functionality of circuit designs and showed the effectiveness of our approaches in solving the problem. The errors due to IR drops occurred to all of the three designs, implying days (or even months) of iterations for fixing the errors using the traditional design flow shown in Figure 2(a). By applying our approaches, all IR-drop errors were eliminated early at the floorplanning stage. Figure 10(a) shows the initial floorplan for CKT-1. As shown in Figure 10(b), the waveform for the oscillator circuit (HM1) is not correct due to excessive IR drops. Our analysis successfully predicted such IR-drop errors during floorplanning. By fixing the floorplan as shown in Figure 10(c), the oscillator circuit is correctly operated and the waveform obtained at the post-layout simulation is shown in Figure 10(d). The results show that our approaches can predict and solve the IR drop problem early at the floorplaning stage, avoiding the expensive design iterations.

In the second experiments, we tested the accuracy and efficiency of our power/ground network analyzer running at the floorplanning stage. For each macro in the three designs, we computed its IR drop by our analyzer at the floorplaning stage and also measured it using Synopsys/PowerMill at post-layout simulation. The results are listed in Table 1. In Table 1, Columns 1 and 2 give the block names and their area ratios for the circuits. Columns 3–6 reports the DC and transient (worst-case) IR drops computed by our analyzer at the floorplaning stage and those measured by Synopsys/PowerMill at post-layout simulation. Columns 7 and 8 give the errors between those computed at the floorplanning stage and post-layout simulation. The last row for each circuit gives the running times and the *absolute* average errors. As shown in the table, our analyzer obtained very accurate IR-drop information early at the floorplaning stage, compared with the post-layout simulation. For the DC analysis, the average (maximum) errors for CKT-1, CKT-2, and CKT-3 are only 3.43% (6.89%) , 5.69% (8.41%), and 2.71% (4.46%), respectively; for the transient (worst-case) analysis, the respective average (maximum) errors for CKT-1, CKT-2, and CKT-3 are only 7.29% (12.01%), 7.75% (15.18%), and 8.30% (13.09%). In particular, our analyzer is very efficient. The running times for our analyzer are only 270 sec, 420 sec, and 375 sec while the post-layout simulations (using PowerMill) need 158404 sec, 5364150 sec, and 442830 sec for CKT-1, CKT-2, and CKT-3, respectively. The accuracy and efficiency of our power/ground network analyzer lay a strong foundation for the effectiveness of the proposed power integrity-driven design flow and enable the single-pass design methodology.

6 Conclusion

We have presented an efficient, yet sufficiently accurate analyzer for P/G network synthesis at the floorplanning stage. The analyzer has made single-pass design methodology for IR-drop power integrity possible. Future work involves developing efficient techniques for obtaining more accurate results by considering dynamic current models of macros and other dynamic behaviors of P/G networks.

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