A Synthesis Flow Toward Fast Parasitic Closure For Radio-Frequency Integrated Circuits

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ABSTRACT
An electrical and physical synthesis flow for high-speed analog and radio-frequency circuits is presented in this paper. Novel techniques aiming at fast parasitic closure are employed throughout the flow. Parasitic corners generated based on the earlier placement statistics are included for circuit resizing to enable parasitic robust designs. A performance-driven placement with simultaneous fast incremental global routing is proposed to achieve accurate parasitic estimation. Device tuning is utilized during layout to compensate for layout induced performance degradations. This methodology allows sophisticated macromodels of performances versus device variables and parasitics to be used during layout synthesis to make it truly performance-driven. Experimental results of a 4GHz LNA and a mixer demonstrate fast parasitic closure with this methodology.

Categories and Subject Descriptors
B.7.2 [**Hardware**]: Integrated Circuits - *Design Aids*

General Terms
Design, Algorithms

Keywords
Synthesis, Sizing, Layout, Parasitic, Modeling, Radio Frequency

1. INTRODUCTION
Radio-frequency circuits are highly sensitive to layout parasitics. Consequently, multiple iterations between frontend circuit design and backend layout are normally required to achieve parasitic closure. Conventionally, to account for layout effects, parasitics are extracted from an initial layout and included in subsequent resizing. Since the parasitics of only one layout is taken into account, convergence remains unpredictable. On the layout side, sensitivity based performance-driven layout techniques[2][3] has been proposed to address electrical concerns. However such performance constraints usually over-constrain the layout without acknowledging that parasitic effects can often be compensated for by device resizing. Conventional layout process is divided to placement and routing. Since parasitics cannot be estimated accurately during placement without routing details, such an approach cannot achieve satisfactory placements for parasitic-sensitive RF designs. In [4] a simultaneous floorplanning and routing algorithm is presented with floorplans represented as slicing trees. In [5] simultaneous circuit and layout synthesis is achieved with a template-based layout.

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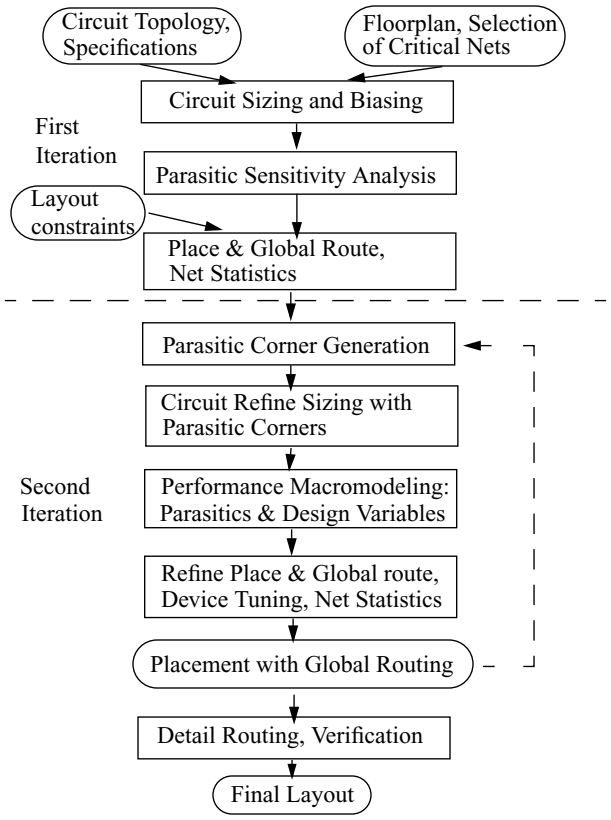

Figure 1. Proposed Circuit And Layout Synthesis Flow Diagram.

In this paper, we propose a circuit and layout synthesis flow to address the above issues. In circuit synthesis, a set of parasitic corners based on the statistics of previous layout runs is included to ensure that the sized circuits are parasitic robust. In the layout synthesis, a direct performance-driven placer with simultaneous fast incremental global routing and device tuning is proposed to maximize layout flexibility and expedite convergence. The target applications for this flow are silicon-based radio-frequency and high-speed analog IC's operating below 10GHz. In this frequency range, interconnects are treated as parasitics, not as fixed-length transmission lines as in MMIC's.

The proposed synthesis flow is shown in Figure 1. An industrial circuit synthesis tool[6] based on full simulations[8] is used. The flow starts with circuit constraints and some layout estimations. The former includes the topology of the circuit, performance specifications, while the latter includes a rough floor-plan, from which parasitics are estimated and used for synthesis. The inclusion of a layout estimate is especially helpful and practical for RF designs. After the first circuit synthesis, a sensitivity analysis is performed and more

layout specific constraints are added, followed by a direct performance-driven layout synthesis[3]. The subsequent circuit resizing and layout are the focus of this paper and will be discussed in detail in the following sections.

The paper is organized as follows. In Section 2 we present details of parasitic corner generation for circuit resizing. In Section 3 we describe macromodeling for performance-driven layout and in Section 4 we describe performance-driven placement with simultaneous incremental global routing and device tuning. Experiments on two radio-frequency designs are presented in Section 5. Finally we conclude the paper in Section 6.

2. PARASITIC CORNER GENERATION

A conventional approach for parasitic-aware circuit synthesis is to include parasitics extracted from a previous layout during circuit resizing. The key problem with this approach is that it takes only the parasitics from the last layout, but fails to capture a bigger picture. Since the same layout engine with the same goals is used in the subsequent iterations, we believe that the *history* of the parasitics over the last layout run is valuable in providing a prediction of the *future* values of the parasitics. If we can capture a bigger picture of the parasitic values in the earlier layout iteration for the circuit resizing, the resulting design should have a much greater chance of convergence.

In our proposed methodology, statistical parasitic data is recorded during the first layout synthesis after the temperature is sufficiently low to filter out hot random data. Figure 2 shows probability histograms of some RF net lengths over two successive layout runs for the LNA described in Section 5. It shows that the distributions between two runs match fairly well. The distributions are not normal, but still can be characterized by a nominal point, a lower and upper bound given a total probability coverage, say 80%, in between. This information provides a prediction of future parasitic values. Having this information, parasitic corners can be generated for the subsequent circuit resizing. We assume a linear relationship between parasitics and performances. Performances after layout are allowed to be relaxed by Δp_j from the original spec p_j *(j=1 to m)*. We assume uniform probability coverages k_j for performance j for all parasitics. The worst corner can be computed by solving k_j:

$$k_j\left(\sum_i^n s_{ij} d_i\right) = \Delta p_j \qquad (j=1 \text{ to } m) \qquad (1)$$

where s_{ij} is the sensitivity of performance j to parasitic i, d_i is the upper or lower variation of parasitic i. Whether the upper or lower variation is chosen depends on the sign of the sensitivity, thus the parasitic corner for performance j can be expressed as:

$$Corner_j = [d_1, d_2, \ldots, d_i, \ldots, d_n] \cdot k_j \qquad (2)$$

Without considering the correlations among parasitics, the parasitic corners generated in this way are pessimistic. A more rigorous corner generation method is described in [7]. For each performance j, there is one worst corner and one best corner (with the same k_j but in the opposite parasitic direction) both of which will be considered for resizing. Having both the best and worst corners makes the synthesis more centered and robust.

3. MACROMODELING

Performance macromodels are needed for performance-driven layout. Since layout parasitics have a much lower impact on the circuit

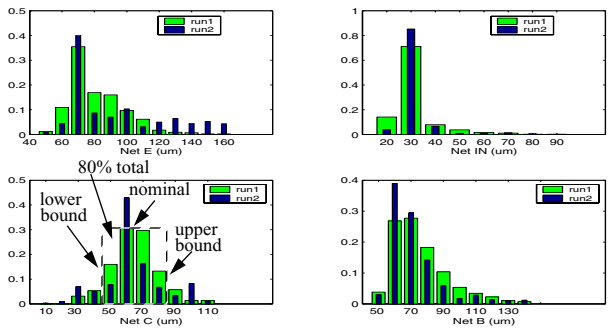

Figure 2. Probability Histograms of RF Net Lengths over Two Successive Placement Runs for the LNA Example Circuit.

than device variables, modeling parasitic effects is generally an easier task. For typical parasitic variation ranges in this application, a quadratic polynomial as shown below proved to be sufficient:

$$y = a_0 + \sum_{i=1}^{n} a_i x_i + \sum_{(i=1);(j \geq i)}^{n} a_{ij} x_i y_j \qquad (3)$$

Given the parasitic distributions, the feasible macromodeling ranges can be identified through iterative fitting experiments. To make the parasitic macromodel valid during the layout synthesis, the intermediate placements with parasitics outside the modeling ranges are penalized.

Another application of macromodeling is for device tuning. It is well known that proper device resizing can often compensate for performance degradations. And a small change in devices can potentially compensate for large degradations. Since SPICE simulation during layout is impractical, alternatively macromodels can be used. Accurate macromodeling[9] covering a wide design space is still an unsolved problem, however macromodeling for this application is viable because of greatly relaxed requirements. The goal here is, given the capability of a macromodeling method, to find a restricted set of device variables and limited ranges so that the performances can be modeled accurately. We are willing to give up those device variables or restrict their ranges if they are too difficult to model.

4. PLACEMENT WITH SIMULTANEOUS GLOBAL ROUTING AND DEVICE TUNING

Placement with simultaneous incremental global routing of critical RF nets is proposed to achieve accurate parasitic estimations. A grid-based maze router is used for the global routing task. A final detailed routing can be done manually following the global routing to complete the design. The assumption is that the final routing will have negligible parasitic discrepancy with the global routing such that the parasitic closure is maintained.

The placer itself is a commercial simulated-annealing based analog placer[1][6]. Global routing is performed for every intermediate placement. Performances are computed based on the parasitics and included in the cost function. RF specific constraints such as planarization are also considered. The overall cost function is formulated as:

$$Cost_{total} = \sum_i W_i L_i + \sum_j W_j P_j + \sum_k W_k R_k \qquad (4)$$

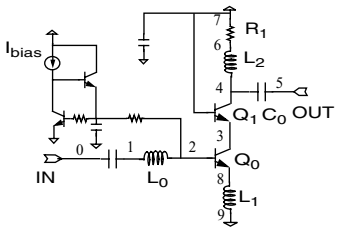

Figure 3. Example Circuit: SiGe LNA.

where L_i's are generic layout costs, P_j's are performance costs, R_k's are RF specific costs, and W's are the corresponding weights.

The speed requirement for the router is paramount since it needs to route over 10^4 placements for a typical layout run. During simulated annealing placement, device placements are incrementally perturbed. Therefore routing can be performed in the same incremental way, e.g., only those nets that are affected by the move need to be rerouted. Experiments showed that this technique alone can speed up routing by 3-5 times. An advantage of this simultaneous placement and routing strategy is that most routing congestions can be resolved by the placer, hence the router can be kept simple and fast. Rip-up/reroute is not used to save time. Nets are pre-ordered according to their symmetric constraints, sensitivities and estimated lengths. The primary cost for most nets is just the net length while the performance constraints are enforced by the placer. For relatively dense layouts, the placer alone can not resolve the cross-coupling problem. To keep the router simple and yet effective, we qualitatively introduce noisy and sensitive nets, which are routed with certain minimum separations. The placer will then evaluate the cross-coupling quantitatively through the macromodels. A grid size of typical RF net width, e.g., 5-10μm, is sufficient for accurate and fast routing. Three types of net symmetry are supported, namely, mirror symmetry, cross symmetry and self symmetry.

Simultaneous device tuning is utilized to explore the extra layout flexibility and to increase chance of convergence. Since the tuning ranges are small, typically within +/-5%, with the incremental routing, most time no new routing is needed. Using a stochastic optimization engine to solve device tuning has the advantage of supporting flexible macromodels. On the contrary, geometric programming[10] imposes restrictions such as convexity and is hard to combine efficiently with the rest of the layout synthesis problem.

5. EXPERIMENTAL RESULTS

5.1 A 4GHz SiGe Low Noise Amplifier

We first demonstrate our methodology with a 4GHz SiGe[11] low noise amplifier (LNA) shown in Figure 3. 7 independent design variables, and 10 RF nets are identified for synthesis. An RF net model with net width and length as input variables is derived from the SingleWire model from the PDK. The net width is fixed and the grid size is 10μm.

After the first circuit synthesis, all performance specs are met as shown in Table 1 Row A. Then the first placement is performed with RF net statistics collected as shown in Figure 2. As shown in Table 1 Row B, S22 and S11 specs are not met with this layout. Then parasitic corners of S11 and S22 are determined following (1). A resizing with the corners is performed. The results are shown in Table 1 Row C. Table 2 shows results of the S22, S11, at the nominal and worst parasitic corners after this resizing. A separate resizing without parasitic corners is also performed and shown in Table 1 Row C' and Table 2. Its results at nominal point meet specs, but fail at both corners. This demonstrates that the design with parasitic corners are more parasitic robust.

Table 1: LNA Synthesis Results*

	S11 (dB)	S22 (dB)	S21 (dB)	NF (dB)	IIP3 (dBm)	Runtime(s)
Specs	-16/-15	-16/-15	17	1.6	-5	
A	-16.7	-16.7	18.9	1.53	-3.2	2120
B	**-14.7**	**-14.3**	17.8	1.60	-2.7	230
C	-17.1	-16.3	17.0	1.59	-3.0	820
D	-16.9	-15.9	17.2	1.56	-2.5	130
E	-16.6	-16.1	17.1	1.56	-2.7	-
C'	-16.4	-17.3	17.2	1.58	-2.9	260
D'	-15.5	**-14.1**	17.1	1.57	-2.6	110

*A: after 1st circuit synthesis, B: after 1st layout synthesis, C: after 2nd circuit synthesis with parasitic corners, D: after 2nd layout synthesis, E: after final detailed routing, C': after 2nd circuit synthesis without parasitic corners, D': after 2nd layout synthesis without device tuning. S11, S22 specs are for circuit/layout synthesis. Total current consumption is 8.2mA fixed after A. Runtime is measured on an average of 10 Sun Blade100's for A, C, C' and one Sun Ultra 10 for B, D, D'.

Table 2: Synthesis With/Without Parasitic Corners

	With Parasitic Corners			Without Parasitic Corners		
Specs	Nom. Point	Corner A	Corner B	Nom. Point	Corner A	Corner B
S11(dB)	-17.1	-16.0	-17.6	-16.4	**-14.5**	-15.6
S22(dB)	-16.3	-19.5	-15.3	-17.3	-15.8	**-13.9**

Table 3: Quadratic Macromodel: ranges and errors

Upper/Lower Bounds of RF Net Lengths and Tunable Device Parameters								
Nets/Devs	Net0	Net1	Net2	Net3	Net4	Net5	Net6	Net7
Low (μm)	20	30	30	20	60	60	30	30
Up(μm)	40	90	90	80	180	150	90	90
Nets/Devs	Net8	Net9	Q0(el)	Q1(el)	C0(w)	L0(d)	L1(d)	
Low(μm)	10	30	72	66	17	310	130	
Up(μm)	30	90	84	78	19	330	150	
Quadratic Macromodel Errors								
Performances		S11	S22	S21	NF	IIP3		
Mean Error		0.7%	1.5%	0.11%	0.03%	0.5%		
Max Error		1.8%	2.6%	0.23%	0.08%	1.2%		

Table 4: Performance Compensation by Device Tuning

		S11(dB)	S22(dB)	S21(dB)	NF(dB)	IIP3(dBm)
Placement. 1	before	-15.4	**-13.9**	17.3	1.59	-3.2
	after	-15.1	-15.3	17.5	1.59	-3.6
Placement 2	before	**-14.2**	**-14.8**	16.4	1.55	-2.8
	after	-15.7	-17.7	16.9	1.57	-3.7
Device Tuning		Q0 (el)	Q1(el)	C0(w)	L0(d)	L1(d)
Place. 1(before/after)		72/72	**72/66**	18/18	320/320	140/140
Place. 2(before/after)		**72/78**	**72/66**	18/18	**320/330**	**140/130**

Macromodeling is performed with 200 training and 50 checking samples. The model ranges are listed in Table 3. L2 is not included because it is too sensitive. With a quadratic model, the overall mean errors are less than 2% and worst case errors less than 3%, which demonstrate the practicality of this strategy. Table 4 shows two

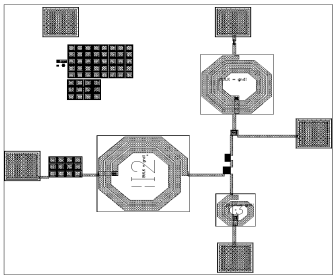

Figure 4. LNA Placement With Global Routing of RF Nets.

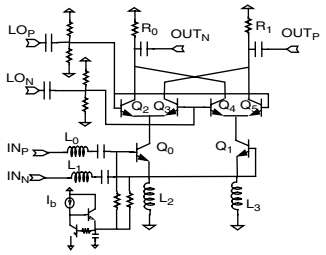

Figure 5. Example Circuit: 4GHz SiGe Mixer.

Table 5: Mixer Synthesis Results*

	S11 (dB)	NF (dB)	Gain (dB)	IIP3 (dBm)	Icc (mA)	Runtime (s)
Specs	-16/-15	6	12.5/12	-3	7	-
A	-20.5	5.2	12.8	-2.3	5.2	8,600
B	**-14.8**	5.5	**10.3**	-1.7	5.2	570
C	-16.4	5.6	12.6	-1.9	5.8	2,700
D	-15.8	5.5	12.2	-1.7	5.8	330
E	-16.1	5.5	12.2	-1.7	5.8	-

*A-E and runtime condition are the same as for Table 1.

example placements before and after device tuning is performed. It shows device tuning can compensate for large degradations even with such small tuning ranges. A second layout synthesis is performed and the results are listed in Table 1 Row D. For comparison, a separate layout run is performed without device tuning. The results are shown in Table 1 Row D' with the S22 spec violated. Experiments show that, for the LNA, with a conventional flow, multiple iterations are needed to achieve parasitic closure.

The final placement with global routing is shown in Figure 4. Note that there is a 60μm halo around inductors as required by the design rules. Final detailed routing is performed manually following the global routing and parasitic closure is maintained as shown in Table 1 Row E. The final layout is about 0.8mm by 0.9mm excluding pads.

5.2 A 4GHz SiGe Mixer

Now we turn to a bigger design which is a 4GHz SiGe mixer as shown in Figure 5. It has 7 independent design variables, 30 devices and 21 RF nets. LO nets are identified as noisy nets and are kept away from the input/output nets. Synthesis results for each synthesis stage are listed in Table 5. Parasitic corners for S11 and Gain are included in the resizing run (Row C). A quadratic macromodel is built for the last layout run (Row D). Synthesized final placement and global routing is shown in Figure 6. The layout size is 0.95mm by 1mm.

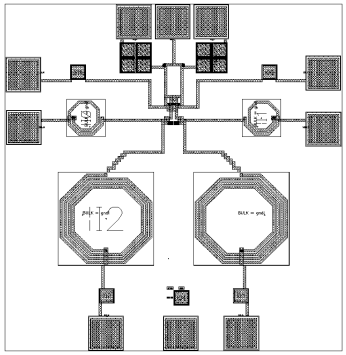

Figure 6. Mixer Placement With Global Routing of RF Nets.

6. CONCLUSIONS

We proposed a circuit and layout synthesis flow for RF integrated circuits. The concept of statistical parasitic corners is introduced to ensure that circuit synthesis results are parasitic robust. Device tuning is utilized during layout synthesis to maximize layout flexibility and design convergence. Circuit macromodels in terms of both parasitics and restricted device tuning parameters are used in performance-driven layout synthesis. Device level placement with simultaneous incremental global routing allows accurate performance estimations for RF layouts.

7. ACKNOWLEDGMENTS

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