A Communication-Theoretic Design Paradigm for Reliable SOCs

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ABSTRACT

Presented is a design paradigm, pioneered at the University of Illinois in 1997, for reliable and energy-efficient system-on-a-chip (SOC) in nanometer process technologies. These technologies are characterized by non-idealities such as coupling, leakage, soft errors, and process variations, which contribute to a reliability problem. Increasing complexity of systems-on-a-chip (SOC) leads to a related power problem. The proposed paradigm provides solutions to both problems by viewing SOCs as communication networks, and employs ideas from error-control coding, communications, and information theory in order to achieve the dual goals of reliability and energy-efficiency.

Categories and Subject Descriptors

B.8.1 [**Performance and Reliability**]: reliability, testing and fault-tolerance.

General Terms: Algorithms, Reliability.

Keywords: Low-power, system-on-a-chip, reliability, communications, coding.

1. INTRODUCTION

Power dissipation is a problem that concerns both microprocessors and communication systems. High power dissipation increases the substrate temperature of integrated circuits increasing leakage currents, reducing performance and battery life for mobile applications, and adversely impacts material reliability, thereby necessitating the use of complex power management systems and expensive packaging technologies. The power/performance problem has been worked on for a long time.

Complicating the power/performance problem is the recent emergence of noise and the dramatic increase in process variations in nanometer process technologies. Both, noise and process variations, result in logic errors resulting in system failure. In other words, there is a reliability problem as well.

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Unfortunately, all power/performance optimization techniques only aggravate the reliability problem. As an example, supply voltage scaling is a popular technique to reduce power but at the expense of noise-immunity. It is not possible to talk about low-power or high-performance design techniques without considering reliability. The coupling of reliability and power/performance issues has raised serious questions regarding our ability to design reliable and efficient (low-power/high-performance) computing systems in nanometer process technologies. This fact puts at risk, the affordability of microsystems and hence the ability of the semiconductor industry to extend Moore's law well into the nanometer regime.

We describe a *communication-theoretic* paradigm for the design of reliable and efficient system-on-a-chip (SOC) of the future. The design paradigm views integrated microsystems as miniature communication networks operating in the presence of noise. The paradigm was first proposed [1] in 1997 and has since developed into two distinct but related areas of research: 1) information-theoretic techniques for determining the lower bounds on energy-efficiency in the presence of noise, and 2) circuit, algorithmic noise-tolerance techniques for computation and communication. The proposed paradigm naturally leads to the concept of networks-on-a-chip. The 2001 and 2003 International Technology Roadmap for Semiconductors echoes the sentiments described in [1] by stressing the need for a communication-centric design paradigm for SOCs and error-tolerance as a design challenge. A tutorial article on the proposed communication-theoretic paradigm can be found in [2].

2. ACKNOWLEDGMENTS

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3. REFERENCES

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