Concept and Extraction Method of ESD-critical Parameters for Function-Based Layout-Level ESD Protection Circuit Design Verification

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Abstract - On-chip ESD (electrostatic discharging) protection is a challenging IC design problem. New CAD tools are essential to ESD protection design prediction and verification at full chip level. This paper reports a novel concept and extraction method of ESD-critical parameters for function-based layout-level ESD protection circuit design verification, which has been used to develop the first intelligent CAD tool of such kind. Design examples in 0.35µm BiCMOS are presented.

I. Introduction

In order to avoid ESD-induced damages, ESD protection circuits are required for practical IC chips [1]. As IC technologies continue to migrate into the very-deep-sub-micron (VDSM) region, on-chip ESD protection circuit design emerges as a major design challenge to IC designers, particularly for mixed-signal and RF ICs. One of the major problems facing IC designers is the lack of practical CAD tools dealing with the complex ESD protection design verification. As a result, the trial-and-error approach still dominates in ESD protection design practices.

The first critical mission of full-chip ESD protection design verification is at layout level because it is desirable for IC designers to conduct quick, yet sufficiently accurate verification after the physical design is completed. The key point in physical design verification is to check whether all the designed ESD protection structures (i.e., intentional ESD elements) are designed properly in layout and if there is any life-threatening parasitic ESD-type devices (i.e., parasitic ESD devices) existing in the core IC circuit being protected, which often lead to early ESD failures. Unlike the traditional IC DRC and LVS checking, this layout-level ESD verification should cover much more sophisticated checking aspects associated with ESD protection operations.

Currently existing ESD protection design checking CAD tools offer only basic layout checking functions, e.g., layer spacing and path resistances, very similar to the ordinary IC DRC checking operation [2-4]. Reference [2] discussed an ESD design rule-checking program and provided several ESD DRC rules. Reference [3] reported an ESD design error-checking tool that performs metal bus resistance and diffusion checking. Reference [4] is another DRC checker to verify ESD/latch-up reliability. While such dimension checking is important, it provides limited benefits to practical ESD protection design verification.

This paper presents a novel ESD-critical parameter concept, discusses the extraction method of ESD-critical parameters from the layout and its applications. The paper is organized as follows. Section II reviews the basic ESD protection operation. Section III discusses the concept of ESD-critical parameters and extraction method. Section IV describes the utilization of the new concept in a new layout-level ESD design verification CAD tool. Section V offers several design examples.

II. ESD Protection Operation

Fig. 1 illustrates the typical I-V characteristics for ESD protection structures, where the ESD protection unit is triggered on under ESD stress, driven into a deep snapback region to form a low-impedance discharging path and to clamp the pad voltage to a low holding level. Apparently, the critical design parameters for an ESD protection structure include the triggering point (V_t1, I_t1), holding point (V_h, I_h), discharging resistance (R_{D0}) etc. Whatever ESD protection solutions used, these important parameters are universal to describe the behavior of them under ESD stresses.

III. Concept and Extraction Method of ESD-Critical Parameters

The goal of the layout-level ESD protection design verification is to locate critical ESD devices (critical ESD devices are those intentional or parasitic devices having a chance to be turned on under ESD stresses) in the layout and/or generate the input deck for schematic-level simulation. Some simple CAD tools were reported [2-4] to perform ESD design verification based on some basic layout checking functions, such as critical layer spacing checking and worst-case path resistance estimation. While such basic layout checking is important, it is only an over-simplified ESD DRC checking routine.

Upon the observation that ESD-critical parameters can be used to describe the behavior of all kinds of ESD devices, intentional or parasitic, this work propose to perform layout-level verification by quantitatively checking critical ESD parameters along with the connections between different ESD devices to locate critical ESD devices.

A. New Concept of ESD-Critical Parameters

ESD-critical parameter is a concise, but quantitative parameter matrix that describes the basic ESD protection
operation. As discussed in the previous Section, these ESD-critical parameters should include important ESD operational features such as triggering point \((V_{th}, I_{th})\), holding point \((V_h, I_h)\) and discharging impedance \((R_{on})\) etc. They determine where/when an ESD structure is turned on; how good the pad voltage clamping is; how efficient the ESD current may be discharged and how much ESD stress may be handled. In addition to these universal parameters, a few structure-specific parameters should also be included. For example, for BJT and MOSFET based ESD protection structures, the effective current gain, \(\beta\) is an ESD-critical parameter because it determines how efficient the BJT is, which is the fundamental ESD mechanism in these structures. For SCR-type ESD protection structures, the \(\beta\)-product, i.e., \(\beta_{NPN}\beta_{PNP}\), of their parasitic NPN and PNP BJTs is clearly an ESD-critical parameter because if it is less than one, they will never have a chance to be turned on [1].

### B. Extraction of ESD-Critical Parameters

Regarding ESD parameter extraction, most existing works [1,5] do the job by modeling devices and extracting parameters from measurements. While these works intend to obtain more accurate results by taking into consideration of more effects or retrieving parameters from measurements, the procedure are too complicated to be used at layout level. In our work, however, ESD parameters are extracted directly from layout and technology data, based upon some proper approximations of device physics and circuit analysis equations. The reason is that our aim is to conduct a quick, yet sufficiently accurate ESD design verification at layout level. The task of getting more accurate ESD behavior at the chip level will be left for the schematic-level simulation – an on-going research topic. Furthermore, our practical design implemented in a commercial 0.35\(\mu\)m BiCMOS technology has verified the reasonable accuracy of our extraction equations as described in Section V.

### IV. Use ESD-Critical Parameters for Function-Based Design Verification at Layout Level

#### A. Comprehensive Layout-Level Design Verification Based Upon the Concept of ESD-Critical Parameters

Success of ESD protection design depends on the whole IC chip, which shows the mutual interactions between the ESD protection structures and the core circuit. Further, in addition to characterizing individual ESD devices, ESD-critical parameters can also be used to characterize the operation of an ESD protection network consisted of many ESD protection devices. For example, if ESD devices A and B are connected in series, the total \(V_{th}\) of the combined A+B ESD network is the sum of \(V_{th}\) of A and B. Using the new concept of ESD-critical parameters, some comprehensive layout-level checking tasks, listed below, can be readily addressed.

#### A1. To Locate Critical ESD Devices

Numerous parasitic ESD devices may be extracted from a layout file, of which only a handful of them might be relevant to ESD operation. By investigating ESD-critical parameters extracted and connections between ESD devices, critical ESD devices can be located in the layout.

#### A2. To Find the Discharging Path Between Two Pads

To check if an IC chip would fail during an ESD stress appearing between two given bonding pads, it is necessary to find and analyze the discharging path between them. This problem can be addressed through first finding all paths between the given pads, then calculating ESD parameters for each path and pinning-down the one most-likely ESD discharging path. This idea can be further used by a standard ESD zapping test simulator, e.g., HBM [1] testing, to examine if an IC chip would fail under a standardized ESD stressing test applied between any two pads.

### B. ESDInspector, A New CAD Tool for ESD Protection Physical Design Verification

As a complete solution, the new concept of ESD-critical parameters and its extraction method described above was applied to the first smart CAD tool for whole-chip ESD protection circuit, entitled ESDInspector. The details of the ESDInspector CAD tool will be presented in a separate paper. Fig. 2 shows the flow chart of the ESDInspector, which consists of an ESD device extraction engine to extract all intentional and parasitic ESD devices based on a subgraph isomorphism algorithm [6]. The ESD-critical parameter extraction engine, marked by a double-lined box, calculates all related ESD parameters discussed previously. Currently, extraction equations for 8 typical ESD protection devices are provided. Any new ESD parameter equations can be defined as a new ESD protection structure is devised.

### V. Design Examples

The new concept of ESD-critical parameters and extraction method were verified in several ESD protection design examples in a 0.35\(\mu\)m BiCMOS technology.

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**Fig. 2 A flow diagram for the ESDInspector.**
A. Diode ESD Protection Device

The diode features a simple turn-on, instead of a snapback, I-V curve. Hence, its holding point is the same as its triggering point. According to basic junction equations, 
\[ V_{t1} = V_{on}, \quad \text{and} \quad I_{t1} = I_{s} \exp(qV_{on}/nKt). \]

B. GGNMOS (ground-gate NMOS) ESD Protection Device

The cross-section of a ggnMOS is illustrated in Fig. 3(a). The principle of it follows. As a positive ESD transient appears at an I/O pad, i.e., D, the DB junction is reversed biased until breakdown. Avalanche current flows through the parasitic resistance \( R_b \) and forward turn-on the BS junction, hence, triggers the parasitic NPN transistor Q and forms a discharging path. In our implementation, we define the triggering as the point where Q turns on. The ESD-critical parameter equations for ggnMOSs are given as,
\[ I_{t1} = V_{on} / R_b, \quad \text{and} \quad V_{t1} = V_{BR} + V_{on} + I_{t1} \cdot R_c, \]
where \( V_{BR} \) is the breakdown voltage of the BS junction, and \( R_c \) is the collector resistance of the transistor Q. And \( I_{t1} = \beta I_{t1} \) and \( V_{t1} = V_{ce(sat)} + R_c \cdot I_{t1} \) where \( \beta \) and \( V_{ce(sat)} \) are current gain and of the saturated C-E voltage of Q, respectively.

Table I shows the extracted and measured data for ESD-critical parameters of two ggnMOSs.

C. SCR (silicon controlled rectifier) ESD Protection Device

SCR, and other advanced SCR-like devices, such as MVSCR (medium-voltage SCR) and LVSCR (low-voltage SCR), are regarded as the most efficient ESD structures.

C1. Triggering Point Calculation

The operation of the SCR before the triggering point can be described as a pair of twoBJT transistors, i.e., a vertical p-n-p Q1 and a lateral n-p-n Q2, as shown in Fig. 3(b) [7]. The triggering happens at the breakdown of the N-well/p-substrate junction [1]. Due to the nonlinear current gain behaviors, it is virtually impractical to find an exact expression for the \( I_{t1} \). However, a reasonably good estimation can be obtained by assuming that one of transistors turns on first and defining triggering as the point where the other one turns on [8]. Thus, the triggering can be divided into two types: i.e., lateral triggering or vertical triggering, whichever occurs first. For the lateral triggering,\[ I_{t1} = V_{on}/\alpha_2 R_{nw} \quad \text{and} \quad V_{t1} = V_{BR} + V_{on} + I_{t1} R_{c2}, \]
where \( \alpha_2 \) and \( R_{c2} \) are the current gain and collector resistance of Q2, and \( V_{BR} \) is the breakdown voltage of the N-well/p-substrate junction.

C2. Holding Point Calculation

After triggering, the SCR acts like a p-i-n diode [7]. If \( n>p>n_{i} \), where \( n \) and \( p \) are carrier concentration of the N+ region and P+ region respectively, the \( I_{h} \) can be written as,
\[ I_{h} = q(\mu_n + \mu_p) n E A + V_{br} = V_{on}(Q2) + V_{ce(sat)}(Q1) + I_{h} R_{c1} \]
where \( E \) is the average electric field and \( A \) is the junction area of the p-i-n diode.

C3. MVSCR and LVSCR

|| Devices | \( V_{t1} \) (V) | \( I_{t1} \) (mA) | \( V_{h} \) (V) | \( I_{h} \) (mA) |
|---------|-------------|-------------|-------------|-------------|
| SCRs    | CAD Test   | CAD Test   | CAD Test   | CAD Test   |
| ggnMOS1 | 9.53       | 10.4       | 22.9       | 68.5       | 9.11       | 8.22       | 251.7      | 117        |
| ggnMOS2 | 9.39       | 9.58       | 18.3       | 6.88       | 7.61       | 6.88       | 201.3      | 76.3       |

Since \( V_{t1} \) of the SCR is generally too high, MVSCR and LVSCR were devised for lower \( V_{t1} \) [1]. The \( V_{BR} \) of MVSCR is reduced by replacing the N-Well/p-Substrate junction with a N-Well/P+ junction. The reduction of \( V_{t1} \) of LVSCR is realized by using a trigger-assisting ggnMOS device. After triggering, both MVSCR and LVSCR behave almost the same way as an SCR device. Table II shows the extracted and measured ESD-critical parameters for SCR, MVSCR and LVSCR with the same dimensions.

VI. Conclusions

In conclusion, we presented a novel concept of ESD-critical parameter and its extraction method, which were applied to develop a smart layout-level ESD protection circuit design verification CAD tool. Practical design examples using the new concept, implemented in 0.35μm BiCMOS technology, were discussed.

References