A Dual–Band Switching Digital Controller for a Buck Converter

Martin Yeung–Kei Chui, Wing–Hung Ki and Chi–Ying Tsui

Department of Electrical and Electronic Engineering
The Hong Kong University of Science and Technology
Clear Water Bay, Hong Kong SAR, China
Fax: (852) 2358–1485, email: eemartin@ee.ust.hk

Abstract — A 0.6µm CMOS integrated digital PID controller for a buck converter is fabricated and tested. It consists of: (1) a VCO driving a counter to serve as an ADC; (2) a PID compensator that employs a programmable integration time for enhancing accuracy and stability; and (3) a dual-band switching PWM generator with a modified tapped delay line for better output resolution and area efficiency. The converter switches at 1MHz, while the tracking time is 50µs for a step change of 1V.

I. Converter Architecture

Early digital implementation of controllers for switching converters used a bulky discrete-component approach. With the advance of VLSI technology, digital controllers can be integrated with the power stage, and the integrated converter is more programmable and cost-effective. Fig.1 shows the architecture of our proposed digital controller. The converter output voltage \( V_o \) compares with the reference voltage \( V_{ref} \) to produce an error voltage \( V_e \) at the output of the error amplifier to drive a VCO (voltage-controlled oscillator) that exhibits an approximately linear voltage-to-frequency characteristic. The frequency range of the VCO can be relaxed because it deals with the error voltage rather than the whole range of the output voltage. The output of the VCO serves as a clock signal to a counter, which generates a binary number \( N \) as output, thus serving as an analog-to-digital converter. During start up, the \( v_\) and \( v_ \) inputs of the error amplifier is momentarily shorted, which represents a zero error. The output of the counter is then the zero-error reference \( N_0 \). During normal operation, \( N_0 \) is subtracted from \( N \) to produce the digitized error signal \( e(n) \), which is then sent to the PID compensator that implements the Proportional, Integral and Derivative actions [1]. The output of the compensator \( d(n) \) is sent to the PWM generator, which converts the binary number into an analog duty ratio to drive the main switch of the buck converter.

![Simplified schematic of buck converter with digital controller](image)

II. Special Features and Functional Blocks

Dual band switching: For a converter with a fixed output \( V_o \), the output voltage of the error amplifier only varies within a small range around \( V_e \). It would be a waste to quantize the full range of \( V_e \). In our design, the voltage of 0V to \( V_e \) is divided into the Low Band (0V to \( 2V_e/3 \)) and the High Band (\( V_e/3 \) to \( V_e \)). A Band Selection signal “BS” chooses the desired operating band. The effective resolution is thus increased. For a 6-bit quantization of the band voltage \( V_e \), which is equal to \( 2V_e/3 \), an equivalent resolution of \( V_e/96 \) is obtained. Note that the two bands overlap to avoid numerical saturation in the PID controller.

VCO design: The design of the VCO uses a \( R\text{-}C\text{_}T \) ramp generator. An inverter chain replaces the conventional hysteretic comparator to obtain a high frequency ramp.

PID controller: The PID compensator has a resolution of 6 bits. The digital duty ratio \( d(n) \) is composed of the Proportional, Integral and Derivative actions based on \( e(n) \). Multiplication and division are implemented by left and right shift operations, respectively. The stability of a buck converter is determined by its loop gain \( T(s) \), which consists of the frequency responses of the power stage \( H(s) \) and the PID compensator \( A(s) \):

\[
T(s) = A(s)H(s) = \frac{1}{s/K_i} \left( 1 + \frac{G_p}{K_i} s + \frac{G_{i}T/K_i}{1 + (L/R)s + LC^2} \right).
\]

where \( L \), \( C \) and \( R \) are the inductor, capacitor and load resistance values of the buck converter, respectively. \( G_p \) and \( G_{i} \) are the gains of the \( P \) and \( D \) control respectively, and \( T \) is the sampling time. \( K_i = G_i/T \) is the effective integral gain, where \( G_i \) is the integral gain. The complex zeros of the PID controller is designed to achieve pole-zero compensation for the complex poles of the power stage, and the bandwidth of the control loop is thus increased.

Programmable \( T \): For stability, the integral gain is usually small (\( G_i << 1 \)). Due to bit limitation, a quantized error \( e(n) < 1/G_i \) will be rounded off to zero after a right-bit shift operation. The steady-state error increases with the decrease in \( G_i \). To cater for both situations, a longer integration time can be used together with a larger \( G_i \), thus keeping \( K_i = (G_i/T) \) constant, where \( T \) is the integration time, i.e., the sampling time of the integral control.

PWM generator: A tapped delay line architecture is commonly used in the implementation of a PWM generator, and our design employs a delay line reuse technique to reduce the number of delay elements needed. A 32-stage delay line is looped three times in one switching cycle, and an equivalent of 96 taps can be obtained. When the output voltage is in the Low Band (\( BS=0 \)), the multiplexer of the PWM generator output is enabled at the first or second loop, and the digital word generated by the PID controller maps to the duty ratio of 0 to 2/3. The controller can thus regulate the output voltage from 0 to 2/3\( V_e \). Similar action applies if \( V_e \) falls in the High Band, with a regulation range of 1/3\( V_e \) to \( V_e \).

III. Experimental Results

A buck converter with a digital controller was fabricated in a 0.6µm CMOS technology (Fig.2). The die area is 1.8×2.1mm², and the control circuit measures 0.6×1.3mm². The converter switches at 1MHz with a 3.3V supply, while the oscillation range of the VCO is 10MHz to 80MHz. A 47µH inductor is used and the output capacitor is 2.2µF. High efficiency is obtained over a wide operating range and a maximum efficiency of 92% is achieved. Fig.3 shows the Low Band regulation from \( V_o = 0V \) to 2V. Clamping occurs when the target voltage is set out of the operating region. The High Band

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regulates similarly and is not shown. Fig.4 shows that the output could track a change in an input voltage of 40mV, comparable to the theoretical 34mV of 1 LSB using the dual-band scheme. Fig.5 shows the transient response of the converter output by programming the integration time. Large integration time decreases the effective integral gain ($K_i$), and the system stability is maintained without increasing the steady-state error. Fig.6 shows the step-up transient response in the Low Band, with a change in $V_{ref}$ of 0.5V to 1.5V. A tracking time of 50 $\mu$s was achieved.

IV. Conclusions

An integrated digital controller for DC-DC switching converters is fabricated and tested. The dual-band switching scheme improves the effective resolution of the digital controller. The programmable integration time technique enhances the system stability without increasing the steady–state error. Table 1 compares the performance of the proposed digital-control regulator with prior arts. It shows that this design has better dynamic performance and a wider output voltage range.

V. References


<table>
<thead>
<tr>
<th>Tracking Speed</th>
<th>Output range @ supply voltage (V)</th>
<th>Controller area @CMOS process</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wei [1]</td>
<td>~1ms/V</td>
<td>1.1–4.4@5 N/A</td>
</tr>
<tr>
<td>Ichiba [2]</td>
<td>180µs/0.9V</td>
<td>1.4–2.5@3 0.5mm²@0.3 µm</td>
</tr>
<tr>
<td>Kim [3]</td>
<td>80µs/–1V</td>
<td>1.1–2.3@2.5 0.35mm²@0.25µm</td>
</tr>
<tr>
<td>Hiraki [4]</td>
<td>400µs/0.2V</td>
<td>1.3–2.2@3.3 0.42mm²@0.2µm</td>
</tr>
<tr>
<td>Dancy [5]</td>
<td>100µs/1V</td>
<td>N/A</td>
</tr>
<tr>
<td>Namgoong [6]</td>
<td>&lt;6ms/V</td>
<td>1.5–3.5@5 N/A</td>
</tr>
<tr>
<td>This Work</td>
<td>50µs/V</td>
<td>0.2–3@3.3 0.78mm²@0.6µm</td>
</tr>
</tbody>
</table>

Fig.2 Chip micrograph

Table 1. Comparison with prior arts

Fig.3 Low Band regulation region

Fig.4 Smallest distinguishable transient step

Fig. 5 Transient response with different integration times

Fig. 6 Transient response for a $V_{ref}$ step of 0.5V to 1V