DEPOGIT: Dense Power-Ground Interconnect Architecture for Physical Design Integrity

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Abstract - In recent deep submicron VLSI design, signal integrity (SI) and power-ground integrity (PGI) have become very important to design in a short time. As a solution, we propose DEPOGIT, which is a new dense power-ground interconnect architecture that realizes more robust physical design integrity. This architecture is a method of running both the power and ground wires adjacent to the signal wires. This provides not only the general shielding effect but also explicit decoupling capacitance (decap) by means of the wires. Using this architecture also guarantees regularity, thus reducing manufacturing variations in interconnects.

As a result of quantitative analysis performed using 90 nm technology node, we demonstrate that high-quality decap of over 50 nF in a 10 mm square chip can be obtained, the resistive IR-drop can be less than 20% of that of a conventional power grid, transient peak noise can be reduced by about 80%, and the inductive crosstalk effect of the signal wire can be greatly reduced.

I. INTRODUCTION

Along with the scaling of process technology, interconnect dimensions are becoming finer and higher operating frequencies are being used. Today, the main issues in deep submicron VLSI design are signal integrity (SI) and power-ground integrity (PGI) problems. The principal SI problem is that crosstalk noise due to interference between adjacent wires causes delay fluctuations when the signals in the wires change simultaneously. Several techniques such as pseudopin assignment [1], buffer insertion [2], and shielding [3] are applied in order to preserve SI. The major PGI problems are, first, device switching and the resistance (R) of a power bus cause DC IR-drop, and second, RLC, including the inductance (L) and capacitance (C) of the power bus, generates ΔV noise, causing increased signal delay. Several methods are used to avoid these PGI problems, such as reducing the pitch of a power mesh grid, increasing the width of power and ground buses, and inserting decoupling capacitance (decap).

Important issues in timing convergence include design for manufacturability (DFM) and layout parasitic extraction (LPE). Regarding DFM, post-layout processes such as chemical-mechanical polishing (CMP), dummy-fills and optical proximity correction (OPC) are carried out in order to improve the planarization and critical dimension control of interconnects. Regarding LPE, in order to achieve higher accuracy, an interconnect library containing a large number of wire structures is generated using an electro-magnetic field solver. In addition, the effect of inductance at high frequency cannot be ignored, and so accurate extraction of it is necessary. However, because interconnect structures are becoming complicated and because 3 sigma variations of interconnect dimensions now exceed 15% [4], no further improvement in accuracy can be expected merely by using a library. Libraries yield iterative analysis, repair and verification loops, thus greatly increasing high-performance system-on-chip (SoC) turn-around time.

Dense wiring fabric (DWF) [5-7] has been offered to solve these issues. Figure 1 illustrates the DWF structure which all signal (S) wires are located between the power (P) and the ground (G) wires. As a result of the shielding effect, delay fluctuations and glitch noise due to capacitive and inductive crosstalk in the signal can be avoided, and also parasitic extraction using regularity can be facilitated. However, DWF is focused on the effect of SI and regularity, and also no mention is made on PGI. This structure makes a certain contribution to improved resistivity of the power supply network, but is ineffective for generating decap.

Traditional power supply networks have been designed in view of static DC analysis of IR-drop. However, operating frequency has been increasing of late, and furthermore it has recently become necessary to carry out dynamic analysis in terms of RC response. Thus, not only wire sizing but also inserting decap in proximity to the noise source are required. With conventional power supply networks, however, abrupt large current flows in them produce on-chip L di/dt noise. The ratio between power supply voltage and L di/dt noise due to inductance tends to be \( (L \frac{di}{dt})/V_{dd} \propto L \cdot P_c \cdot f / V_{dd}^2 \) [8]. Here, \( P_c \) is the chip power consumption, \( f \) is the operating frequency, and \( V_{dd} \) is the power supply voltage. According to the 2002 International Technology Roadmap for Semiconductors (ITRS) [9], even for a low power SoC, \( f \) indicates a ×1.5 tendency and \( V_{dd} \) a ×0.8 tendency, and \( P_c \cdot f / V_{dd}^2 \) increases about ×2.3 for each generation. The technique to avoid \( L \frac{di}{dt} \) noise is the same as that used to avoid dynamic IR-drop, and involves inserting decap. In other words, the key to solving this
problem is inserting high quality, large decoupling capacitance.

The existing optimal decap allocation is done during the floorplan and cell layout phase, with the pre-estimated power consumption and the placement of MOS decap determined prior to wiring [10, 11]. However, these methods do not consider the decap that is generated by wire coupling capacitance after the final routing. Also, because of the restrictions incurred due to inserting decap in proximity to the noise source, the area cost of decap insertion, which is sometimes necessary at bottlenecks in the floorplan, can be extremely high, such as in the case shown in Fig. 2. The shaded areas in Fig. 2 show the decap located in the vicinity of the macro block.

The problems of SI, PGI, DFM and LPE have been discussed separately. We propose a new interconnect architecture for physical design integrity, which solves the above problems simultaneously.

The remainder of the paper is organized as follows. The basic construction and the advantages and penalty of the new interconnect architecture that we propose are described in Section II, its features are clarified by quantitative analysis and verification in Section III, and finally a summary is given in Section IV.

II. DENSE POWER-GROUND INTERCONNECT ARCHITECTURE

A. Basic Concept

![Fig. 3. Basic structure of new interconnect architecture.](image)

We propose a dense power-ground interconnect (DEPOGIT) architecture. This concept basically consists of a \(PGP\) … pattern, as shown in Fig. 3. Here, \(P\) indicates the power wire and \(G\) indicates the ground wire. A large amount of decap can be created by employing a \(PG\) pattern as much as possible. Each signal wire is basically located between power and ground wires. The width and spacing of the signal wires can be selected freely, however, if the use of a grid router is assumed, and the width and spacing are varied according to the grid pitch. Each power wire and each ground wire should as much as possible be connected by via holes between the same or different layers. Even though any layer can be a candidate for DEPOGIT, the first or second metal layer is often used for local interconnects, so it is better to use layers other than those used in the current cell-based design.

B. DEPOGIT Structures

Table I shows a combination of several wires in the case where signal wires are passed through the basic structure. Here, we newly introduce the concept of a tile. The tile is a unit of the repeated pattern of \(PGS\). Increasing the thickness of the power supply wire at the outermost part of the tile, for example, enables it to share the power supply bus that is ordinarily intended for supplying power, and thus enables electrical and magnetic interference to be minimized between tile units.

Here, consider the combinations of power-ground and signal wires as shown in Table I. Basically the signal is shielded with a pair of \(PGs\), which makes it possible to achieve decoupling effect. The number of signals among the \(PG\) wires is determined depending on how sensitive the signals are to each other. For example, if the automatic router can find two signal pairs that could be adjacent and that are shielded by the \(PG\) from other sensitive signals in each track in the whole chip, the overall signal ratio (density) becomes equal to 50%, which is the same as the traditional shielding structure. We can increase the amount of added decap by increasing the number of adjacent signals with the same signal ratio, e.g., \(3S\) or \(4S\) in Table I.

**TABLE I**

<table>
<thead>
<tr>
<th>Signal Ratio</th>
<th>1S</th>
<th>2S</th>
<th>3S</th>
<th>4S</th>
</tr>
</thead>
<tbody>
<tr>
<td>2/3</td>
<td>PG</td>
<td>PG</td>
<td>PGS</td>
<td>PGS</td>
</tr>
<tr>
<td>1/2</td>
<td>PG</td>
<td>PG</td>
<td>PGP</td>
<td>PGP</td>
</tr>
<tr>
<td>1/3</td>
<td>PG</td>
<td>PG</td>
<td>PGPG</td>
<td>PGPG</td>
</tr>
</tbody>
</table>

Another advantage of the tile structure is as follows. Vacant track segments occur when the signal wire is shifted to another layer by means of a via hole midway along the tile. In this case, 50% wire density, which is another feature of DWF, is not guaranteed. If the tile structure is used, adding an extended power or ground wire segment having
the same width as that of the signal wire, from the outer border \( P \) or \( G \) of the tile concerned, enables near-perfect 50\% wire density to be achieved. This dense regular DEPOGIT tile can improve the extraction accuracy and reduce random variations, which are the merits of high density. Details are described in Section III.

C. Advantages and Penalty

The advantages and penalty of the DEPOGIT architecture are briefly as follows.

1. Advantages
   • Improvement of PGI:
     It is possible to generate explicit decap by using \( PG \) pair wires, and reduce dynamic power supply noise.
   • Improvement of SI:
     Capacitive and inductive crosstalk noises are reduced due to the shielding effect.
   • Improvement of DFM:
     Uniformity of the wiring improves the local and global density. Thus it eliminates the need of dummy metal insertion for density correction.
   • Improvement of PE accuracy and speed:
     The fact that no post-layout dummy metal is needed eliminates the uncertainty of extraction caused by floating metal, and the regularity reduces random interconnect variations and the number of structure patterns, permitting high-accuracy and high-speed extraction.

2. Penalty
   • Increase in chip area:
     When a signal wire is completely surrounded by a \( PG \) pair for each signal wire, a chip area or the number of layers increases. However, it is possible to reduce the area penalty by not using the bottom two layers, taking into account the wire utilization rate, and in the case of a non-critical wire, by inserting a \( PG \) pair every few signal wires.

Our proposed architecture provides flexibility in the use of layers and combinations of \( PGS \) patterns by trade-off of advantages and penalty corresponding to the needs.

III. PHYSICAL DESIGN INTEGRITY IMPROVEMENT

In this section, we analyze the advantages and penalty of DEPOGIT quantitatively. The most significant advantage in comparison with previous methods such as DWF is the generation of enormous decoupling capacitance, which makes it possible to obtain robust power supply noise immunity as a result. Although the signal crosstalk avoidance and the wire regularity produce almost the same effects as those of a general shielding, they also provide a total solution for physical design integrity, as we will make clear. We use the interconnect parameters as shown in TABLE II based on the 90 nm technology of ITRS for detail analysis.

A. Generation of Enormous Decoupling Capacitance

We analyze the amount of the decoupling capacitance in our proposed method. Figure 4 shows the predicted decap value at several ratios of signal to total wires, the patterns of which are illustrated in Table I. We assume that the die size is 10 mm square with 9 layers and that the wires have the minimum width and spacing. The capacitances between the \( P \) and \( G \) wires were obtained by using a field solver [12]. As shown in Fig. 4, for example, even if we restrict the signal ratio to 0.5, which is equal to the traditional shielding structure, we can obtain additional capacitance from 10 nF to 100 nF. If we apply the DEPOGIT only from M3-M9, the capacitance value will be 70 nF. This covers 43\% of the decap value required for current microprocessors, i.e., 160 nF [13].

![Fig. 4. Predicted decap values of DEPOGIT.](image-url)

The time constant of well decap is very large [10], but that of DEPOGIT is very small. Also, as the thickness of gate oxide is scaled, the gate leakage current increases [14], and in order to meet severe low power target, it is necessary to partially use thick-oxide decap. In the case of thick-oxide, the capacitance obtained per unit area decreases, necessitating an even greater chip size. In the future high-performance LSI design, we cannot expect a sufficient contribution from the well capacitance, so the needs of capacitance between the \( P \) and \( G \) wires obtained using this method will be significant.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of metal levels</td>
<td>9</td>
</tr>
<tr>
<td>Resistivity (( \mu \Omega \cdot \text{cm} ))</td>
<td>2.2</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>3.1</td>
</tr>
<tr>
<td>Minimum width (( \mu \text{m} )) (Global)</td>
<td>0.28</td>
</tr>
<tr>
<td>Minimum spacing (( \mu \text{m} )) (Global)</td>
<td>0.28</td>
</tr>
<tr>
<td>Metal thickness (( \mu \text{m} )) (Global)</td>
<td>0.4305</td>
</tr>
<tr>
<td>Height (( \mu \text{m} )) (Global)</td>
<td>0.3895</td>
</tr>
</tbody>
</table>

**TABLE II**

**INTERCONNECT PARAMETERS USED FOR ANALYSIS.**
B. Power-Ground Integrity Improvement

Here, we analyze the effect of the DEPOGIT architecture on power supply noise. In general, there are two models for packaging a VLSI. One is the model for the power supply from the peripheral pad of a wire-bonded IC. The other is for the flip-chip-bonded array I/O for a high-frequency IC.

First, we analyze the resistive IR-drop for a chip with 10 mm square in the case of wire bonding. Suppose the traditional power grid structure uses the top two metal layers with 50-µm pitch. We define two types of wire width. Type 1 is 2-µm power wire width and type 2 is 5 µm. We use the current noise source that is equivalent to the one that causes 10% IR-drop in type 1 at $V_{dd} = 1$ V. Figure 5 compares the proposed DEPOGIT and a traditional structure. The figure shows that the DEPOGIT has very low resistivity and high immunity to the IR-drop. For example, the IR-drop in DEPOGIT with less than 0.7 signal ratio is less than 2% IR-drop, where in the traditional structure it is 10%.

Next, we analyze the L di/dt noise. An analysis of power supply noise is carried out based on the assumption of a flip-chip for high-frequency applications. In the traditional method, the top two layers consist of the power wiring. The width is 2 µm and the grid pitch is 100 µm, and the pad pitch is assumed to be 400 µm. Figure 6(a) shows the equivalent circuit of this structure. In the proposed method, M3-M9 is wired at high density with minimum spacing, one out of every three wires is a signal wire like PGSPGS, and the wire width used in the top two layers is 2 µm. Figure 6(b) shows the transient analysis waveform obtained when the wiring is represented as an RLC equivalent circuit and a triangular wave current source is applied to the grids as in Fig. 6(a). The analysis shows that in the traditional grid mesh, 3% ΔV noise occurs in the RC extracted circuit and 5% noise occurs in the RLC extracted circuit. With the DEPOGIT structure, the noise is reduced to 1% in the RLC extracted case.

C. Signal Integrity Improvement

At GHz frequency operation, in the case of wide wiring such as the clock wiring, the delay fluctuations due to inductance are not negligible. Also, when multiple signal wires are switched in the same direction, as in the case of a bus structure, we cannot ignore the effect of glitch noise due to inductive crosstalk resulting from a magnetic field generated by the large current flowing through a victim wire. Here, the effectiveness of prevention of inductive crosstalk using the DEPOGIT structure is analyzed.

We use a 32-bit bus structure for the crosstalk analysis. We assume the frequency is 4 GHz, the rising time is 25 ps, the driver resistance is 50 Ω and the wire length is 1 mm. A comparison between the two structures was performed (Fig. 7). The structure of Fig. 7(a) uses the top two metal layers with 50-µm pitch and 2-µm width. The structure of Fig. 7(b) uses the top two metal layers with minimum pitch and minimum width.
The wire at the center of layer 7 is the victim (V) wire. All the other signal wires are aggressor (A) wires. Fig 8 shows the SPICE simulation result of the detailed ratio of glitch noise at the far end, as seen from the driver in the victim wire. As can be seen from the figure, the proposed method has high immunity to crosstalk noise.

\[ \text{DEPOGIT} \quad \text{Traditional} \]

**Fig. 8. Crosstalk analysis results.**

**D. Extraction Accuracy Improvement**

Another advantage of DEPOGIT is the improvement in regularity. In the case of the DWF structure, the signal wire is always shielded by PG, so the wiring density per unit area is 50%, which is the theoretical maximum value. Here, the via hole size is assumed to be no greater than the wire width, and also it is assumed that the wire width and spacing are the same. In actual routing, when we look at the specific layer, the direction of the signal wire changes when a via hole is put in the middle of the tile. This causes an empty track segment as shown in Fig. 9(a). If we define the utilization of routing resources as \( \alpha \), the wire density per unit area in the conventional structure is \( (1+\alpha)/4 \). Let us suppose that \( \alpha=50\% \) and that the wire density is 37.5%.

Here, as shown in Fig. 9(b), if the DEPOGIT structure is used, each side of a tile has a P or G segment. This makes it possible to achieve an average wire density of almost 50% by extending the wire from the endmost PG wires of the tile to the unfilled tracks.

Figure 9(c) shows the case where there is no PG shielding except for the endmost PG wire. In this case, the overhead of the wire resources is minimized but the regularity is dramatically improved. It is expected that this will be effective in minimizing interconnect process variations.

DEPOGIT requires no dummy metal filling, and also enables more uniform density to be obtained. In addition, the density and uniformity of its interconnects enables improved RLC extraction accuracy. As shown in Fig. 9, all of the wiring layers other than the topmost and bottom layers are shielded from the adjacent layers, and the upper and lower layers are of high density, so the number of types of pattern libraries necessary for extracting the capacitance of 2.5-D is greatly reduced. Furthermore, the uncertainty of the capacitance due to dummy metal is eliminated, and thus extraction accuracy is improved.

**Fig. 10. Regular DEPOGIT structure.**

Table III shows an example of a capacitance matrix that has the structure shown in Fig. 10. The value of \( C_{12} \) in Table III means the ratio of the coupling capacitance between the center wire 1 in Fig. 10 and adjacent wire 2 to the total coupling capacitance for wire 1 with the wire 2 to 8. It can be seen that in the intermediate layers the coupling capacitance between a certain wire of interest and non-adjacent wires is no more than 1%, and in the topmost layer this coupling capacitance is no more than 8%.

Thus, this density and uniformity make it possible to predict the coupling capacitance prior to detail wiring with much greater accuracy.

**Table III**

<table>
<thead>
<tr>
<th>Layer</th>
<th>( C_{12} )</th>
<th>( C_{13} )</th>
<th>( C_{14} )</th>
<th>( C_{15} )</th>
<th>( C_{16} )</th>
<th>( C_{17} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>M9</td>
<td>92.4</td>
<td>3.4</td>
<td>1.3</td>
<td>0.7</td>
<td>0.4</td>
<td>0.3</td>
</tr>
<tr>
<td>M7</td>
<td>99.0</td>
<td>0.9</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
</tbody>
</table>

**E. Evaluation of area penalty**

We evaluate a change made in the wiring area when the proposed architecture is used. The original total area \( A_{\text{org}} \) is

\[ A_{\text{org}} = A_{\text{chip}} \cdot N_{\text{org}}, \]

(1)
where $A_{chip}$ is the original chip area and $N_{org}$ is the original number of layers. The new total area $A_{new}$ due to our proposed architecture is roughly expressed by

$$A_{new} = A_{chip} \left\{ R_{org} \left( N_{org} - N_{app} \right) + R_{sig} \cdot N_{app} \cdot R_{sig} + N_{org} \cdot R_{fix} \right\}, \tag{2}$$

where $R_{wiring}$ is the ratio of the wiring area to chip area, $N_{org}$ is the original number of layers, $N_{app}$ is the number of layers in which the proposed method was applied, $R_{sig}$ is the ratio of signal line to total wiring area, and $R_{fix}$ is the ratio of the fixed area which is not available for wiring. The ratio of metal density to chip area is generally from 20% to 40% in each layer. The ratio of the area necessary for wiring becomes twice the metal density when spacing is assumed to be the same as the wiring width. To achieve uniformity, dummy metal is inserted in 10% to 30% of the total area.

Either the wiring area or the number of layers increases if a wiring pattern with a small signal line ratio is used. As an example of the area calculation, we assume that the proposed architecture whose pattern is PGSSSS on the average is applied to intermediate layers without both two bottom layers for the local power-ground lines and two top layers for the global power-ground lines, and that the free area of all the layers is used. Namely, $N_{org}$ is 9, $N_{app}$ is 5, and $R_{sig}$ is 2/3. We also assume that $R_{wiring}$ is 60% and $R_{fix}$ is 20%. As a result, from (1) the original total area $A_{org}$ is 9$A_{chip}$, and from (2) the total area $A_{new}$ to which the proposed architecture is applied is 8.7$A_{chip}$. Thus, in this example, the proposed method can be applied without any significant area penalty being incurred.

IV. Conclusion

We have proposed a new interconnect architecture for physical design integrity. The basic structure of this architecture consists of dense power-ground wire pairs. It provides the shielding effect and can also generate an explicit decoupling capacitance by means of PG pair wires. Also, this structure can guarantee high density and uniformity of wire, and eliminate the need for dummy metal. As a result, this architecture can simultaneously improve the signal integrity, power-ground integrity, design for manufacturability and accuracy of parasitic extraction, thus leading to robust design.

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