Abstract - As the operation frequency reaches gigahertz in deep-submicron designs, the effects of inductance on noise and delay can no longer be neglected. Some of the previous techniques such as net ordering, shield insertion, twisted-bundle layout structure, and interdigitated techniques are either inefficient or incur too much area penalty. In this paper, we present two techniques — ground-aware net routing and source pin positioning — that can reduce inductance effectively without incurring area penalty. In order to prove the effectiveness of our techniques, we use the famous 3D field-solver FastHenry [7] to extract inductances and verify our results. All simulation results show that our proposed techniques can significantly reduce inductances without incurring area penalty.

1 Introduction

As the process technology advances, inductance effects on on-chip interconnect structures have become increasingly significant [10]. This phenomenon is caused by the following factors: (1) because of the introduction of copper and wider upper-layer metal wires, the resistance of interconnect reduces, (2) the use of low-k dielectric decreases the capacitance effects, and (3) high clock frequency (short rise/fall time) decreases the impedance of wire capacitance which is $1/j\omega C$ ($\omega = 2\pi f$), and increases the impedance of wire inductance which is $j\omega L$. All of these make inductance effects more significant than before, especially on global interconnects such as clock wires and signal buses. Inductance effects will continue increasing as the process technology keeps shrinking.

On-chip inductance effects in high-performance circuit designs might impact interconnect in many ways. The performance of a circuit will be regarded due to the increase of wire delay [1][6]. The reduction of signal transition times together with inductive crosstalk can cause signal integrity related problems [4]. Signal overshoots and undershoots due to wire inductance may damage devices. Finally, inductance in power and ground grids can increase the noise in the supply and ground voltages when large currents flow. Therefore, inductance effects cannot be neglected in today’s high-performance circuit designs.

Most existing works focus on reducing coupling capacitance. There are still not many works on minimizing inductance effects. Massoud et al. proposed interdigitated techniques to reduce self-inductance [9]. He and Lepak [4] presented simultaneous shield insertion and net ordering to minimize capacitive and inductive coupling. He and Xu [5] found out that both self and mutual inductance can be reduced in stripline and micro-stripline structures. Zhong et al. developed the twisted-bundle layout structure for minimizing inductive coupling noise [12].

Although most of previous works can successfully reduce inductance effects, they might suffer from the same shortcoming – the more inductance effects they reduce the more area penalty they pay. Since the cost of a chip is quadratically proportional to the die area, those area overheads will limit the usage of those techniques. Others like net ordering are not effective enough since inductances are long-range effects [5]. In this paper, we suggest two routing techniques, ground-aware net routing and source pin positioning, that can successfully reduce on-chip interconnect inductance without incurring area penalty. In order to prove the effectiveness of our techniques, we use the famous 3D field-solver FastHenry [7] to extract inductances and verify our results. All simulation results show that our proposed techniques can significantly reduce mutual inductance without incurring area penalty.

The rest of this paper is organized as follows. Section 2 describes the coplanar interconnect structure and some basic electromagnetic concepts. Section 3 explains the ground-aware net routing technique and conducts some simulations to verify its efficiency. Section 4 describes the source pin positioning techniques and gives the simulation results to prove its efficiency. Finally, Section 5 concludes our work.

2 Preliminaries

According to Faraday’s law, the mutual inductance can be calculated by deriving the magnetic flux linking one loop related to per unit of current in the other loop [3] as shown in Equation (1):

$$L_{ij} = \frac{\Phi_j}{I_i} = \frac{1}{\mu_s} \int S \cdot \vec{B} \cdot d\vec{S},$$

where $\Phi_j$ is the magnetic flux in loop $j$ due to the current $I_i$ in loop $i$, $\vec{B}$ is the magnetic flux density arising from current $I_i$ in loop $i$, and $S$ represents the surface bounded by the loop $j$. $L_{ij}$ represents the self inductance of loop $i$, whereas $L_{ij}$ ($i \neq j$) represents the mutual inductance between loops $i$ and $j$.  

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From Faraday's law as shown in Equation (1), there are three possible methods to reduce the mutual inductance: (i) by creating a negative magnetic flux to cancel a positive one; (ii) by eliminating the loop area of the second loop (loop $j$); (iii) and by reducing the magnetic flux density. For example, the twisted-bundle layout structure uses method (i) to reduce the coupling inductance, shield insertion, stripline, and micro-stripline structure use the mixed methods of (ii) and (iii), and net ordering together with micro-stripline uses method (iii) to reduce the coupling inductance.

Figure 1 depicts the coplanar interconnect structure used throughout this paper. Here, $s$ stands for a signal wire while $P$ and $G$ stand for a power and a ground grids of identical width, $w_c$. Assume that all wires are of the same height $h$, the width and the length of each signal wire are $w_i$ and $l_i$, respectively, and the overlapping length of two signal wires is $l$. In this paper, we set the clock frequencies to 10 GHz in our simulations. And we assume that all signals use the nearest power/ground grids as their return paths [2]. Both power and ground grids are treated as ground grids in this paper. We use the famous 3D field-solver FastHenry [7] to extract inductances of interconnects.

3 Ground-Aware Net Routing Techniques

As shown in Figure 2 (a) and (b), if we want to route two signal nets $s_1$ and $s_2$ ($s_1$ is longer than $s_2$) in a coplanar structure, there are two possible routing topologies. For these two routing topologies, both of them have the same coupling capacitance because of the same overlapping length. By using Equation (2) of the AMAS (Analytical Model Approximation of Coupling Inductance) [11], $L_{ii}$ is proportional to $l$ when $w_i$, $w_g$, $d_i$, and $d_g$ is constant, and is given by

$$L_{ij} = \frac{l_0}{2\pi} \left( \ln \left( \frac{(0.5w_i + d_i + w_g)^{0.5}(d_g + d_i + 1.5w_i)}{(0.5w_i)^{0.5}(d_g + 0.5w_i)} \right) \right) + 1.$$  

Therefore, coupling inductance is also proportional to the overlapping length when wire lengths are longer than wire spaces ($l_i >> d_i$ and $l_i >> d_g$) as $w_i$, $w_g$, $d_i$, and $d_g$ remains the same [11]. Hence, both topologies also have the same coupling inductance.

However, the self inductance of $s_1$ ($L_{11}$) in Figure 2 (a) will be larger than that in Figure 2 (b). The reason is that the loop area of $s_1$ in Figure 2 (a) (gray region) is larger than that in Figure 2 (b). And the larger loop area implies the larger inductance. By using Equation (3) of the AMAS (Analytical Model Approximation of Self-inductance) [11], $L_{ii}$ is a function of $d_i$ when $r_i$ ($0.5w_i$), $r_g$ ($0.5w_i$), and $l_0$ is constant. So the self inductance $L_{11}$ can be reduced by decreasing $d_i$.

$$L_{ii} = \frac{l_0}{2\pi} \mu_0 \left[ 0.375 + \ln \left( \frac{(r_i + d_i)^{0.5}(r_g + d_i)}{r_i r_g} \right) \right].$$  

Therefore, we suggest routing the critical net (the longest net) as near the ground grid as possible to minimize inductance effects. This concept is also a utilization of the method (ii) discussed in the previous section.

Next we use FastHenry to extract the inductance in Figure 2 to verify our discussion. We set $h = 2\mu m$, $w_i = 1\mu m$, $d_i = 1\mu m$, $w_g = 2\mu m$, $d_g = 1 \text{ or } 5\mu m$, $d_g = 26\mu m$, and the wire lengths of $s_1$ and $s_2$ are 2000$\mu m$ and 500$\mu m$, respectively. The simulation results are shown in Table 1. From Table 1, we can observe that both $L_{11}$ and $L_{12}$ are improved by reducing the loop area of $s_1$, but the reduction of $L_{12}$ is marginal because the coupling inductance is also proportional to the overlapping length of wires when wire length is long enough as mentioned above. We should also note that $L_{22}$ increases as the loop area of $s_2$ increases, but $s_2$ here is not a critical net. Besides, the increment of $L_{22}$ is less than the decrement of $L_{11}$. Therefore, we can reduce inductance effects by using this technique.

<table>
<thead>
<tr>
<th>$d_g$ ($\mu m$)</th>
<th>$d_g=5\mu m$</th>
<th>$d_g=1\mu m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{11}$ ($10^{-11}$H)</td>
<td>$15.5033$</td>
<td>$14.1692$</td>
</tr>
<tr>
<td>$L_{12}$ ($10^{-11}$H)</td>
<td>$3.53447$</td>
<td>$3.8646$</td>
</tr>
<tr>
<td>$L_{22}$ ($10^{-11}$H)</td>
<td>$2.51043$</td>
<td>$2.51123$</td>
</tr>
<tr>
<td>Reduce</td>
<td>$8.61 %$</td>
<td>$9.34 %$</td>
</tr>
</tbody>
</table>

To show that the coupling capacitances between $s_1$ and $s_2$ in Figure (a) and (b) are about the same, we use another famous 3D field-solver FastCap [8] to extract the capacitances. The coupling capacitance $C_{12}$ is 1.745 fF in Figure (a) and 1.857 fF in Figure (b) for $d_g = 5\mu m$. Hence, the coupling capacitances remain about the same by using these two routing topologies as mentioned before.
In order to show that reducing the loop area (reducing \( d_{g1} \)) is more effective than just increasing the wire space (increasing \( d_s \)) in minimizing inductance effects, we conduct the following simulations. As shown in Figure 3, we decreased \( d_{g1} \) from 5\( \mu \)m to 1\( \mu \)m and increased \( d_s \) from 1\( \mu \)m to 5\( \mu \)m both with step 1\( \mu \)m while keeping all other parameters fixed, and plotted the curve of the self inductance \( L_{11} \). As shown in Figure 4, we also decreased \( d_{g1} \) and increased \( d_s \), and plotted the mutual inductance \( L_{12} \).

From Figure 3, we observe that \( L_{11} \) remains almost unchanged by increasing \( d_s \) but reduces rapidly by decreasing \( d_{g1} \). Since the loop area of \( L_{11} \) will remain constant no matter how \( d_s \) changes, \( L_{11} \) will remain the same as \( d_{g1} \) increases. (The small increase of \( L_{11} \) is due to the fact that a small fraction of signal current returns from the farther ground grid.) However, the loop area of \( L_{11} \) is significantly determined by \( d_{g1} \), so \( L_{11} \) decreases rapidly as \( d_{g1} \) decreases. Hence, if \( d_{g1} \) is zero, \( L_{11} \) is supposed to be zero, too.

In Figure 4, the mutual inductance \( L_{12} \) decreases linearly to the reduction of \( d_{g1} \) while it only decreases slightly with the increasing of \( d_s \). Since inductance effects are long-range effects, increasing wire space will gain only little improvement in minimizing the mutual inductance. Nevertheless, since the mutual inductance strongly depends on the loop area, reducing loop area (decreasing \( d_{g1} \)) is more effective for reducing the mutual inductance.

Therefore, in this section, we conclude that we should route the longest net (it is often a critical net) as close to the power/ground grids as possible to minimize inductance effects. As a side effect, this routing topology will also benefit from reducing coupling capacitance to the net.

## 4 Source Pin Positioning

Consider the coplanar structure as shown in Figure 5, signal wire \( s_1 \) has one source and one sink, and signal wire \( s_2 \) has one source and two sinks. A question arises: Does the position of the source pin of \( s_2 \) affect the value of the coupling inductance? The answer is affirmative, and it does have a great impact on coupling inductance. We conduct the following simulations to show how the position of the source affects the coupling inductance. We set \( h = 2 \mu \)m, \( w_s = 1 \mu \)m, \( d_i = 1 \mu \)m, \( w_g = 2 \mu \)m, \( d_{g1} = 5 \mu \)m, \( d_{g2} = 26 \mu \)m, and both the wire lengths of \( s_1 \) and \( s_2 \) are 2000\( \mu \)m. Then we change the position of the source of \( s_2 \) from the left end to the middle of the wire. We define that the left end of the signal wire \( s_1 \) is at position 0\( \mu \)m, so the middle of the wire is at position 1000\( \mu \)m.

The value of the coupling inductance \( L_{12} \) with respect to the position of the source is plotted in Figure 6, and the self inductance \( L_{22} \) with respect to the position of the source is plotted in Figure 7.

From Figure 6, we observe that as the position of the source approaches the middle of the wire, the coupling inductance decreases more rapidly. When the source is positioned at the middle of the wire, the coupling inductance is almost equal to zero. To explain this situation, we consider Figure 8 with an assumed current \( I \)
flowing from the source of $s_2$. Since the impedances of the left and the right wire segments are identical because of equal lengths, the currents flowing in the two parts are also equal ($0.5I$) but in opposite directions. Therefore, the magnetic fields caused by the currents in the left and the right wire segments are equal in magnitude, but in opposite directions.

According to Equation (1), the coupling inductance $L_{12}$ can be derived by calculating the magnetic flux in Loop 1 due to the current $I$ in Loop 2:

$$L_{12} = \frac{1}{I} \int_{S_{11}} \vec{B}_{12} \cdot d\vec{s}_1. \quad (4)$$

We divide the surface of Loop 1 into two equal parts $S_{11}$ and $S_{12}$ as shown in Figure 8. Then, we rewrite Equation (4) as

$$L_{12} = \frac{1}{I} \left( \int_{S_{11}} \vec{B}_{21} \cdot d\vec{s}_{11} + \int_{S_{12}} \vec{B}_{22} \cdot d\vec{s}_{12} \right), \quad (5)$$

where $\vec{B}_{21}$ and $\vec{B}_{22}$ are due to the currents in the left and the right wire segments, respectively. Therefore, the two integrations over $S_{11}$ and $S_{12}$ cancel each other:

$$\int_{S_{11}} \vec{B}_{21} \cdot d\vec{s}_{11} = -\int_{S_{12}} \vec{B}_{22} \cdot d\vec{s}_{12}. \quad (6)$$

Hence, the mutual inductance between signals $s_1$ and $s_2$ is zero:

$$L_{22} = \frac{1}{I} \left( \int_{S_{11}} \vec{B}_{21} \cdot d\vec{s}_{11} - \int_{S_{12}} \vec{B}_{22} \cdot d\vec{s}_{12} \right) = 0. \quad (7)$$

This concept is also a utilization of the method (i) discussed in Section 2.

From Figure 7, we observe that the self inductance $L_{22}$ is similar to the mutual inductance $L_{12}$ with respect to the position of source. The reason is also due to the cancellation of the equal-in-magnitude but opposite-in-direction magnetic fields. However, $L_{22}$ cannot be minimized to zero when the source of $s_2$ is in the middle of the wire. As pointed out in [11], the self inductance of a wire loop contains two parts — the internal and the external self inductance which are inside and outside the conductor, respectively. The external self inductance can be reduced to zero by simply re-deriving the equations from Equation (4) to (7). However, the internal self inductance will not change whatever the source position changes. Therefore, the reduction of the self inductance $L_{22}$ will saturate to the value of the internal inductance of $L_{22}$ when moving the source position closer to the middle of the wire.

To show the effectiveness of positioning the source in reducing inductance effects, we conducted simulations in the stripline structure as shown in Figure 9. We set $h = 2\mu\text{m}$, $w_s = 1\mu\text{m}$, $d_s = 1\mu\text{m}$, $w_g = 2\mu\text{m}$, $D_1 = 1.4\mu\text{m}$, $D_2 = 4.8\mu\text{m}$. Both the wire lengths of $s_1$ and $s_2$ are set to $2000\mu\text{m}$. Then we changed the position of the source of $s_2$ from the left end to the middle of the wire. The value of the self inductance $L_{22}$ with respect to the position of source is plotted in Figure 10, and the coupling inductance $L_{12}$ with respect to the position of source is plotted in Figure 11.

From Figures 10 and 11, we can conclude that the reductions of inductance effects are also very significant in the stripline structure when the source of $s_2$ is positioned at the middle of the wire.
Therefore, we conclude that when routing wires with multiple sinks, we shall place the source of the net (especially for a longer wire) as near the middle of the wire as possible to minimize inductance effects. Besides, this routing topology can also be applied to the stripline and the micro-stripline structure to minimize inductance effects.

5 Conclusion

In this paper, we have presented two techniques — ground-aware net routing and source pin positioning — that can reduce inductance effectively without incurring area penalty. To show the effectiveness of our techniques, we applied the famous 3D field-solver FastHenry [7] to extract inductances and verify our results. All simulation results have shown that our proposed techniques can significantly reduce inductance effects without incurring area penalty.

Our future work lies in developing an algorithm combining these techniques to minimize inductance effects in the coplanar interconnect structure.

6 Reference