An implementation of memory-based on-chip analogue test signal generation

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Abstract – This paper presents a memory-based on-chip analogue test signal generation approach that is suitable for the test of an Analogue and Mixed-Signal (AMS) core. This core contains programmable electronic interfaces for acoustic and ultrasound transducers. The test signals that must be generated on-chip have only low or moderate frequencies (10 Hz-10 MHz). The test circuitry designed in a 0.18 mm CMOS technology includes a programmable shift-register, a clock divider, and a programmable switched-capacitor filter bank. By controlling the shift-register length and the sampling frequency, the paper shows that high quality single tone signals can be generated on chip in the band of interest.

I. INTRODUCTION

Low-cost testing of Analogue and Mixed-Signal (AMS) cores requires avoiding the use of expensive AMS testers. Testing AMS cores using a digital tester can be achieved by generating on-chip, from digital seeds, the analogue test signals for the core cells and by producing output digital signatures from the cells response.

In this paper, we will focus on the on-chip analogue test signal generation. In our study, we are limited to the on-chip generation of test signals at low and moderate frequencies (10 Hz - 10 MHz) since the AMS core corresponds to a programmable electronic interface for acoustic and ultrasound sensors. Note that testing audio circuits for deep sub-micron technologies is expected to be a major challenge when they are combined with large numbers of noisy digital circuits [1].

We have focused our attention towards a memory-based approach for the generation of single tone analogue signals by low pass filtering a periodic bit stream generated with a shift-register. By controlling the shift-register length and clock frequency, we show that high quality signals can be generated on-chip in the band of interest, while keeping simple the realisation of the on-chip filter.

The paper is organized as follows. We will first review previous works in the field of on-chip analogue signal generation before detailing the actual architecture of the on-chip test generation strategy. The strategy is next evaluated by simulation and a CAD tool useful for defining the digital test patterns required is illustrated. The implementation of the circuitry in a 0.18 µm CMOS technology, including the digital part and the analogue filtering will be presented next. Finally, we will conclude with a summary of our current and future work.

II. PREVIOUS WORK

The on-chip generation of analogue test signals by low-pass filtering a periodically reproduced bit-stream previously encoded via sigma-delta modulation has been proposed in [2]. This technique is especially suitable for the generation of single and multi tone test signals, producing high quality signals that are not susceptible to filter shape. The technique has also been shown for the generation of arbitrary band-limited pulses.

Other researchers have applied this technique to the generation of ramp signals for the static test of Analogue-to-Digital Converters (ADCs) [3]. However, it is difficult to obtain a high resolution ramp with this technique. Low-pass filtering a bit stream encoding the ramp for removing quantisation noise always introduces distortion in the peaks and valleys of the up/down ramp [4].

Several authors have proposed the use of pseudo-random test signals generated by means of Linear FeedBack Shift-Registers (LFSRs) [5]. This technique radically simplifies the task of test signal generation. However it requires considerable memory and Digital-Signal Processing (DSP) on-chip to analyze the output response of linear circuits.

In this paper, we will show a realization of the technique proposed in [2] that uses a small amount of memory for generating high quality tones. This is obtained by controlling the shift-register length and the sampling frequency. The advantage of the technique is that only short digital test patterns need to be scanned into the chip for generating test signals for the cells of a mixed-signal core working at low and moderate frequencies

As shown in Figure 1, to generate an analogue signal, a bit-stream is first loaded into a shift-register during phase T1. The loaded bit-stream is then periodically reproduced during phase T2 at the output of the shift-register, by connecting the

output of the register to its input. The actual bit-stream (a test pattern or seed for the shift-register) must be previously obtained by simulation by means of a ΣΔ modulator that encodes the desired analogue test signal (in this example, a single tone signal with frequency *f* sampled at frequency f_s). The bit-stream at the output of the shift-register clocked at frequency f_s is filtered on-chip to recover the actual encoded analogue signal (in this figure a low-pass filter with a cut-off frequency of $fc=f$). The actual filter must be of one order higher than the modulator used to code the signal, so that the slope of the rising quantisation noise does not match the falling attenuation of the filter. Much of the quantisation noise is centred on $f_s/2$ and the filter must be able to strongly attenuate high frequency noise, with a linear behaviour such that it does not modulate the noise back to the frequency band of interest [6].

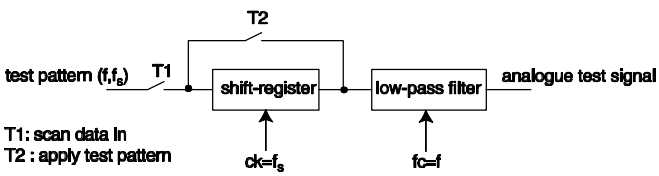


Fig. 1. Principle of Operation.

It is well known that by repeating a sample set, the actual signal will contain a limited number of coherent frequencies [7] given by:

$$f = \frac{M}{N} f_s \qquad M = 0,1,2,3,....,\frac{N}{2} \qquad [1]$$

where N is the number of samples (bits in the shift-register). The frequency resolution is then set by f_s/N.

In our work, we can well exploit this approach since high frequency clock signals will be available from the overall chip, providing the basis for high oversampling ratios with respect to the analogue acoustic and ultrasound signals processed by the core cells under test. We will show how by controlling on-chip the shift-register length (*N*) and the sampling frequency we can generate single tone test signals with a quality high enough for the core cells.

III. Architecture for Signal Generation

The architecture for signal generation is shown in Figure 2. In this circuit, the sampling frequency that clocks the shift-register is controlled by simple division of the chip clock (we assume on-chip a 1 GHz clock signal, without any loss of generality). The shift-register length is controlled by programming a length between a minimum of 100 bits and a maximum of 200. The filter block connected at the output of the shift-register is also programmable (both order and cut-off frequency) and allows recovering the analogue signal encoded in the bit-stream.

A test vector for on-chip generation of an analogue signal is 256 bits long, as shown in Figure 3. The test vector includes the seed to be loaded in the shift-register and the programming of the clock division factor, seed (shift-register) length, filtering control and other control signals required to drive the analogue test signal generated to the actual module under test.

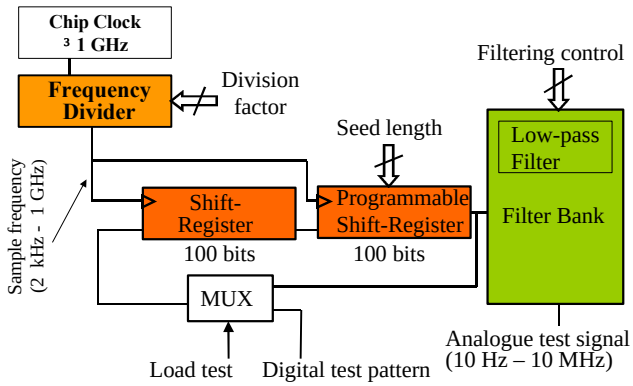


Fig. 2. Architecture for on-chip analogue test signal generation.

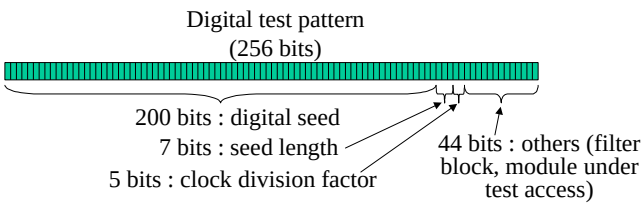


Fig. 3. Structure of the test patterns used for on-chip analogue test signal generation.

The advantage obtained by being able to control both the shift-register length and the sampling frequency can be well understood by looking at Table 1.

TABLE I
Fundamental frequencies obtained by controlling the shift-register length and the sampling frequency.

Programmable shift-register length between 100 and 200 bits

DIV	FS	N				
		100	101	.....	199	200
1	1,00E+09	1,00E+07	9,90E+06		5,03E+06	5,00E+06
2	5,00E+08	5,00E+06	4,95E+06		2,51E+06	2,50E+06
4	2,50E+08	2,50E+06	2,48E+06		1,26E+06	1,25E+06
8	1,25E+08	1,25E+06	1,24E+06		6,28E+05	6,25E+05
16	6,25E+07	6,25E+05	6,19E+05		3,14E+05	3,13E+05
32	3,13E+07	3,13E+05	3,09E+05		1,57E+05	1,56E+05
64	1,56E+07	1,56E+05	1,55E+05		7,85E+04	7,81E+04
128	7,81E+06	7,81E+04	7,74E+04		3,93E+04	3,91E+04
256	3,91E+06	3,91E+04	3,87E+04		1,96E+04	1,95E+04
512	1,95E+06	1,95E+04	1,93E+04		9,81E+03	9,77E+03
1024	9,77E+05	9,77E+03	9,67E+03		4,91E+03	4,88E+03
2048	4,88E+05	4,88E+03	4,83E+03		2,45E+03	2,44E+03
4096	2,44E+05	2,44E+03	2,42E+03		1,23E+03	1,22E+03
8192	1,22E+05	1,22E+03	1,21E+03		6,13E+02	6,10E+02
16384	6,10E+04	6,10E+02	6,04E+02		3,07E+02	3,05E+02
32768	3,05E+04	3,05E+02	3,02E+02		1,53E+02	1,53E+02
65536	1,53E+04	1,53E+02	1,51E+02		7,67E+01	7,63E+01
131072	7,63E+03	7,63E+01	7,55E+01		3,83E+01	3,81E+01
262144	3,81E+03	3,81E+01	3,78E+01		1,92E+01	1,91E+01
524288	1,91E+03	1,91E+01	1,89E+01		9,58E+00	9,54E+00

20 possible sampling frequencies

2000 possible fundamental frequencies F (M=1) in the range 10 Hz – 10 MHz

As a function of the sampling frequency and the shift-register length, we can obtain a principal coherent frequency (*M=1* in Equation [1]) in the band 10Hz- 10MHz with a frequency resolution better than 0.5 %. Choosing

N=100 corresponds to an Over Sampling Ratio (OSR) of 50 while *N=200* corresponds to an OSR of 100. Using the principal frequency for coding the signal has the advantage that the actual analogue signal can be recovered from the bit-stream by simple low-pass filtering for a single tone signal.

IV. Evaluation of the Approach

We have studied by simulation the quality of the analogue signals that can be generated on-chip in terms of the Spurious Free Dynamic Range (SFDR) and the Total Harmonic Distortion (THD) obtained as a function of the OSR. The results are shown in Figure 4

We notice first that each row in Table I must give the same results in terms of SFDR and THD as a function of the signal frequency. For example, to generate a signal at 10 MHz, we will use a division factor of 1 (giving a sampling frequency of 1 GHz) with a shift-register length of 100 bits. This corresponds to an OSR of 100. The results in terms of SFDR and THD for this signal are the same as those obtained for the generation of a signal at 5 MHz, using a division factor of 2 and a sampling frequency of 0.5 GHz that corresponds also to an OSR of 100. Thus the curves of SFDR and THD as a function of OSR are representative of the overall table.

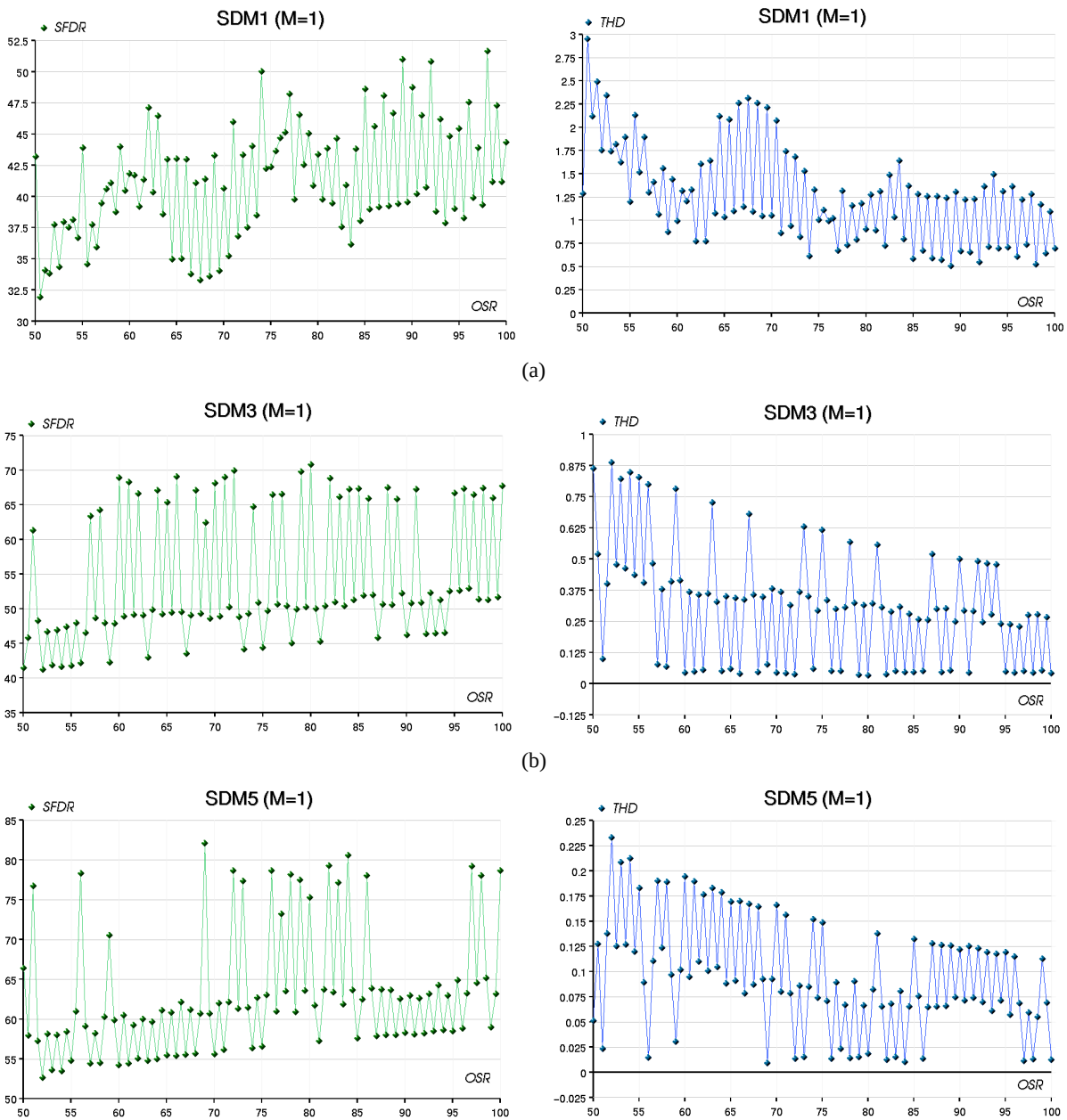


Fig. 4. SFDR and THD as a function of OSR for single tone signals generated using non-optimized bit-streams. The bit-streams are produced with a ΣΔ modulator of increasing order : 1,3 and 5, respectively, from (a) to (c).

In the results of Figure 4, each point is obtained as follows. For each value of OSR, the corresponding number of bits (*N=100* for *OSR=50*, *N=200* for *OSR=100*) are read from the modulator output after ten periods of the input analogue signal, so that the modulator output can be considered stable. These bits are then fed to a shift-register of length *N*, with the output connected to the input, and clocked at the sampling frequency. The output of the shift-register is fed to a low-pass filter with a cut-off frequency set to the frequency of the input analogue test signal, the filter being one order higher than the modulator.

The results of Figure 4 show that both the SFDR and the THD tend to increase with the value of OSR and with the order of the modulator (and corresponding low-pass filter). We notice however a difference between the case in which the shift-register length N or the OSR (OSR=N/2) is even or odd. In the case of N even, the results are sometimes good and sometimes bad, showing a need for optimizing the bit stream. On the other hand, when N is odd, the results are always bad. Thus in Figure 4(c), for example, for the modulator of 5^{th} order and for the SFDR plot, we observe a top line that corresponds to N even and good results. The bottom line corresponds to N even and bad results. Finally, The intermediate line corresponds to N odd and always bad results.

V. A CAD TOOL FOR SEED GENERATION

A CAD tool helps us in automatically generating the test vector that must be loaded to generate on-chip an analogue test signal. As shown in the graphical interface of Figure 5, the tool takes as input a description of the wanted analogue signal and produces as output the digital seed (in hexadecimal code) that must be loaded in the test circuitry, optimizing the shift-register length and sampling frequency that allow obtaining a high quality analogue signal. The tool is fully integrated in the CADENCE environment and the calculation process inherent to the tool operation is transparent to the user. In fact, there is no simulation taking place, since all calculations are directly performed through functions existing in the environment, either programmed using the Skill language or obtained via built-in functions (such as those required for DFT calculations). Thus, each point in the graphs of Figure 4 is obtained in about 1 second, without optimization (very similar results were obtained using circuit simulation). Currently, this tool works for the generation of single tone signals and is being extended for multi-tone and more general band-limited signals, considering bit-stream optimization as discussed next.

VI. OPTIMIZATION OF SEEDS

As shown by [2], the quality of the signals generated can change significantly with very small deviations of the parameters of the analogue test signal to be coded (such as the phase or the amplitude). For example, Figure 6 shows the change of SFDR as a function of the phase of the input analogue signal. The phase has been changed between 70° and 110° with steps of 0.1°. It can be seen that the THD of the bit-stream obtained is either good (around 0.125%) or bad (around 1.125%) with a very important difference between both cases. This is the same type of behaviour that we observe in the results of Figure 4, when N is even, where the results are sometimes good and sometimes bad.

Optimizing the bit-stream requires then choosing the phase that gives the highest SFDR. The general approach to do this is to choose randomly several phases and calculate the SFDR. It is experimentally seen that after a few iterations, the result obtained is practically optimal (this is obvious given that the results tend to be either good or bad, as suggested by Figure 6).

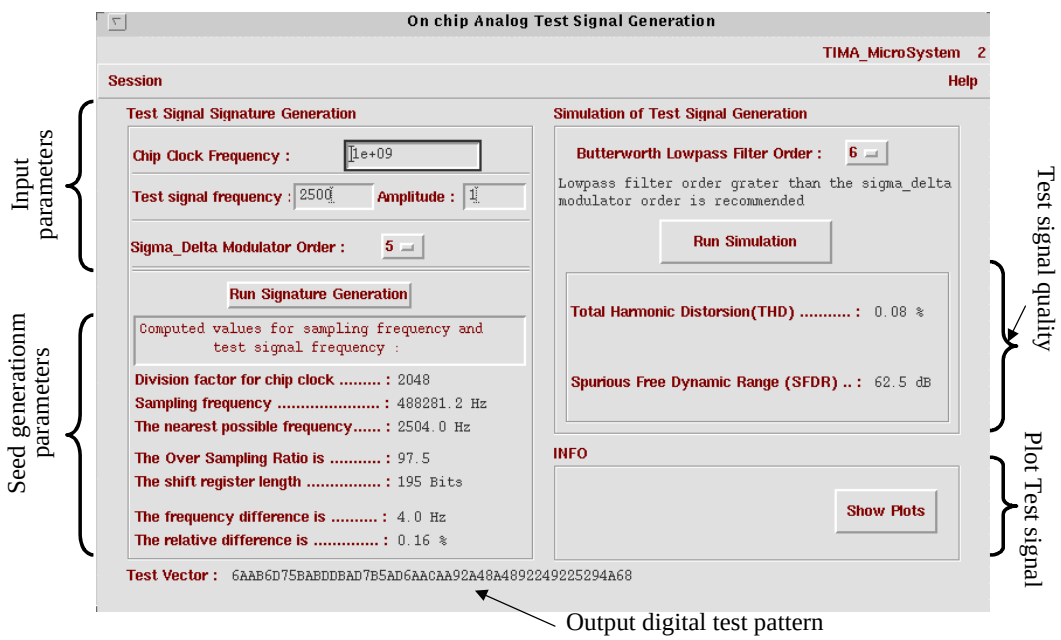


Fig. 5. Seed generation tool graphical interface.

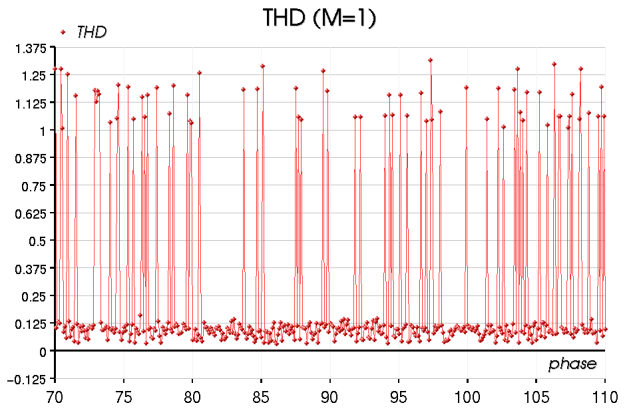


Fig. 6. THD of an on-chip generated signal as a function of the phase of the analogue signal fed to the ΣΔ modulator.

Such a procedure has been implemented in the CAD tool. The tool also has the possibility of optimizing multiple parameters at the same time, such as SFDR, THD and the amplitude of the coded signal.

Figures 7(a) and 7(b) shows the results obtained after optimizing the bit-streams for the case of modulators of first and second orders. In the first case, 25 iterations were used and in the second case 40 iterations. These results can be compared with Figure 4. It also appears more clearly that the signal quality tends to increase with the OSR.

The most significant point is that only the results obtained with an even number of shift-register bits get optimized, showing always good results that are systematically much higher than those obtained with an odd number of bits and that increase with the oversampling ratio. In conclusion, the shift register length has to be limited to an even length. Despite this, we can still show a frequency resolution better than 1 % for the signals that must be generated in the frequency band of interest

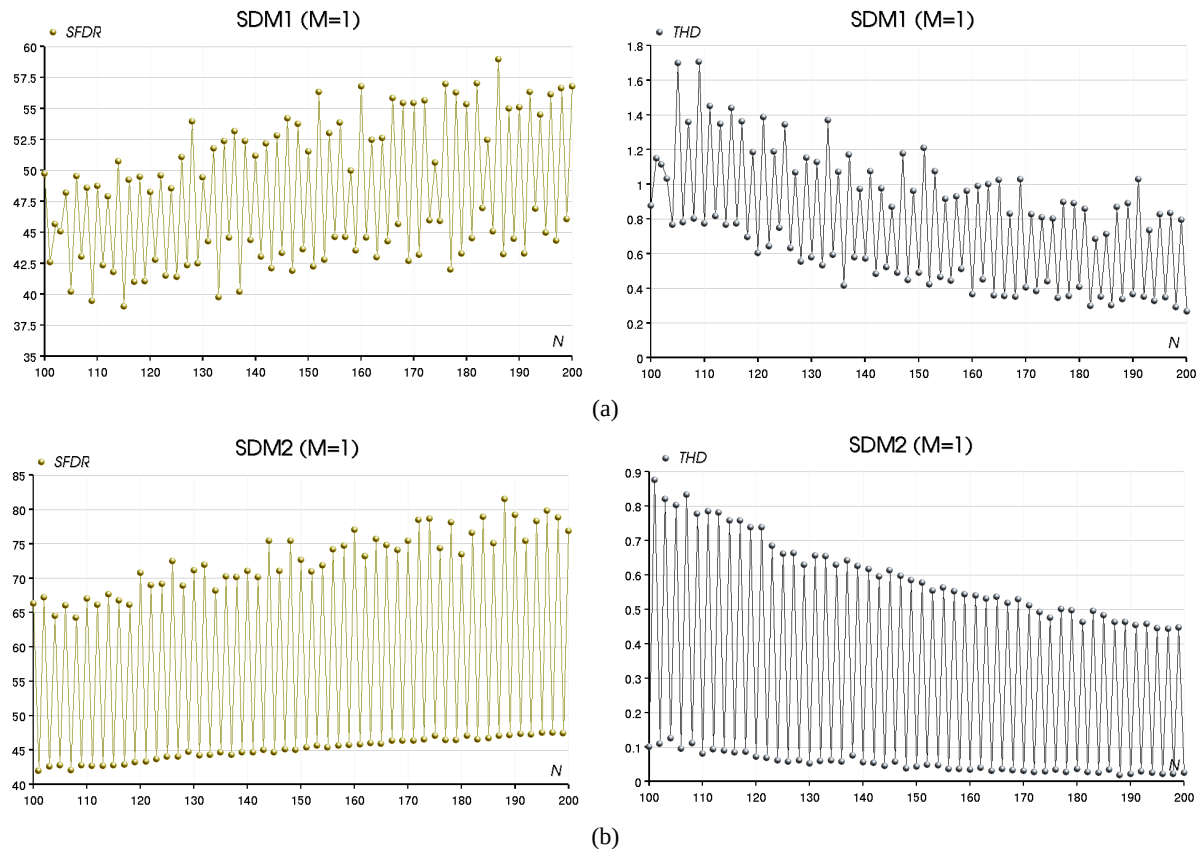
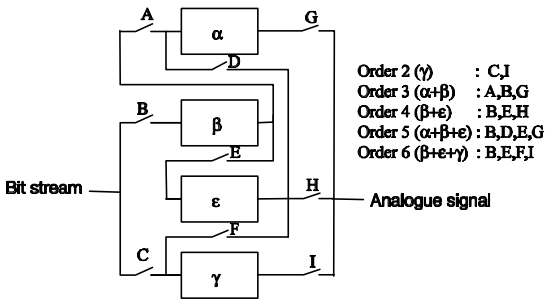


Fig. 7. SFDR and THD for the case of optimized bit-streams coded with ΣΔ modulators of first (a) and second order (b), as a function of the OSR.

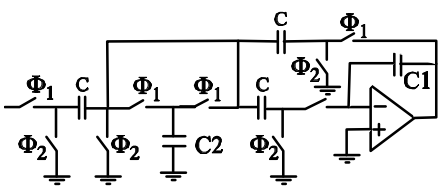
VII. CMOS IMPLEMENTATION

The test circuitry of Figure 2 is implemented in a 0.18 µm CMOS technology, considering a chip clock frequency at 1 GHz. The structure of the programmable filter bank is shown in Figure 8(a). It is composed of four programmable switched-capacitor blocks of first and second order that can be combined to realise low-pass Butterworth filters of

second to sixth order. Block α corresponds to an integrator and blocks β, γ, and ε correspond to a second order Rauch filter shown in Figure 8(b). The switched-capacitor resistors (C=0.5 pF) are designed such that the -3 dB frequency is 100 times smaller than the sampling frequency.

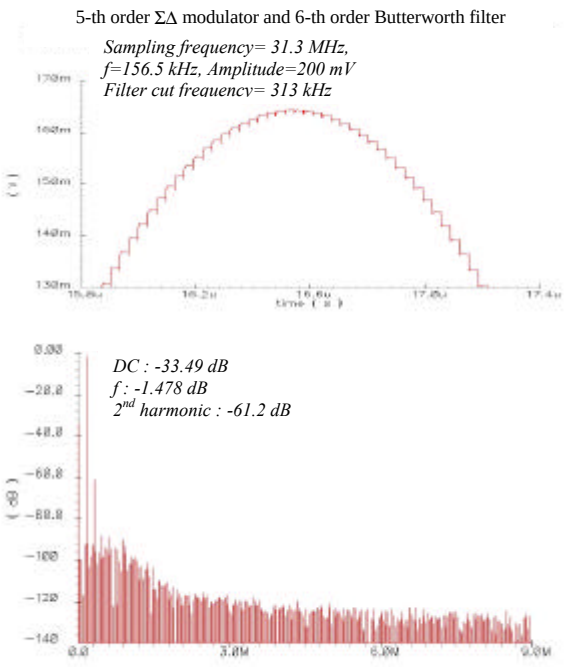


(a)



	α	β		ε		γ	
	Cint	C1	C2	C1	C2	C1	C2
Order 2	-	-	-	-	-	3.75	16,88
Order 3	7.95	2.65	23.87	-	-	-	-
Order 4	-	2.03	31.19	4.9	12.92	-	-
Order 5	7.95	1.64	38.63	4.29	14.75	-	-
Order 6	-	1.37	46.12	5.12	12.36	3.75	16.88

(b)



(c)

Fig. 8. Implementation of the filter bank : (a) architecture of the bank, (b) structure of a filter block and values for the programmable capacitors, and (c) simulation results for a 6-th order filter.

The blocks β and ε have programmable capacitors, according to the order of the filter designed, as given in Figure 8(b) (all capacitor values are in pF) and include a wide-band low-gain CMOS amplifier.

The transistor-level filter bank has been simulated using Spectre RF and works correctly, for the largest filter order, with sampling frequencies from 31.3 MHz down to 1.91 kHz, thus allowing the generation of single tones between 313 kHz and 9,5 Hz (see Table I). Similar results are obtained for high and low sampling rates. Higher sampling rates will require the design of a higher speed large band CMOS amplifier. Figure 8(c) shows the simulation results for the generation of a 200 mV signal at 156.5 kHz with a sampling frequency of 31.3 MHz. A bit-stream at this frequency is generated with a fifth order ΣΔ modulator and fed to the sixth order filter. The -3dB frequency of the filter is 313 kHz. The spectrum of the signal at the filter output gives about 60 dB of SFDR. It must be noted that very similar results are obtained with a second order ΣΔ modulator and a third order filter, simplifying the test circuitry required on-chip

VIII. FUTURE WORK AND ACKNOWLEDGEMENTS

Future work is required to demonstrate the usefulness of the technique in order to test a programmable analogue and mixed-signal core especially suitable for voice and ultrasound sensor applications. Pre-defined analogue test signals for the core cells must be obtained via fault simulation and test generation.

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