VeriCDF: A New Verification Methodology for Charged Device Failures

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ABSTRACT

A novel tool for full-chip verification is reported for CDM-ESD protection. Until recently, ESD protection has been simulated in device level, leading to the well known limitations on capturing global features such as the power protection circuits and package parasitics. In practice, fatal failures occur due to unexpected discharged paths in multi-power supply chips, which can only be verified by chip-level simulation. Associated with the new concept of macromodelling, hierarchical approach provides effective analysis methodology for mixed-signal chips. The hierarchical approach provides the analysis of chip-level discharging paths and reliability of gate oxide. Simulation results on a CMOS ASIC chip processed in a 0.25-μm technology are in accordance with the measurement data. Scanning electron microscope locates a gate oxide fault as our analysis predicted.

Categories and Subject Descriptors

B.8 [**Hardware**]: Performance and Reliability; C.4 [**Computer Systems Organization**]: Performance of Systems

General Terms

Verification

Keywords

Reliability, Modeling, Simulation

1. INTRODUCTION

An electrical surge of voltage or current that exceeds a device's rating can trigger either a catastrophic or parametric device failure. Such a sudden transfer of a voltage or current via inductance or direct contact is called *electrostatic discharge (ESD)*. ESD is a direct cause of electronic device failure when static charge or discharge attacks sensitive devices during manufacturing processes. The common failure modes caused by ESD are metalization meltdown, thermal secondary breakdown and dielectric breakdown.

As technology scaling continues, supply voltages are lowered, which substantially diminishes the tolerance of deep submicron devices. Thus, the risk of malfunctioning caused by ESD increases as the trends in silicon electronics miniaturization proceed. Estimated average product losses due to ESD damage range from 8% to 33% [1]. If such an ESD failure is investigated and controlled during design stage earlier than manufacturing, then valuable resources and cost can be saved and the chip reliability can be improved proportionally. This is the motivation of ESD failure modeling and simulation.

1.1 Issues on Electrostatic Discharge Models

Three primary models of ESD events have been developed: human body model (HBM), machine model (MM), and charged-device model (CDM). The direct transfer of electrostatic charge from the human body as a charge-storage capacitance can possibly cause device damage. The HBM is characterized by a relatively slow stimulus, and often energy-destructive failure occurs as a result. The CDM is intended to simulate charging and discharging events that occur in production equipment and processes. A chip can be charged from sliding down the feeder in an automated assembler, and then a rapid discharge can occur when it makes contact with low-impedance metal plate [2]. Most distinguishable feature of the CDM is the rapid flow of high current through the device that leads to dielectric destruction. As the dielectric failure mode has gained importance with scaled semiconductor devices and increased automated manufacturing lines, the importance of HBM and MM decreases and the CDM accounts for the majority of ESD failure during chip manufacturing. In this work, we focus on the CDM and its failure mechanism.

Previous works on CDM modeling and simulation have concentrated on the compact modeling of MOS transistor as an ESD protection device and have contributed to the analysis of MOS transistor behavior under CDM ESD stress [3, 4, 5]. These modeling and simulation techniques are limited to small ESD protection circuits because of the complexity of the extracted models. However, the overall CDM performance of a chip depends not only on the robustness of an ESD protection circuit, but also on global components such as the power protection network, inductance and resistance of power lines, and parasitic in the package. Moreover, in multiple power supply ICs, unexpected discharge paths can cause many failures that cannot be identified in the analysis of local ESD protection circuits. Therefore, CDM performance needs to be evaluated at the chip level, and large-scale CDM simulation should be used to predict CDM behavior in a chip with reliable accuracy.

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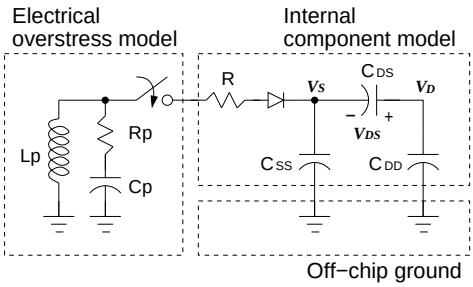

Figure 1: An equivalent circuit model of charged-device ESD event.

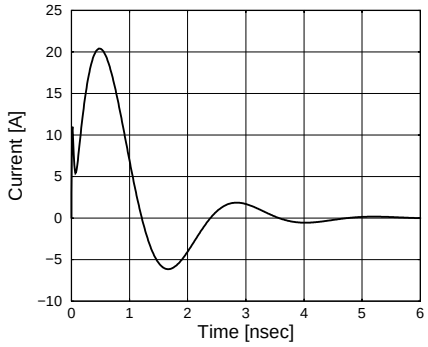

Figure 2: High current transient waveform for 1000 V CDM pulse.

1.2 Proposed Chip-Level CDM Model

In this work, *full-chip* modeling of charged-device failure (CDF) is proposed to overcome the limitations of localized approaches. Chip-level CDF modeling captures the impact of package capacitance and the distribution of power protection circuits on overall CDM performance. Chip-level modeling is accomplished by the divide-and-conquer strategy. For efficient modeling and simulation, the full-chip structure is partitioned into a set of subsystems based on the chip floorplan, the subsystem functionality, and the power bus architecture. A novel *CDM macromodel* is proposed to characterize each subsystem in terms of failure behavior for a given electrostatic overstress. The CDM macromodel incorporates lumped CDM capacitors, and internal resistors and capacitors that can be derived from power-ground network by using a layout extractor and analyzer such as iLEX [6]. Meanwhile, the accuracy of modeling is maintained by considering communication between groups of subsystems. For instance, the gate-oxide reliability of interface buffers used to span different power supply boundaries accounts for interactions between components. Chip-level CDF analysis is performed with a full set of macromodels and the ESD simulator, iETSIM [4].

In order to verify our CDM macromodel and chip-level failure modeling, the CDM tests are carried out for a mixed-signal CMOS ASIC chip processed in 0.25-μm technology. Simulated waveform based on our model is in accordance with the actual measurement data in terms of rise time and peak discharge voltage that determine the CDF. Furthermore, emission microscopy was used to inspect the static *Idd* failure location. As our chip-level simulations predict, a scanning electron microscope (SEM) photograph asserts oxide destructions in the power domain on a high-speed network interface subsystem.

This paper is organized as follows. Section 2 provides necessary details to understand the charging/discharging mechanism of CDM event and corresponding circuit-level CDF model. Section 3 presents the proposed circuit-level CDM macromodel. The hierarchical approach for modeling a chip is also described in this section. Section 4 presents CDM simulation and experimental results. Stress discharging paths are thoroughly investigated in a multi-power IC and the vulnerable devices to CDM stress are presented. Finally, conclusions are drawn in Section 5.

2. CHARGED-DEVICE MODEL (CDM)

The CDM assumes that the charge residing on lead frames and metal parts of a chip are quickly discharged through one pin to off-chip ground and causes failures in junctions, dielectrics, and components that are part of the discharge paths.

The CDM equivalent circuit we propose is illustrated in Fig. 1. The electrostatic charge on the package during the charging event can be modeled by the package capacitances C_{DD} and C_{SS}. C_{DD} (C_{SS}) is a capacitance between on-chip power (ground) metal planes and off-chip ground. We assume that the charge stored on package lead frames are equally distributed to C_{DD} and C_{SS}, and the capacitance between signal lines and off-chip ground is ignored due to little capacitance values. Internal capacitance C_{DS} represents all the lumped capacitance formed between internal power and ground planes.

Chip and tester inductance L_p from 1 to 50-nH as well as the device resistance R of 50 to 300-Ω have significant roles in the CDF. The parameters in the CDM equivalent circuit are largely dependent on the type of package and internal metal configuration. The current waveform of the CDM equivalent circuit after application of 1000 V positive CDM stress is shown in the Fig. 2. The damped oscillation occurs because of an *L-R-C* transition characteristic due to inductance and resistance of the discharging line and the capacitance of the device. The discharging current flowing as the switch turns on is expressed by [7]

$$I_{CDM}(t) = \frac{V_{CDM}}{\sqrt{\frac{L_P}{C_{eq}}}} \exp\left(\frac{-Rt}{2L_P}\right) \sin(\omega_S t) \tag{1}$$

where V_{CDM} is the charging voltage and $C_{eq} = C_P + C_{SS} + \frac{C_{DD} \cdot C_{DS}}{C_{DD}+C_{DS}}$. The series resonant frequency is given by $\omega_S = \frac{1}{\sqrt{L_P C_{eq}}}$. Thus, the peak CDM current is approximately:

$$I_{peak} = \frac{V_{CDM}}{\sqrt{\frac{L_P}{C_{eq}}}} \tag{2}$$

Note that the peak current is a strong function of V_{CDM}, C_{eq}, and L_P, and the damping factor is determined by the values of L_P and R.

2.1 CDM Discharging Mechanism

A CDM behavioral tree as shown in Fig. 3 illustrates a current flow from a package capacitance C_{DV} (representing either C_{DD} or C_{SS}) to off-chip ground. The charge stored in the package capacitance can be discharged through three paths. At the beginning, the charge current flows from a package capacitance C_{DV} into the internal capacitance C_{DS}. After charge is shared by C_{DV} and C_{DS}, if a node voltage V_{ref} is higher than the trigger voltages of internal devices, either internal devices or ESD protection circuits will be activated and discharge the charge to ground. Associated current flows are represented by I_{PC} and I_{Dev}, respectively.

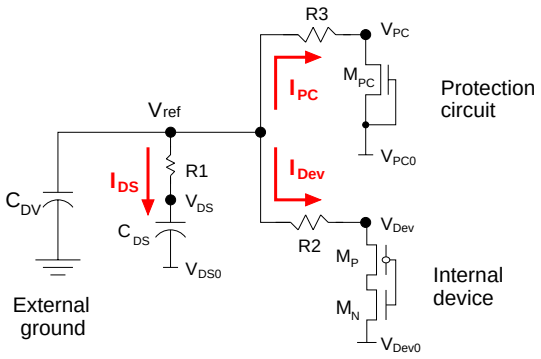

Figure 3: A basic CDM behavioral tree.

To protect internal devices against CDM-ESD stress, protection device M_{PC} should satisfy the following conditions:

$$\tau_{f,pc} < \tau_{f,int} \quad (3)$$

$$R_3 < R_2 \quad (4)$$

where τ_f represents the base transit time of an MOS device. Consequently, the optimization of the protection network which involves the design of protection circuit and the distribution of protection network is essential for robust CDM performance.

3. CHIP-LEVEL CDM MODELING

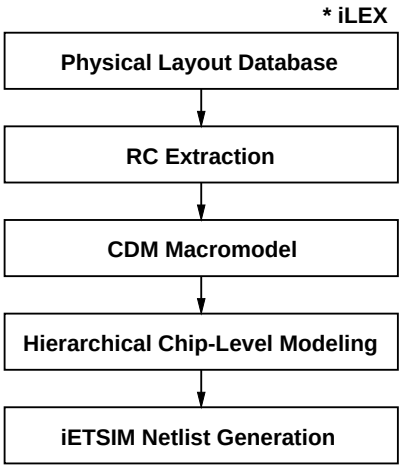

Figure 4: Chip-level CDF model extraction and simulation.

The basic concept of CDM behavior is represented by a CDM tree in a circuit level. It is feasible to apply the CDM behavioral tree for small I/O circuits, but impractical for full-chip simulation with this model. To overcome this inefficiency while maintaining accuracy, we propose a hierarchical method to encompass a full chip. The procedure for hierarchical modeling is outlined in Fig. 4. This procedure involves three major steps in translating a mixed-signal design into a netlist for circuit-level CDF simulation: (1) partitioning a chip into subsystems modeled by a circuit-level CDM macromodel, (2) extracting physical layout parameters for each macromodel, and then (3) simulating full-chip CDM behavior with combined macromodels.

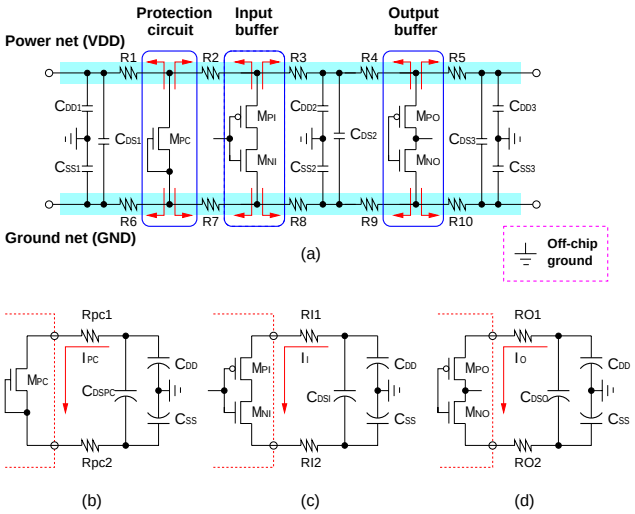

Figure 5: (a) A macromodel for each subsystem in a chip, and equivalent circuits driven by (b) protection circuits, (c) input buffer, and (d) output buffer.

3.1 Hierarchical CDM Modeling

The CDM tree can be built for each internal circuit node, and then CDM behavior is analyzed by using circuit simulator such as HSPICE. However, computational inefficiency of CDM tree-based method prohibits from full-chip simulation to appraise the overall effects of the package capacitance on the CDM performance.

In order to enhance efficiency, we exploit a hierarchical approach to full-chip CDF modeling and simulation. The first step of the simulation process is to partition the full-chip structure into smaller subsystems. Partitioning into subsystems serves two purposes. First, it simplifies the parasitic circuit, namely, the simulation variables within a subsystem. A partition treats each subsystem as a single CDM source and several discharging paths, and the variables are extracted as lumped elements. Second, the flow of CDM charge shifting among subsystems with different power domains can be accurately modeled because partitioning is carried out on the distinct power boundaries.

Partitioning is performed based on the chip floorplan, functions of each circuit block, and power bus architecture. Since the CDM is a charge driven phenomenon and the stress current is discharged through the least-impedance paths along the power-ground networks, major discharge paths such as ESD power protection circuits and I/O buffers in subsystems should be included. In a multi-functioned system, remote blocks on the chip floorplan can contribute to the CDM failures each other and hence should be modeled separately. While each power supply creates a subsystem, a big subsystem can be divided into several different subsystems to simplify the modeling. As a result, hierarchical modeling is carried out based on the following strategies:

- only one subsystem is defined in a specific power domain;
- heterogeneous functional blocks such as analog, RF, digital, and memory should be assigned as different subsystems;
- a block with the same function but remote chip placement can be mapped into different subsystems.

The next section describes the second step of the simulation process, namely the generation and characterization of the CDM macromodel.

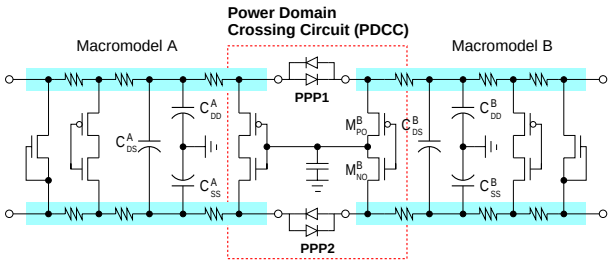

Figure 6: Two macromodels connected with power-to-power protection (PPP) circuits.

3.2 CDM Macromodel for Subsystem

The CDM macromodel captures the behavior of a subsystem with electrical overstress. The CDM macromodel is motivated by an important observation of CDF. The CDM-ESD test involves an ESD waveform of rapid change and high current. Under the high electric fields, most of the CDF occur in the gate oxide and dielectric layers of protection circuits and neighboring I/O buffers [3, 5, 7, 8]. A high electric field can be easily formed across the dielectric at these destructive sites because they are in the discharge path, where the current can be collected from many metal lines.

A macromodel includes a set of simulation variables such as package capacitances, internal capacitance, and the finite resistance of power metal. In addition, the CDM macromodel focuses on ESD protection circuits, input and output buffers, as shown in Fig. 5(a). Other functional devices are simplified into lumped capacitors C_{DS} between the power and ground nets. This simplification is justified by the fact that all the overstress are injected through the power and ground nets. Hence, I/O buffers and protection circuits located in the boundary of the subsystem are attacked and fail ahead of internal components.

Equivalent circuits for protection circuits, input buffer, and output buffer are shown in Fig. 5(b), (c), and (d), respectively. For a protection circuit, R_{PC1} represents the lumped resistance of the power net, R_{PC2} represents the lumped resistance of the ground net, and C_{DSPC} represents the effective internal capacitance driven by protection devices. Those parameters are determined by solving the driving point admittance for power and ground net [9, 10, 11, 12]. Similarly, RC parameters are resolved for I/O buffers. It is important to note that all the three components have the same package capacitance C_{DD} and C_{SS}.

The total quantity of charge stored in a chip is related to the area of the internal conductive parts. The quantity of charge is derived from a simple equation $Q = CV$ and CDM test conditions, as shown in the following equation,

$$Q_{CDM} = \varepsilon_0 A_C V_{CDM} \left(t + \frac{T}{\varepsilon_R} \right)^{-1} \quad (5)$$

where A_C is the total area of the internal conductors, V_{CDM} is the CDM charging voltage, ε_R is relative permitivity of resin used for packaging, and T and t are thickness of resin and air gap, respectively. Accordingly, the package capacitance of a macromodel increases as the conductor area in a macromodel increases. The approximate package capacitance of each macromodel is determined by calculating the area ratio of conductors within a macromodel to the total conductor area within a chip.

Partitioning into subsystems and associated macromodels can improve the computational efficiency. In combining procedure to generate a full-chip model, interactions between subsystems are taken into account to maintain the simulation accuracy. Fig. 6 shows the connection of two adjacent macromodels in different power supplies (namely, different power domains). The diode-based power-to-power protections (PPPs) are inserted between two power domains to create ESD current paths. The box represents a power domain crossing circuit (PDCC), which is the interface circuits between different power supplies.

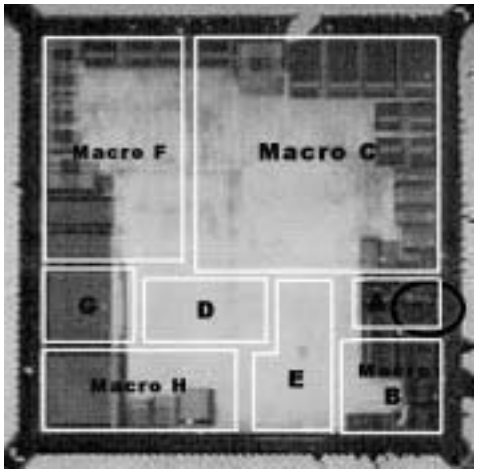

Figure 7: Functional systems of a CMOS ASIC

4. SIMULATION AND EXPERIMENTAL RESULTS

4.1 A Simulation Example

The CDM modeling and simulation methodology described in this work has been applied to several product ICs. As a part of example, a mixed-signal ASIC device processed in a 0.25-μm CMOS technology is presented. The ASIC contains a high-speed I/O interface, data/clock controllers, data converters, embedded static RAM cells, and digital signal processing (DSP) engines. Fig. 7 shows the chip floorplan. In the on-chip power bus architecture with multiple supplies, "power splitting" is employed to distribute different supplies. Each power supply delivers power to all the devices in a functional system. To reduce the complexity of modeling and simulation, a hierarchical approach is employed in such a way that the ASIC is subdivided into seven subsystems (subsystem I $\sim$ VII). Then, each subsystem is converted into a CDM macromodel (Macromodel $A \sim H$). Macromodel A represents a high-speed I/O interface occupying the smallest layout area in this chip. Macromodels C and D denote a DSP, mapped from subsystem III having the largest chip area.

The extracted simulation variables for chip-level CDF analysis are shown in Table 1. The measured total package capacitance is in the range 12.5 to 14.0-pF. The package capacitances for macromodels in the table represent a normalized capacitance ratio of each macromodel when the capacitance of Macromodel A is set to one. All I/O pins are protected by two-stage ESD circuits with a grounded gate nMOSFET (ggNMOS) as the primary protection device. The V_{DD}-to-V_{SS} protection is implemented with an RC-triggered ggNMOS. A symmetric diode string is employed for connecting two different power domains and providing a discharge path.

Table 1: Summary of the variable extraction. * represents the normalized value.

L_P	11.5 nH
C_{pin}	0.64 pF
$C^a_{DD} = C^a_{SS}$	1.0*
$C^b_{DD} = C^b_{SS}$	3.4*
$C^c_{DD} = C^c_{SS}$	10.6*
$C^d_{DD} = C^d_{SS}$	3.2*
$C^e_{DD} = C^e_{SS}$	4.5*
$C^f_{DD} = C^f_{SS}$	9.8*
$C^g_{DD} = C^g_{SS}$	2.5*
$C^h_{DD} = C^h_{SS}$	6.3*
Total package cap. (Meas.)	12.5 $\sim$ 14.0 pF

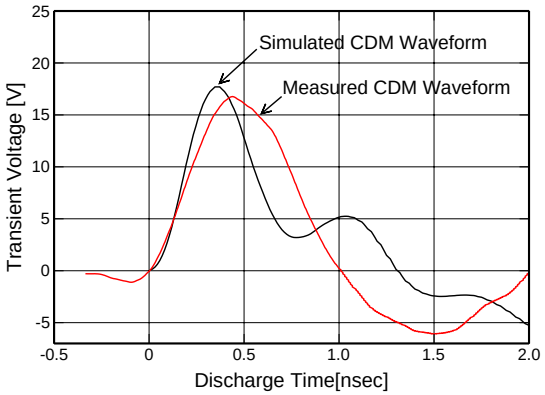

Figure 8: Comparison of measurement and simulation voltages appearing on a grounded pin after application of a 500 V positive CDM stress.

4.2 Simulation Results

Chip-level simulation is performed for analyzing the failure mechanism of a positive CDM event with respect to a stress pin of Macromodel *A*. The simulation can be used to find the maximum tolerable stress in small circuits with a few I/Os by analyzing current waveforms corresponding to all possible stress discharge paths.

Fig. 8 shows the comparison of measurement and simulation for a short rise time CDM pulse. The waveforms are the transient voltages appearing on a stress pin after application of a 500 V CDM pulse. The simulation shows the result of approximately a 400-ps rise time with peak discharge voltage of 18 V, whereas the measurement has a rise time of 450-ps ($\pm$ 80-ps) and peak voltage of 17 V. The simulation matches with the measurement except for a small deviation of the pulse width. In practice, the simulation variables can be either overestimated or underestimated. The main reason for this discrepancy comes from the inaccuracies and distortions resulting from the relay and the voltage probe as well as from dispersion and frequency dependent cable losses affect the measurement of the transient behavior. In addition, for the simplified modeling, we ignore parasitic inductance effect along the PG conductive busses.

The effects of high electric fields and very short pulses which are presented during CDM-ESD pulses on MOSFETs with thin gate oxides have been extensively studied due to their importance in MOS technology [13]. The oxide hardness to ESD pulses has been explained by the 1/E model, referring to the logarithm of time-to-failure as inversely proportional to the applied electric field (or

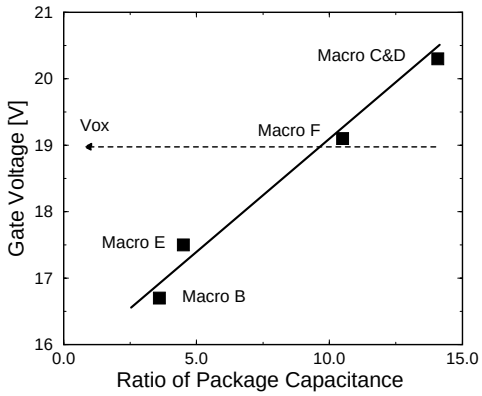

Figure 9: Peak voltages across gate oxides in the PDCC of Macromodel *A* under a 500 V positive CDM stress.

Table 2: Summary of CDM tests.

Device Code	Package Code	Failure Description
CDM1	352-pin PBGA	Functional failures
CDM2	100-pin TQFP	Pass over $\pm$ 1000 V
CDM3	272-pin BGA	Oxide destructions
CDM4	217-pin PBGA	Failures by oxide shorts
CDM5	176-pin PBGA	Oxide destructions

voltage) [14]. The oxide electric field, E_{ox}, of a 3.5-nm oxide for CDM pulse duration of 0.8-ns is extrapolated to 54.5 MV/cm, corresponding to an oxide breakdown voltage of 19.0 V. Using this result, we predict CDF damage by monitoring voltages across all gate oxides during a CDM stress. Fig. 9 shows the voltages across the gate oxides in the PDCC of Macromodel *A* with respect to a stress pin in Macromodel *A*. Note that the induced gate voltages are approximately proportional to the package capacitances of corresponding macromodels. The peak transient voltage is observed at the gate oxide connected to Macromodel *C* and *D* which has the largest package capacitance, as shown in Table 1. The induced voltage exceeds the dielectric strength of the oxide, most likely resulting in a rupture. This result suggests that the reliability of gate oxide must correlate with the package capacitance of connected macromodels. As a result, the gate oxide connected to a macromodel with larger package capacitance suffers severer damage than the gate oxide with smaller package capacitance for a given CDM stress voltage. Note also that the gate oxide is more susceptible to damage when a pin in a macromodel with the smallest package capacitance is grounded.

4.3 Experimental Results

The proposed method can easily be applied to the CDM failure mechanism analysis (FMA) of any product ICs. The products and the relevant test results are listed in Table 2. The failures occurring below 500 V have been observed in three ICs. The results usually show various failure modes. Some failure modes have been randomly observed throughout a whole chip so that the hierarchical analysis hardly predicts the failure locations and their mechanisms. The most susceptible locations against CDM stress are the gate oxides of input circuits neighboring I/O protection circuits. The next frequently observed failure mode is the gate oxide rupture around the interface circuit located between different power-ground nets.

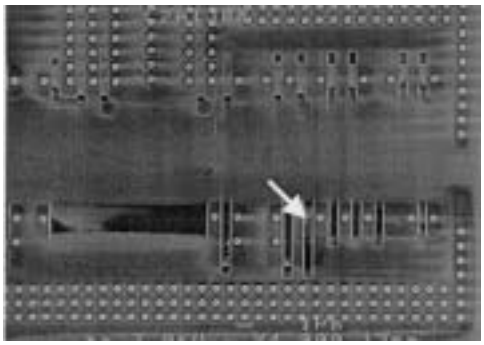

Figure 10: SEM photograph of gate-oxide damage observed after removing the poly layer

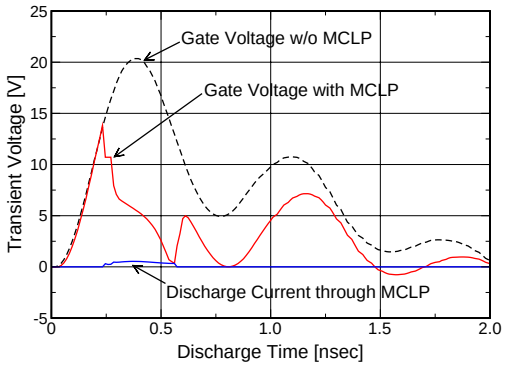

Figure 11: Simulated gate voltage waveforms with and without a clamp device M_{CLP}.

Direct charge CDM tests were performed for various positive and negative voltages. While I/O protection and power protection circuits withstand CDM stress of over 1000 V, the overall CDM robustness of the ASIC is lower than 500 V. Emission microscopy was carried out by inspection of the static *Idd* failure location. Fig. 10 shows SEM views of internal gate oxide destruction observed in the power domain crossing circuit of Macromodel *A* which our chip-level simulations predicted. The gate edge on the source side was damaged and appeared to be melted.

To protect the gate oxide from being damaged, an alternative discharge path, comprised of a ggNMOS M_{CLP} and resistor R_{CDM}, is placed in front of the vulnerable gate oxide. Fig. 11 shows the influence of the protection circuit on the gate oxide protection. Just beyond the turn-on voltage of the protection circuit, the charge transferred from the Macromodels *C* and *D* is discharged through protection device M_{CLP}, and as a result the gate voltage is clamped to a voltage less than the oxide breakdown voltage BV_{OX}. With careful layout design and CDM protection circuits in front of sensitive gate oxides predicted by simulation, the overall CDM performance exceeds 750 V.

5. CONCLUSIONS

Even it may not be well appreciated, estimated ESD failure has been ranked among the top three problems in the state-of-the-art VLSI chip manufacturing. The CDM is the major failure cause of LSIs among various type of ESD failures. One crucial prerequisite of CDM-ESD protection engineering is an efficient and accurate CDM-ESD model in order to identify stress-sensitive components in early design stages. However, it is computationally prohibitive to simulate the CDM behavior of a chip based on such *circuit-level* models.

In this paper, a new methodology was proposed to simulate *full-chip* CDF for a system-on-a-chip with multiple supplies. Hierarchical approach to chip modeling and CDM macromodels yields manageable netlists while generating very accurate prediction to CDF. This hierarchical approach associated with novel macromodel for each subsystem can be easily incorporated into the physical design phase and applied to any complicated chip with multiple functional blocks and power supplies. Chip-level modeling and analysis allow one to investigate the impact of package capacitance and power protection networks on the CDM performance. Thus, this method can help a designer to find vulnerable internal gate oxide in early design stages. We verified our methodology with CDM test results for a CMOS ASIC fabricated on a 0.25-μm technology. As predicted in our simulation results, an oxide destruction was identified in the test chip using a scanning electron microscope.

6. ACKNOWLEDGMENTS

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