CMOS: A Paradigm for Low Power Wireless?

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ABSTRACT

An overview and comparison of different topologies for wireless architectures are discussed, where the main focus lies on the power consumption and possibilities towards integration and reduction of external components. Architectures with reduced number of building blocks (both internal and external) are presented where the main benefits are the low costs, both in the CMOS technology as well as the power.

Categories and Subject Descriptors

B.7 [**Hardware**]: Integrated Circuits

General Terms

Design

Keywords

CMOS Wireless receivers Low-power

1. INTRODUCTION

The super heterodyne receiver has had a good run. It has been the basic workhorse for most RF designs since the 1920s. But many RF designers have been wooed by the idea of dispensing with the cumbersome bundle of filtering, oscillator and frequency-synthesis parts that make up a superhet. Those parts are needed to convert the signal received at the antenna to an intermediate frequency (IF), and ultimately to the baseband level. Direct conversion receivers are freed of the IF stage and, in principle, of the circuitry that comes with it. The transition to direct conversion has picked up pace across a number of wireless application areas. The technique has been easy enough to deploy in systems such as RF ID products, for example garage-door controls and pagers. But they use simple modulation schemes, with relatively easy-going requirements for interference rejection and error rates. There are far more performance related barriers to break through when it comes to modern wireless standards such as GSM. Direct-conversion technology has been slower to penetrate here, although it now accounts for roughly a quarter of GSM phones currently in use.
Zero and low-IF designs are a far simpler proposition in the wireless LAN arena because standards such as Bluetooth and 802.11b have looser requirements in terms of channel filtering compared with GSM. No-one seems to be developing superhets for wireless LANs. Developers of third-generation handsets are expected to pursue direct conversion aggressively, largely because the handsets will need to support both GSM and either flavour of CDMA.
A parallel move to direct conversion is the use of CMOS RF circuitry. It is a research avenue that entered the frame once CMOS geometries had shrunk enough to support gigahertz frequencies. Since "sub-quarter-micron" technologies now come readily available from the main foundries, the amount of full CMOS wireless products available on the market is also clearly rising.[7, 8, 9, 10]
Both price and power consumption are major driving forces for the commercial breakthrough of wireless products. This paper addresses the feasibility of the cheaper CMOS technology as the choice for low power wireless circuit implementation.

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2. WIRELESS ARCHITECTURES

The choice of a suitable wireless architecture can have a direct impact on the overall power consumption. On one hand there are the popular and reliable multi-stage down conversion architectures. On the other hand architectures with a reduced number of down conversion stages have gained interest due to their power saving potential.

Heterodyne receiver

The best known and most widely used architecture is the heterodyne receiver, depicted in Fig. 1. This receiver employs one to multiple stages of an image-reject filter, a mixer and a variable gain amplifier block. Due to the required high quality factors of the image reject mixers, these are generally implemented off-chip. The drawback of implementing off-chip components, apart from the cost increase, is the increased power consumption. These blocks have to be driven with a characteristic impedance (typically 50Ω). Driving signals at or near the RF frequency with such an impedance requires power hungry driver blocks. The implementation of a increasing number of cascaded down conversion stages will generally also be reflected in the overall power consumption.

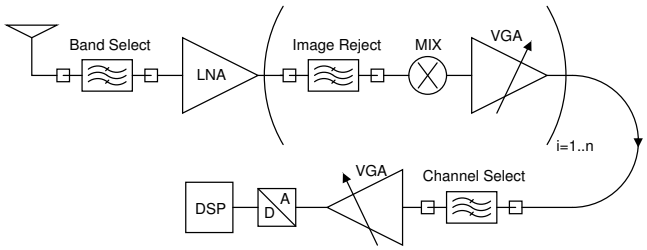


Figure 1: General schematic of the heterodyne receiver

Zero IF receiver

The zero-IF receiver has also been around for a long time [5]. This receiver, also known as a "homodyne" or "direct conversion" receiver, as depicted in Fig. 2 has proven to be a good alternative to the previously described heterodyne receiver. In this architecture, the frequency of the local os-

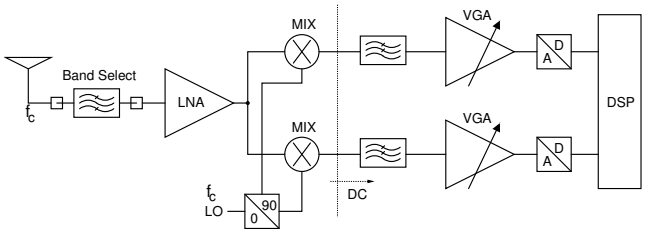


Figure 2: General schematic of the zero IF receiver

cillator signal is equal to the carrier frequency. The advantage being that the wanted signal and the image signal are the same, seriously relaxes the Image Rejection Ratio requirements. The use of an off chip image reject filter is no longer required and hence the LNA no longer needs to drive a 50 Ohm load. The channel select filters of the heterodyne receiver are replaced by low-pass filters that can be implemented on chip. All these properties lead to an architecture with a reduced power consumption.
The major drawback of this architecture, however, is the generation of DC offsets in the downconverted signal, due to self-mixing in the down-conversion mixers, even order distortions and 1/f noise sources. These offsets can easily saturate the amplifiers and filters at the end of the receive chain.
Different strategies, including tuning, trimming, adaptive offset corrections, frame-by-frame corrections,... have been employed to counter this problem [1].

Low IF receiver

A number of other architectures has been developed [13, 2], but only one has found its way from the academics into the commercial market in a number of designs.
The low IF receiver, while having different possible implementations, can generally be represented by Fig. 3. This architecture combines the advantages of the previously discussed receivers into a single analog down conversion stage with reduced power consumption without the DC offset problems. The IF frequency is slightly higher than DC, so the

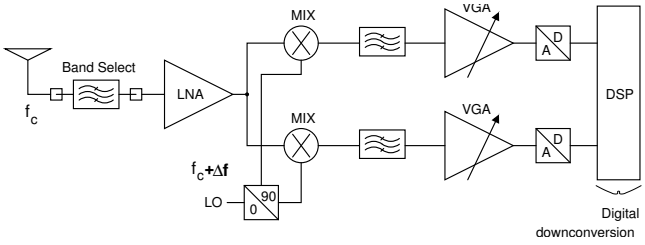


Figure 3: General schematic of the low IF receiver

wanted signal is not corrupted by DC offsets, nor by 1/f noise. The RF image rejection is performed by the I/Q down conversion mixers, which can be implemented as quadrature down converters or double quadrature down converters[4]. The channel selection is performed by the polyphase filter, which also aids the image rejection of the final down conversion to DC, as well as relaxing the dynamic range requirements on the AD converter stage.

3. LOW POWER CMOS WIRELESS RECEIVER IMPLEMENTATION

This section discusses a CMOS implementation example of a low power wireless receiver for GPS applications. The low IF architecture has been chosen for its good power performance.
The implemented receiver topology is shown in Fig. 4. The

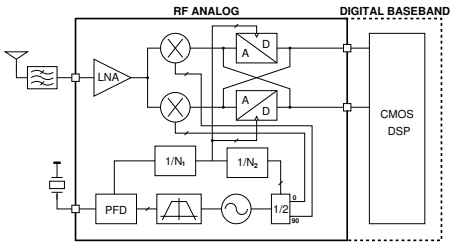


Figure 4: High Level receiver topology

receiver consists of an LNA connected to a switched mixer followed by the AD converter. By using a wide dynamic range AD converter, the VGA function used in many receivers can be shifted to the digital domain. A $\Delta\Sigma$ AD converter can achieve a sufficiently high dynamic range while not exaggerating the power consumption. The front-end converts the RF-signal to digital I and Q signals in a 2 MHz BW centered at 4MHz. The RF mixers are switched with a quadrature LO-signal derived from a VCO running at 3.14GHz followed by a divide-by-2 block. The RF-signal is quadrature down converted by mixers connected directly to the input of the A/D converter. The loop filter of the AD converter is a complex bandpass loop filter which has an asymmetric frequency response for its noise shaping function. The output of the receiver is a digital I and Q bitstream at a bit-rate of 128 MHz.
An anti alias filter in front of the ADC is not necessary anymore because the continuous time loop filter attenuates out of band signals before any signal sampling occurs, as opposed to the switched implementations [17], and is therefore left out.

The different building blocks are discussed next.

3.1 LNA

As seen in Fig. 4 the LNA is only preceded by the antenna and an external blocking-filter. This means no amplification of the signal has been performed before it reaches the input of the LNA. Therefore, the LNA is designed to have a very low noise figure since it sets a lower bound for the total receiver noise figure. The circuit schematic of the LNA is shown in Fig. 5.

A high voltage gain is necessary to sufficiently reduce the

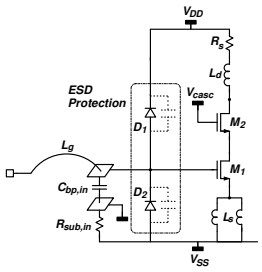


Figure 5: LNA circuit schematic

noise contribution of following mixer block. The low noise figure and high gain are provided by a single-ended common-source amplifier with inductive source degeneration. The cascode transistor reduces the Miller-effect, increasing the stability of the amplifier. It also increases the reverse isolation so that LO leakage to the antenna is minimized. The load of the LNA consists of an inductor which was designed for a high equivalent load resistance R_p, in order to have sufficient voltage gain without jeopardizing the linear operation of the mixer. A patterned ground shield was placed beneath the inductor in order to avoid noise injection and to increase the Q of the parasitic capacitance. To further boost the gain without a penalty in power consumption, the LNA input impedance was designed slightly lower than 50Ω [11]. A ground shield was used for the input bonding pad in order to minimize its capacitance and maximize the Q, which improves noise and gain performance. The input of the LNA is protected against ESD by two reverse biased diodes and a supply clamp.

3.2 PLL

The type II fourth order PLL is shown in Fig. 6[12].

The VCO is built around an on-chip octagonal balanced inductor that is optimized through an in-house inductance simulator-optimizer. The VCO operates at a frequency of 3.14GHz and the quadrature signal is generated from a master-slave frequency divide-by-2. Two DSTC n-latches form a differential dynamic D-flipflop performing the high-speed division. The PLL is locked to a 16.37MHz frequency reference through a divide-by-96 block and a phase frequency detector without dead-zone [6]. The reference frequency spurs are minimized by adding a reference branch in the charge pump core and careful timing of the switch control signals. This way, the charge pump current sources are always on. The current is alternatively flowing in the reference and the output branch of the charge pump. A virtual ground is provided after the charge pump by putting an opamp in the loop filter. This keeps the charge pump switches well in saturation and improves the symmetry between the Up- and the Down- side of the charge pump during locking. For stability reasons, a low frequency zero is inserted in the loop filter. This low-frequency-zero is implemented on-chip without applying any tricks like using a dual-path loop filter [14]. This way, power is saved since we do not need to implement a current summation circuit. This comes at the cost of an increased chip area to implement the loop filter capacitor of almost 2nF on chip.

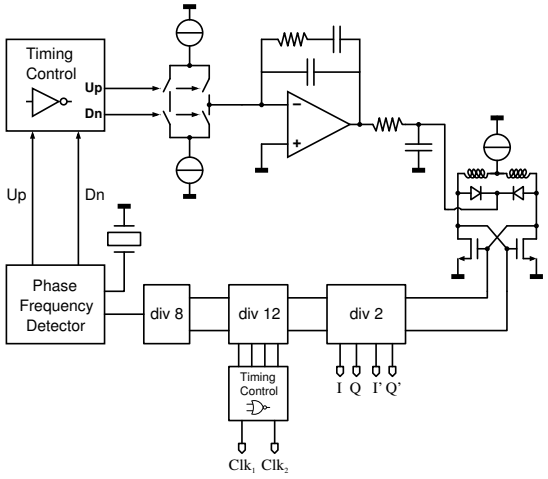


Figure 6: type II PLL schematic

3.3 AD converter

For a given RF down conversion system with an IF frequency BW_c and a bandwidth $2.BW$, different filters can be used to process the IF signal. In the case of a low-IF down conversion stage, the wanted signal is positioned only in the positive frequency band between the frequencies $BW_c - BW$ and $BW_c + BW$. It can be shown [16] that the estimated power consumption of a filter at the low IF frequency is proportional to the width of the passband, integrated over both positive and negative frequencies. Therefore, a quadrature bandpass filter will have the lowest power consumption, as compared to a low pass or regular bandpass implementation. On the other hand, since a low IF receiver as shown in Fig. 3 will have only one VGA stage, a power decrease can be expected when this VGA function is covered by extra dynamic range in the AD converter, in case the extra power necessary for the DR increase in the AD converter doesn't supersede that of the VGA stage. This will of course depend on the system specifications.

3.4 $\Delta\Sigma$ implementation with complex bandpass filter

Figure 7 depicts the equivalent schematic of a first order $\Delta\Sigma$ ADC with a complex bandpass filter. K_R,G_R and K_C,G_C are respectively the real and imaginary feedback coefficients and determine the poles and zeros in the noise transfer function. The indices $''R''$ are used for "real" coefficients, e.g. the coefficients which represent the feedback from an I(Q) node to an I(Q) node, whereas the "complex" $''C''$ indices indicate the coefficients of the feedback from an I(Q) node to a Q(I) node. Note that in the latter case the sign of the feedback coefficient is different for the "I-to-

Q" feedback and the "Q-to-I" feedback. The complex noise transfer function of this modulator has a pole at $-(G_r + K_r).gbw - i(G_c + K_c).gbw$ and a zero at $-K_r.gbw - K_c.gbw$, where gbw is the GBW of the integrator. This can be generalized for higher order loop filters

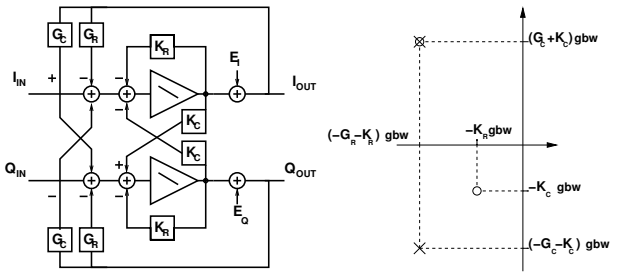


Figure 7: Simplified first order complex ΣΔ (l); poles and zeros plot (r)

3.4.1 ΔΣ architecture

In figure 8 the full ΔΣ architecture is depicted. The loop-filter is a second order complex bandpass filter consisting of two cascaded integrators and two feed-forward OTAs as shown in figure 8. Both blocks of the cascaded structure introduce complex non-conjugate poles at two different frequencies in order to guarantee a broad quantization noise suppression band under varying process conditions. For given specifications, optimal pole positions can be determined. The feed-forward OTAs introduce zeros in the filter frequency characteristics and guarantee the stability of the ΔΣ loop at higher frequencies.

First filterblock

The first filter slice is shown in Fig. 9. The first filter block is implemented as an RC filter and is the most important block in the loop-filter for noise and linearity considerations. The input resistor linearizes the ota transconductance and the degeneration loop gain $gm * Rin$ has to be high enough for the good functionality both in the strength of the virtual ground and the linearization of the transconductance.

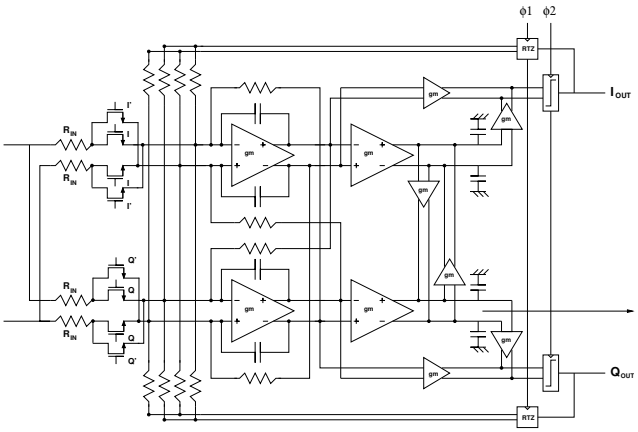


Figure 8: mixer-ΔΣ architecture

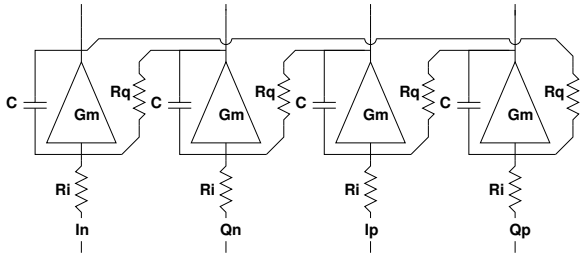


Figure 9: first filter slice

The complex feedback, shifting the integrator characteristic to a complex bandpass filter, is done by the R_Q resistors which are coupled between the outputs of the I(Q) phases and the inputs of the Q(I) phases. The input voltage-to-current conversion is mainly performed by the input degeneration resistor requiring no extra components. The 2kΩ input impedance does not provide a considerable loading on the preceding block. The value of the resistor determines the NF of the entire receiver.
The first OTA is a folded cascode transconductor as shown in Fig. 10. The output common mode voltage is controlled

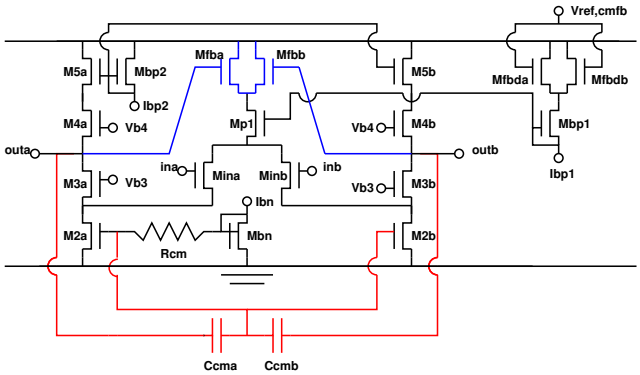


Figure 10: First filter slice ota with CMFB

by both a high frequency feedback loop and a low frequency feedback loop. The first loop is closed by the transistors $M_{fba,b}$ and controls the I_{bp1} biasing. Although reducing the available headroom, this approach is feasible because of the small signal swing level in this receiver AD converter. The GBW of this loop is always smaller than the GBW of the OTA, therefore a second parallel loop with high GBW is needed as well. This loop is closed by the $C_{cma,b}$ capacitors and controls the I_{bn} biasing source. The open loop CMFB transfer function of this loop has a band pass characteristic. The capacitor value is a tradeoff between extra capacitive load on the output and the open loop CMFB gain.

Second filter block

The second filter slice is shown in Fig. 11. The filter is implemented as a gmC filter. The complex feedback is performed by transconductances, which are coupled between I and Q phases. These transconductances have their inputs connected to the outputs of the I(Q) filter stage and their outputs are summed together with the outputs of the Q(I) integrator transconductances.

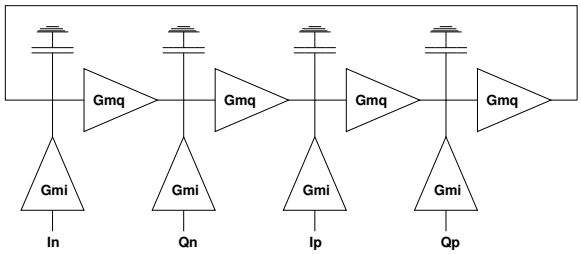


Figure 11: second filter slice

The power requirements for the second filter block are much more relaxed, particularly the noise and linearity specifications are lowered by the gain of the previous block. A simple low power gmC filter implementation with a minor degeneration loop gain is suitable.

The OTAs in the second stage are folded cascode transconductors, similar to the circuits used in the first stage. This is shown in Fig. 12 where the currents of the degenerated transconductances marked "I" and "Q" are summed.

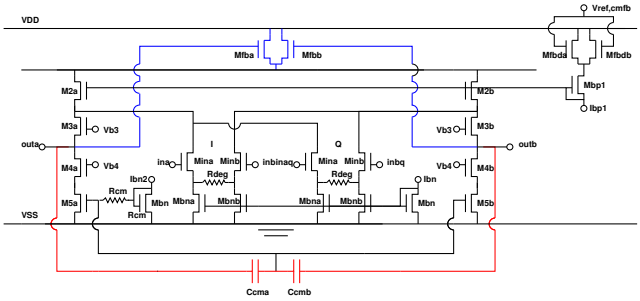


Figure 12: Second filter slice ota with CMFB

The CMFB of this stage is implemented in the same way as in the first stage.

Input stage

The input of the ADC is a summing point for both the IF input signal and the DAC return-to-zero [3] feedback pulses. In this continuous time implementation this is done by current summation on that node. Resistors R_{in} placed between the input of the system and the low impedant ADC input provide the necessary V-I conversion of the input signal. The down conversion is performed by the switching transistors in series with the input resistors. The transistors are connected to the virtual ground inputs of the loop filter. The I and Q LO drive signals are square-waves and can be derived from a PLL. The switches have a much lower on-resistance than the value of the input resistor in order to achieve a very linear mixing operation.

The value of this resistor R_{in} determines the NF of the entire receiver $\Delta\Sigma$ architecture. The linearity is determined by the loop gain of the input transconductance degeneration. This implies that for a certain NF, the power drain in the filter ota is proportional to the desired DR.

In receiver architectures, a single-ended input signal is often preferred to a differential one in order to save power. Both single ended and differential signals can be applied to the input of the AD converter. In the latter case, the CMFB has to be good enough to ensure the necessary single-ended-to-differential conversion and to maintain the linearity requirements. At the dummy input node a replica of the previous block (LNA) output has been placed to make the structure loading as symmetrical as possible. Due to this design choice power and area of an extra active balun at RF frequencies are saved.

Comparator

The comparator[15] is shown in Fig. 13. The feed forward blocks of the loopfilter (B1,B2) are indicated on the left. the cascode transistors $M_{cpp,n}$ reduce the comparator kickback effects. The signals at the output of the comparator are sampled in the SR flip flop.

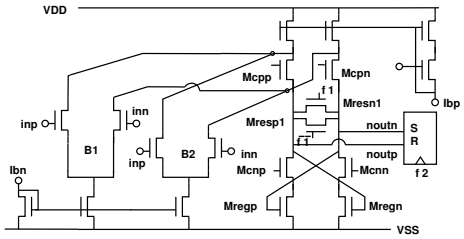


Figure 13: Comparator circuit

4. MEASUREMENTS

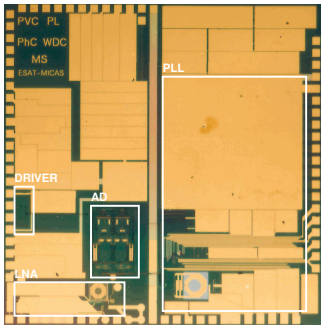


Figure 14: Chip photograph of the receiver

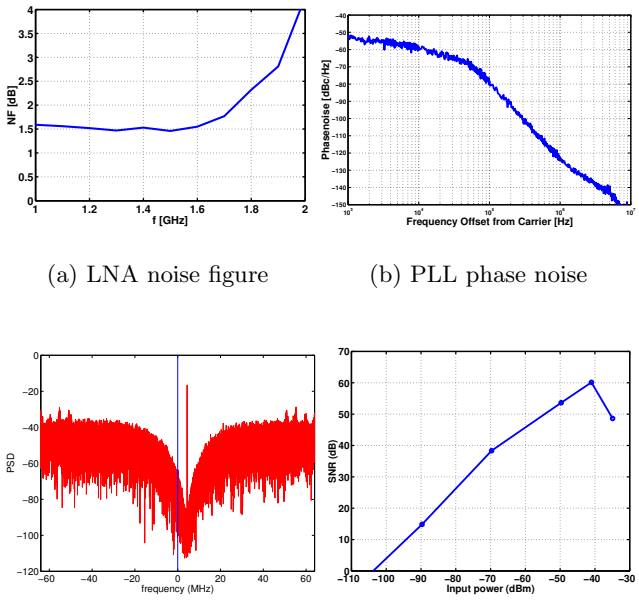
In fig. 14, a photograph of the quadrature modulator receiver with the most important building blocks indicated is shown. It is laid out in a $0.25\mu m$ CMOS process.

The Noise figure vs. frequency of the LNA is shown in Fig. 15(a). The NF at 1.57GHz is 1.5 dB. The LNA consumes 4 mA.

The PLL phase noise is as low as -115 dBc/Hz at 600kHz offset and -138 dBc/Hz at 3MHz offset. Fig. 15(b) presents the PLL phase noise measured at 1.57GHz. The PLL has a locking range of 10% around the center frequency of 1.57GHz. The full PLL consumes 8.5 mA.

The demodulated baseband output spectrum $(I + jQ)$ for a 1.57 GHz input signal at this frequency is shown in Fig. 15(c). The output SNR for increasing input signal levels is shown in fig. Fig. 15(d).

The performance is summarized in Table 1.



(a) LNA noise figure

(b) PLL phase noise

(c) Demodulated baseband output spectrum

(d) Output SNR vs. input power levels

Figure 15: Measurement results

Signal path	
Input Sensitivity (100 Hz)	-130 dBm
Maximum Signal Level	-68 dBm
Specifications	
NF LNA	1.5 dB
DR	62 dB
IMRR	32 dB
Power dissipation	
LNA	8mW
ADC	14.2mW
PLL/VCO	17mW
LO-buffer	2mW
Implementation	
Die area	16 mm^2
Technology	0.25μm CMOS

Table 1: Summary of measurements results

5. CONCLUSIONS

An overview and comparison of different topologies for wireless architectures has been discussed. The low IF topology, as a good candidate for low power wireless receiver integration has been highlighted. An implementation of a fully integrated GPS receiver has been shown as an example of a wireless low power design in a CMOS technology.

6. ACKNOWLEDGEMENTS

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