# **Combined BEM/FEM Substrate Resistance Modeling**

E. Schrik

Delft University of Technology
DIMES / Circuits & Systems Group
Mekelweg 4, 2628 CD, Delft, The Netherlands
eelco@cas.et.tudelft.nl

N.P. van der Meijs Delft University of Technology DIMES / Circuits & Systems Group Mekelweg 4, 2628 CD, Delft, The Netherlands nick@cas.et.tudelft.nl

## **ABSTRACT**

For present-day micro-electronic designs, it is becoming ever more important to accurately model substrate coupling effects. Basically, either a Finite Element Method (FEM) or a Boundary Element Method (BEM) can be used. The FEM is the most versatile and flexible whereas the BEM is faster, but requires a stratified, layout-independent doping profile for the substrate. Thus, the BEM is unable to properly model any specific, layout-dependent doping patterns that are usually present in the top layers of the substrate, such as channel stop layers. This paper describes a way to incorporate these doping patterns into our substrate model by combining a BEM for the stratified doping profiles with a 2D FEM for the top-level, layout-dependent doping patterns, thereby achieving improved flexibility compared to BEM and improved speed compared to FEM. The method has been implemented in the SPACE layout to circuit extractor and it has been successfully verified with two other tools.

# **Categories and Subject Descriptors**

I.6.5 [Simulation and Modeling]: Model Development— Modeling Methodologies; B.7.2 [Integrated Circuits]: Design Aids—Verification; I.6.4 [Simulation and Modeling]: Model Validation and Analysis

## **General Terms**

Verification, Design

# Keywords

substrate noise, modeling, finite element method, boundary element method

#### 1. INTRODUCTION

In present-day micro-electronic designs, substrate noise can have a significant impact on the functionality of the

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for pro£t or commercial advantage and that copies bear this notice and the full citation on the £rst page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior speci£c permission and/or a fee.

*DAC* 2002, June 10-14, 2002, New Orleans, Louisiana, USA. Copyright 2002 ACM 1-58113-461-4/02/0006 ...\$5.00.

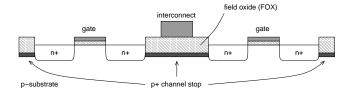


Figure 1: Highly doped (p+) channel-stop layer increases  $V_T$  of the parasitic FET being formed under the Oxide.

design. For example, in a mixed-signal design, the noise injected into the substrate by the digital part can seriously influence the functionality of the analog part. Thus, accurately modeling the behaviour of the substrate as a "noise-propagator" is becoming ever more important in the field of layout-to-circuit extraction [1, 2, 3, 4, 5, 6, 7, 8]. Basically, there are two principal ways of obtaining such a model: the Finite Element Method (FEM; applied in e.g. [6]) and the Boundary Element Method (BEM; described in e.g. [5]). The FEM, which makes a full, in-depth 3D discretization of the substrate, is usually slow, but very versatile and flexible, whereas the BEM, which only discretizes the contact areas on the boundary of the substrate, is much faster but requires a uniform, stratified substrate.

However, in many cases, a uniform stratified substrate is not a realistic assumption, because specific, layout-dependent doping profiles in the top-layers of the substrate are widely applied. An example of this is presented in Figure 1. It actually shows two layout-dependent doping patterns, i.e. the channel-stopper and the source/drain diffusions. Other examples include trenches, sinkers and buried layers.

While FEM based modeling could accurately model such structures, it can often be too slow. On the other hand, the BEM might not always be accurate enough. Therefore, we have developed a combination of BEM and FEM that is faster than FEM but can be more accurate than BEM based methodologies. We describe a new combination of BEM and FEM for substrate resistance extraction, but note that other BEM/FEM combinations can be found in the literature, see e.g. [9]. Reference [10] presents a combined BEM/FEM approach to capacitance extraction.

In fact, we have developed a 3D BEM/2D FEM combination. That is, we treat the top layer of the substrate as 2 dimensional. This will even be faster than a 3D BEM/3D FEM combination, and we show, by comparison of results obtained by our method to those obtained with Momentum [11] and Davinci [12], that in many practical situations the

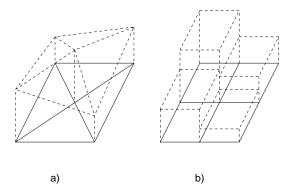


Figure 2: A triangular mesh with a piecewise linear potential distribution for the FEM (a) and a rectangular mesh with a piecewise constant current distribution for the BEM (b).

accuracy is still good enough. The method has been implemented in the SPACE layout-to-circuit extractor [13].

This paper is structured as follows. Section 2 will briefly present some relevant background information on the FEM and BEM methodologies. Section 3 describes our new method. Section 4 presents comparisons of our new method, as implemented in the SPACE layout-to-circuit extractor, to the two other tools mentioned above. Finally, Section 5 states our conclusions.

#### 2. BEM AND FEM BACKGROUND

The finite element method in its simplest form subdivides the conductor domain into triangles (or tetrahedrons in the 3D case) and approximates the potential distribution in the conductor domain by a piece-wise planar (1st order) function that is defined over these triangles (see Figure 2a). The minimization of a functional that relates to the consumed energy in the conductor domain is then used as an alternative formulation for the Laplace equation. This is equivalent to modeling each triangle by a delta-type resistor network [14, 15] and solving the final resistances from the relation between the potentials and currents in the total resistor network.

The so-obtained resistor network is sparse. That is, the number of resistors is proportional to the number of nodes in the network. The network solution is typically accomplished by Gaussian elimination, or equivalently, star-delta transformation. All nodes but the terminal nodes (connected to circuit or device ports) are subsequently eliminated. By exploiting the properties of VLSI interconnect patterns, this can be done efficiently [16, 17] without destroying the sparsity of the network too much.

The BEM for resistance extraction [5] is derived from an integral equation form of the Laplace equation. Note that we will here consider the 3D case. The BEM only requires a discretization of that part of the boundary of the domain where (inhomogeneous) Dirichlet conditions hold. These Dirichlet conditions hold at those parts of the boundary where current can enter/leave the substrate (i.e. at the substrate contacts, which can be formed in many ways, see [4, 1]). At the remainder of the boundary, homogeneous Neumann conditions hold.

The BEM uses a so-called Green's function as the kernel

in the integral equation. This Green's function can be interpreted as the potential in a certain point due to a unit current injected somewhere else. In order to approximate an arbitrary current distribution over the Dirichlet part of the boundary, the substrate contacts are discretized into panels and a shape or basis function for the current is assumed. In its simplest form, this models the current as a piecewise constant (0-th order) current distribution (see Figure 2b). That is, the current is constant on each panel but discontinuous between panels. Because of the Dirichlet condition, the potential over a panel must also be constant — the panels form an equipotential region.

Based on this discretization, the collocation method or the Galerkin method [18] can be used to obtain a system of equations with  $\mathbf{U}$  as the vector of N panel potentials,  $\mathbf{X}$  as the vector of (unknown) panel currents and  $\mathbf{G}$  as the elastance matrix describing the potential at panel i due to a unit current in panel j:

$$\mathbf{U} = G\mathbf{X} \tag{1}$$

The BEM then continues by defining an incidence matrix  ${\bf F}$  relating panels and contacts. By denoting  ${\bf V}$  as the contact potential vector and  ${\bf I}$  as the contact current vector, we can write

$$\mathbf{U} = F\mathbf{V} \tag{2}$$

$$\mathbf{I} = F^T \mathbf{X} \tag{3}$$

It follows that

$$\mathbf{I} = F^T G^{-1} F \mathbf{V} = Y \mathbf{V} \tag{4}$$

where  $\mathbf{Y}$  is an admittance matrix for the resistive substrate with the substrate contacts as ports.

Thus, we see that also with the BEM the result is a resistance network. Compared to the FEM, however, this is a full resistance network, and each node is in principle connected to every other node. All the nodes are port nodes; there are no internal nodes. Model order reduction should be used to simplify this network, and/or a windowing technique such as [5] can be used to a-priori extract a reduced order model.

## 3. A COMBINED FEM/BEM METHOD

We will consider layout-dependent doping patterns with the following properties

- 1. they are situated in the top layer of the substrate
- $2.\ \,$  they are thin compared to e.g. the thickness of the epi-layer or their horizontal dimensions
- 3. their resistivity is low compared to the resistivity of the surrounding substrate

Under these conditions, the noise voltages in the neighborhood of such structures are mainly dominated by the shape and resistivity of these structures and the noise current is flowing mainly horizontally along these structures. Thus, we could approximate the substrate behavior locally with a 2D model. Globally, we would still need a 3D model.

The above observation motivates the combination of a local 2D method (i.e. 2D FEM) with a global 3D method (i.e. 3D BEM). In Section 4 we will experimentally investigate the validity of the 2D approach.

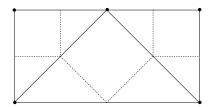


Figure 3: Illustration of a dual FEM/BEM mesh.

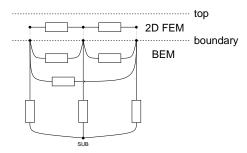


Figure 4: Schematic representation of the combined BEM/2D FEM modeling approach.

For the development of this method, we will consider 1st order elements for the FEM and 0th order elements for the BEM, as they are more common.

Equation 4 actually forces the potential of the panels on the same contact to be equal; contacts form an equipotential region. However, we are free to treat each panel as a separate 'subcontact', also when they touch each other. This corresponds to  ${\bf F}$  being the unity matrix. The result is a full network of resistances with all the panels as ports.

Thus, we can identify nodes in the FEM mesh with panels in the BEM mesh, and it is natural to make the meshes each other's dual. Stated otherwise, with each node of the FEM discretization exactly one BEM panel is associated, which geometrically consists of all the points in the plane closer to this FEM node than to any other FEM node. Thus, a BEM panel is actually the Voronoi polygon [19] of a FEM node. In fact, the dual of the Voronoi diagram, with an edge between each node and all the nodes "closest" to it, is a so-called Delaunay triangulation which is in a certain sense optimal for FEM modeling as it avoids sharp angles.

Figure 3 illustrates two dual meshes. The solid lines form the FEM mesh, while the dashed lines form the dual BEM mesh. Note that, in general, the edges from the Voronoi polygons (i.e. BEM panels) are constructed from the perpendicular bisectors of the Delaunay triangulation on the set of nodes.

Given this correspondence of FEM and BEM discretizations, the resistance networks from both procedures may be connected together, as is illustrated in Figure 4. The result is a mixed sparse/dense resistance network, that will model the current flow in the top and deeper layers of the substrate respectively.

Figure 3 illustrates that the resulting BEM panels are, in general, not rectangular. This is allowed from a theoretical point of view, although it makes the numerical calculation of the entries of the matrix **G**, using either the collocation or the Galerkin method, less efficient. One practical way of performing these computations might be by decomposing

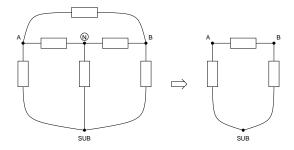


Figure 5: Simple example of the star-delta transformation; by eliminating node N, a simpler but equivalent network remains.

the irregularly shaped BEM panels into independent rectangular and triangular panels and connecting them with the incidence matrix. An alternative solution, but probably less accurate, would be to construct independent FEM and BEM meshes, and to join the associated resistance networks based on proximity of the FEM nodes and, say, the center of gravity of the BEM panels. That is, each BEM panel is associated with the closest FEM node.

The FEM/BEM combination produces a combined resistance network, of which the FEM part is sparse and the BEM part is full. Nearly the simplest of such a combined FEM/BEM network is illustrated in Figure 5a. Here, the resistances between A and N and B and N are parallel connections of a FEM and a BEM resistance, the others are from the BEM only. We assume that nodes A and B are the port nodes, connected to the rest of the circuit. Node N is an internal node.

This network can be simplified using Gaussian elimination or, equivalently, star-delta transformation. The result is shown in Figure 5b. Care should however be taken when interpreting the results quantitatively. This is explained as follows.

Consider the numerical example as in Figure 6. Figure 6a and 6b show the two originally unconnected FEM and BEM networks respectively, where the >> notation means that the value of the resistor is very large compared to the other values. Figure 6c shows the resulting combined network before star-delta transformation. Figure 6d shows how the delta network from eliminating the star node N is connected in parallel to the other resistors, and Figure 6e shows the final result.

Now, it is important to note that the resulting direct resistance between A and B (i.e. 41k) is actually larger than the 28k from the FEM method alone. Thus, by connecting a BEM network to the FEM network, the direct resistance is actually increased. This possibly counter-intuitive fact can be understood by noting that there is also a path from A to B via node SUB. After elimination of SUB, the resistance between A and B would actually be smaller than the 28k obtained from the FEM. In addition, a more detailed analysis shows that when adding more internal nodes the value between A and B actually converges to still greater values.

Furthermore, note that it may not be allowed to eliminate node SUB when it is connected to a bias or ground supply. In that case, the coupling between A and B in Figure 6e would actually be weaker than in the pure FEM case of Figure 6a. This is however precisely what is intended and accomplished by fixing the substrate potential.

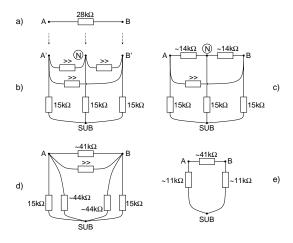


Figure 6: Illustration of star-delta transformation for combined FEM/BEM network

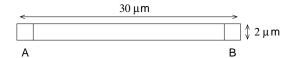


Figure 7: A simple strip of channel-stop with terminals A and B at the ends.

#### 4. **RESULTS**

We have implemented the new method as described above in the SPACE layout-to-circuit extractor and performed a number of experiments to assess the validity and efficiency of the method.

The convergence behavior as discussed in Section 3 is actually confirmed in the following experiment. Consider the layout shown in Figure 7. It represents a line of channelstop which has terminals A and B at the ends. The line is  $30 \,\mu m$  long,  $2 \,\mu m$  wide and  $0.5 \,\mu m$  thick, and it has a sheet resistivity of  $2000 \Omega/sq$ . The substrate is uniform with conductivity of 10 S/m and a thickness of  $250 \,\mu m$ , with a backplane metalization. The corresponding terminal in the netlists is called 'SUB'. The FEM resistance between A and B (i.e. for the channel stop alone) is 28K. Table 1 shows the result of the combined FEM/BEM method for an increasing number of discretization sections, as indicated in the first column labeled '#'. Columns 2-4 give the resistor values in the extracted netlist. The last column presents the effective resistance value if node SUB would be eliminated. Both columns 2 and 5 clearly show convergence behavior, as also illustrated in Figure 8.

We have verified the results above with Momentum [11], a 2.5D EM simulator for passive circuit analysis. The results

Table 1: Resistances in  $k\Omega$ . R(A,B) $R_{eff}(A,B)$ R(A,SUB)R(B,SUB)16.93 8.1458.146 8.302 26.90 9.6329.78511.283 34.09 10.17 10.28 12.784 37.63 10.42 10.50 13.455 41.07 10.58 13.99 10.6444.91 10.81 10.85 14.61

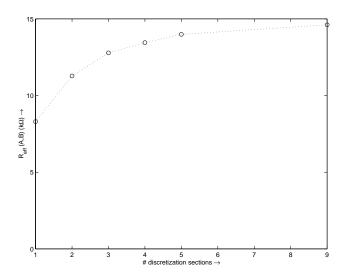


Figure 8: The effective resistance between nodes A and B under increasing refinement.

were as follows:

$$R(A,B)$$
 R(A,SUB) R(B,SUB) R<sub>eff</sub>(A,B)  $40.3 kΩ$   $11.0 kΩ$   $11.2 kΩ$   $14.3 kΩ$ 

Clearly, this data is consistent with the SPACE data for the finer discretization levels.

Figure 9 compares the results of our method, as implemented in SPACE, with those of Momentum as a function of channel stop resistivity. The results were obtained using a 9 section discretization for SPACE and we ensured that the Momentum mesh was comparable (by visual comparison) to the SPACE mesh. Upon varying the resistivity of the channel stop layer from  $100\,\Omega/\mathrm{sq}$  until  $10,000\,\Omega/\mathrm{sq}$ , we see a slight increase of the error, but the difference stays within 6%.

Figure 10 shows another layout where the channel stop region is only located in the middle between A and B but not directly connected. A and B are still of size  $2 \, \mu m \times 2 \, \mu m$  and  $30 \, \mu m$  apart (center to center). The channel stop region is of size  $w \times w$  and has resistivity  $1000 \, \Omega/\mathrm{sq}$ .

We have varied w between  $0 \mu m$  (no island present) and  $24 \mu m$ , and we have calculated the resistance network between A, B and SUB again, with both SPACE and Momentum. The results can be found in Figure 11. We can see clearly that SPACE and Momentum both show similar behaviour; the difference is typically within 8%. As it appears, there is some offset between SPACE and Momentum. At this moment, we are not yet able to fully explain this offset, but it might be caused by a minor difference in the handling of the terminals (A and B).

Both our new method as well as Momentum both model the channel-stop layer on top of the substrate and cannot accurately model an actual doping pattern in the substrate. Therefore, we have to investigate how good this is as an approximation. This investigation was performed by comparing our method to Davinci [12], a 3D FEM device simulator.

Davinci, because of its adaptation to the task of device simulation, severely limits the size of the structure that can

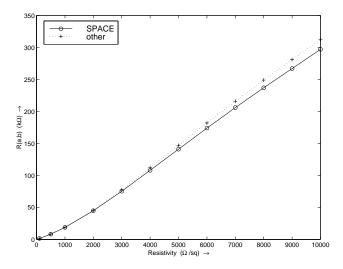


Figure 9: The direct resistance between terminals A and B for increasing values of the resistivity of the channel-stop strip (see Figure 7).

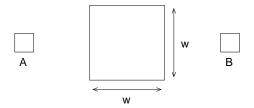


Figure 10: Basic setup of the "island" structure. The parameter "w" determines the size of the island, while keeping it square.

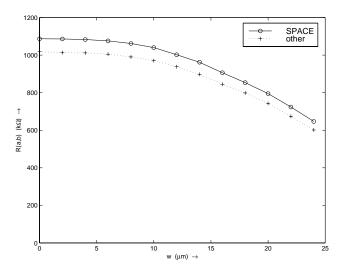


Figure 11: Direct resistance between terminals A and B for increasing values of w (see Figure 10).

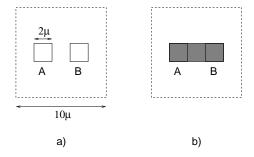


Figure 12: Top view of the experiment setup for the comparison between SPACE and Davinci. a) 2 separate terminals, b) 2 terminals "connected" by highly doped pattern

Table 2: Resistance values and computation times for different experiments.  $R_{AB}$  = resistance between terminals A and B,  $R_{AS}$  = resistance between terminal A and the backplane.

Experiment	Figure 12a		Figure 12b	
method	SPACE	Davinci	SPACE	Davinci
$R_{AB} (k\Omega)$	187	177	5.22	4.08
$R_{AS}$ $(k\Omega)$	22.2	38.0	21.1	33.0
time (s)	31	351	58	382

be analyzed. We have used a version that is restricted to 30k grid points, and for simplicity we have applied a uniform grid.

The basic layout is shown in Figure 12a. It has two terminals A and B on top of a uniform substrate. All dimensions are (multiples of)  $2\,\mu m$ , the substrate has a conductivity of 10 S/m and is  $5\,\mu m$  thick. Again, there is a backplane metallization. The dashed box in Figure 12 corresponds to the FEM domain boundary. For Davinci, we have assumed n-type silicon with  $N_d=4.6*10^{14}cm^{-3}$ , which should correspond to the conductivity of 10 S/m.

Figure 12a shows the layout without, and Figure 12b with a channel-stop doping. This doping  $(0.5\,\mu m$  thick and with  $N_d=4.6*10^{16}cm^{-3}$  which corresponds to a conductivity of 1000 S/m) will "connect" A and B like in the example of Figure 7.

The results can be found in Table 2, which was obtained using suitable mesh settings such that the results from both methods had converged (Davinci used 26011 grid points). The table clearly shows that the results of the FEM method and the FEM/BEM method are reasonably close. There can be many reasons for the remaining differences, including the fundamental fact that the FEM (Davinci) needs a bounded domain (a cuboid) and the BEM (SPACE) assumes a domain laterally extending to infinity.

The bottom row of the table shows that the new method can be considerably faster.

# 5. CONCLUSIONS

In this paper, we have addressed the problem of how to model layout-dependent doping patterns in the top layers of the substrate. A full 3D FEM method would easily be able to incorporate these doping patterns into a model, but this method is not fast enough for large-scale problems. To increase the speed, a BEM method would be more convenient

to use, but this method is not capable of dealing with the layout-dependent doping patterns.

This paper describes a method that makes a combination between a 2D FEM method for the layout-dependent doping patterns and a 3D BEM method for the lower levels of the substrate. Our main assumptions upon which the validity of this approach is based, are that the layout-dependent doping patterns are thin, and that their resistivity is significantly lower compared to the underlying substrate.

A number of experiments have shown that the results of our method compare very well to those generated by Momentum and Davinci, and that the new method will be a valuable addition to the repertoire of methods/models that are useful for layout-to-circuit extraction.

Our future research will concentrate on determining the limitations of our method and how we can circumvent them. In particular, we will investigate the behaviour of our method when varying the thickness and the resistivity of the specific doping patterns and we will investigate the possibilities of extending our 2D FEM/BEM method to a 3D FEM/BEM method for more accuracy and flexibility. Also, the problem of model reduction for the resulting large, mixed sparse/dense networks will have to be addressed as well.

## 6. REFERENCES

- R. Gharpurey and R.G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 344–353, Mar. 1996.
- [2] R.B. Merrill, W.M. Young, and K. Brehmer, "Effect of Substrate Material on Crosstalk in Mixed Analog/Digital Integrated Circuits," in *IEEE International Electron Devices Meeting*, pp. 433–436, Dec. 1994.
- [3] R. Singh, "A Review of Substrate Coupling Issues and Modeling Strategies," in *Proc. CICC*, pp. 491–498, May 1999.
- [4] X. Aragones, J.L. Gonzalez, and A. Rubio, Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs. Boston: Kluwer Academic Publishers, 1999.
- [5] T. Smedes, N. P. van der Meijs, and A. J. van Genderen, "Extraction of Circuit Models for Substrate Cross-talk," in *Proc. Int. Conf. on Computer-Aided Design*, (San Jose, California), pp. 199–206, Nov. 1995.
- [6] D.K. Su, M.J. Loinaz, S. Masui, and B.A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Electronics*, vol. 28, pp. 420–430, Apr. 1993.
- [7] F.J.R. Clement, E. Zysman, M. Kayal, and M. Declercq, "LAYIN: Toward a global solution for parasitic coupling modeling and visualization," in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 537 – 540, May 1994.
- [8] N.K. Verghese, T. Schmerbeck, and D.J. Allstot, Simulation techniques and solutions for mixed-signal coupling in ICs. Boston: Kluwer Academic Publishers, 1995.
- [9] C.A. Brebbia, The Boundary Element Method for Engineers. Plymouth: Pentech Press, 1978.
- [10] P. M. Dewilde and E. B. Nowacka, "Circuit Models for

- the Hybrid Element Method," in *Proc. Int. Symp. on Circuits and Systems*, (Atlanta, Georgia), pp. IV 616–619, May 1996.
- [11] Momentum, a 2.5 D EM Simulator by Agilent EEsof, see http://eesof.tm.agilent.com.
- [12] Davinci, a 3D Device simulator by Avanti, see http://www.avanticorp.com.
- [13] F. Beeftink, A.J. van Genderen, N.P. van der Meijs, and J. Poltz, "Deep-Submicron ULSI Parasitics Extraction Using Space," in *Design, Automation and Test in Europe Conference 1998, Designer Track*, pp. 81–86, Feb. 1998.
- [14] J.E. Hall, D.E. Hocevar, P. Yang, and M.J. McGraw, "SPIDER - A CAD System for Modeling VLSI Metallization Patterns," *IEEE Transactions on CAD*, vol. 6, pp. 1023 – 1031, Nov. 1987.
- [15] A. J. van Genderen, Reduced Models for the Behavior of VLSI Circuits. PhD thesis, Delft University of Technology, Delft, The Netherlands, Oct. 1991.
- [16] N. P. van der Meijs and A. J. van Genderen, "Delayed Frontal Solution for Finite-Element based Resistance Extraction," in *Proc. 32nd Design Automation Conf.*, (San Francisco, California), pp. 273–278, June 1995.
- [17] A. J. van Genderen and N. P. van der Meijs, "Using Articulation Nodes to Improve the Efficiency of Finite-Element based Resistance Extraction," in *Proc.* 33rd Design Automation Conf., (Las Vegas, Nevada), pp. 758–763, June 1996.
- [18] R.F. Harrington, Field Computation by Moment Methods. New York: The Macmillan Company, 1968.
- [19] F.P. Preparata and M.I. Shamos, Computational Geometry: An Introduction. Springer Verlag, 1985.