On the Efficacy of Simplified 2D On–Chip Inductance Models†

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ABSTRACT

Full three–dimensional (3D) inductance models of on-chip interconnect contain an extremely large number of forward coupling terms. It is therefore desirable to use a two–dimensional (2D) approximation in which forward couplings are not included. Unlike capacitive coupling, however, truncating mutual inductance terms can result in loss of accuracy and even instability. This paper investigates whether ignoring forward couplings is an acceptable choice for all good IC designs or if full 3D models are necessary in certain on-chip interconnect configurations. We show that the significance of the forward coupling inductance depends on various aspects of the design.

Categories & Subject Descriptors

B7.2 [**Integrated Circuits**] Design Aids – *simulation, verification*

General Terms

Theory, algorithms

Keywords

On-chip inductance, PEEC, sparsified model

1. Introduction

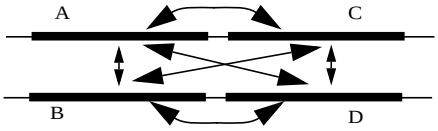
Although accurate analysis of the RLC interconnects can be performed based on the Partial Element Equivalent Circuit (PEEC) method [10], the full PEEC models obtained by three dimensional field solvers (refer to [6][7][8][9]) often produce an intractable complexity problem for subsequent analyses. Several approaches have been proposed to tackle the problem by extracting *sparsified* inductance matrices [11][12][13][14][15]. Recently, novel approaches for modeling the inductive effect based on a new type of circuit element *K (*susceptance*)* were proposed [16][17] that can be used to facilitate sparse, localized window–based inductance extraction models [17].

Inductance sparsification approaches based on truncation or approximation of forward coupling elements have been applied recently for both modeling and analysis [3][4][5]. In [3], a partial circuit model was proposed in which mutual inductance elements are included only if they are between parallel wires. In [4], the authors utilized a similar truncation approach for inductance modeling of shielded clock trees. An interesting 2D model was proposed for parallel wires in [5]. The authors first extract the total self and coupling inductance of the whole wires. A fraction of the total inductance value is then assigned to each bundle of segments as self and parallel inductance. Since in these circuit models, inductance coupling only exists in the two dimensions perpendicular to the current flow, we refer to them as two–dimensional (2D) models. Clearly, the complexity of the inductance modeling problem can be substantially reduced by using 2D models. However, the accuracy of the 2D models is not adequately justified, and only some experimental results have shown a good match for the specific types of circuits in [4][5].

In this paper we present a theoretical analysis of the 2D modeling error. We show that for long on-chip busses, where the inductance effects are typically most pronounced, the magnetic field generated resembles that of dipoles due to close-by current return paths. Analytical formulas are derived for the forward coupling inductance in terms of both partial and loop (effective) inductance. Furthermore, realistic RLC circuit models are used to analyze the forward coupling effect in real-world on-chip interconnects. Finally, we propose a combined two–dimensional inductance methodology that can provide a better accuracy and efficiency trade-off and, therefore, a practical solution to the modeling and analysis of large interconnect systems.

2. Motivation

Accurate three-dimensional PEEC models for general shaped on-chip interconnects can be obtained via field solver based extractors such as gismo [6], FastCap [7], FastHenry [8], and Raphael [9]. Usually the capacitance and inductance models are extracted separately as matrices, then they are combined to form the PEEC model. A full three-dimensional PEEC model includes a large number of resistors, capacitors, and inductors. Before sparsification, the coupling capacitors and the mutual inductors constitute a dominant portion of the model.



We distinguish three types of coupling (mutual) terms as illustrated using the two wire/two segment example above. The parallel segments in the two wires are perfectly aligned.

- *Parallel coupling:* the capacitive and inductive coupling between the parallel, aligned segments of the conductors. For example, the coupling between segment A and B.
- *Forward self coupling:* the coupling between segments of conductors belonging to the *same* line. For example, the coupling between segment A and C.

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- *Forward mutual coupling:* the coupling between non–aligned segments of conductors belonging to *different* lines. For example, the coupling between segment B and C.

As we know, capacitive coupling is a short range effect. Particularly, the forward self capacitive coupling and the forward mutual capacitive coupling terms are several orders of magnitude smaller than the self and parallel coupling terms for long wires. Moreover, the forward self coupling does not change the total capacitance of a conductor. Therefore, the forward capacitive coupling is known to be negligible. In many situations, even the parallel coupling capacitors beyond immediate neighbors are often discarded due to insignificant relative magnitude.

Unlike capacitance, coupling inductance between conductors reduces very slowly with distance. The long range magnetic coupling presents a vast number of non-negligible mutual terms in full 3D inductance extractions. For a system of N lines with M segments each, a full inductance model includes NM self terms, $(N-1)NM/2$ parallel coupling terms, and $N(M-1)NM/2$ forward coupling terms. The number of the forward coupling terms are no less than the parallel terms as long as each line contains at least two segments. When the number of segments for each wire is increased to improve the accuracy of the discretized model, apparently forward coupling inductance terms will become the major obstacle for runtime and storage efficiency.

3. Two–Dimensional Inductance Models

Two types of methods have been used in practice for the 2D model formulation.The first method is a partitioning and cascading based approach that has been reported in recent publications [3][4]. The circuit area is first partitioned into several sections. The self inductance and the mutual inductance are extracted for the parallel wire segments in every section and then cascaded to form the inductance model for the entire area.

The second method is applicable for aligned parallel interconnect structures [5]. Instead of dividing the wires into segments before extraction, this method first extracts the partial inductance between the entire wires. Then the wires are divided into equal length sections and the inductance values are uniformly distributed to the parallel segments in each section.

Note that the 2D models obtained from the above two methods are numerically different, even though they assume the same circuit topology. We refer to the model generated by the first method as the *cascaded* model, and the model generated by the second as the *normalized* model, following the authors of [5].

For the two wire/two segment example, the *cascaded* 2D model has the following representation,

$$\begin{bmatrix} L_A & M_{AB} & 0 & 0 \\ M_{AB} & L_B & 0 & 0 \\ 0 & 0 & L_C & M_{CD} \\ 0 & 0 & M_{CD} & L_D \end{bmatrix}, \quad (1)$$

where L_A stands for the partial self inductance of segments A, M_{AB} stands for the partial coupling inductance between segment A and B.

The second method, in contrast, generates the 2x2 inductance matrix for the entire wires first:

$$\begin{bmatrix} L_A + L_C + 2M_{AC} & M_{AB} + M_{BC} + M_{AD} + M_{CD} \\ M_{AB} + M_{BC} + M_{AD} + M_{CD} & L_B + L_D + 2M_{BD} \end{bmatrix} \quad (2)$$

Suppose the two stages of segments have equal length, splitting (2) renders the *normalized* 2D model.

$$\begin{bmatrix} L_A + M_{AC} & M_{AB} + M_{BC} & 0 & 0 \\ M_{AB} + M_{BC} & L_A + M_{AC} & 0 & 0 \\ 0 & 0 & L_A + M_{AC} & M_{AB} + M_{BC} \\ 0 & 0 & M_{AB} + M_{BC} & L_A + M_{AC} \end{bmatrix} \quad (3)$$

Note that the forward coupling terms, e.g., M_{AC}, M_{BC}, are not discarded. Instead, they are components of the 2D self and parallel terms ("folded" into these terms).

An important advantage of the 2D models as a sparsification to the original full 3D model is the *guaranteed stability* of these models. Note that the representations of both the cascaded models and the normalized models are block diagonal matrices. Furthermore, all the blocks are positive definite because they are the full matrix representations for real systems. For the cascaded model, each block is a full inductance matrix of the corresponding section. For the normalized case, every block is the scaled version of the full matrix for the unpartitioned system. Therefore, the block diagonal matrix for the 2D models is always positive definite.

Given the obvious benefits of using 2D inductance models, the primary consideration is the accuracy of these models. Critical to this problem is the magnitude of the forward coupling inductance.

4. Analysis of Forward Coupling Inductance

4.1 Basic Formulas for Partial Inductance

Although 3D field solver based extraction programs are generally required to compute the inductance model of arbitrary shaped objects, accurate analytical formulas are available for interconnects of regular shape [1][2]. In this section we explore the significance of forward coupling inductance using the following formulas.

- The mutual partial inductance between two parallel conductors with constant cross section (including the self partial inductance, which can be viewed as the mutual inductance between a conductor and its self),

$$M(l, d) = \frac{\mu}{2\pi} l\left(ln\left(\frac{2l}{R}\right) - 1 + \frac{d}{l}\right) \quad (4)$$

  where d is arithmetic mean distance between the two conductors and R is the geometric mean distance between them.

The above expression is the expansion form of the exact formula. It is accurate when d/l is small [1]. It is not limited to the conductors with rectangular cross section, nor does it require the two conductors to have identical cross section. Thus our discussion will be valid to a wide range of interconnects including wires of different aspect ratios. Two specialized forms of (4) are also used later in this paper.

- The self partial inductance of a rectangular bar

$$L(l) = \frac{\mu}{2\pi} l\left(ln\left(\frac{2l}{B+C}\right) + \frac{1}{2} - ln(\varepsilon)\right) \quad (5)$$

where B and C are the thickness and width of the wires respectively, and ln(ε) is a small positive constant depending solely on the ratio B/C, ln(ε) < 0.0025.

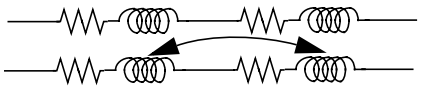
- The mutual partial inductance between two parallel equal rectangular bar

$$M(l, d) = \frac{\mu}{2\pi} l\left(ln\left(\frac{2l}{d}\right) - ln(k) - 1 + \frac{d}{l}\right) \quad (6)$$

where d is the pitch between the traces and $ln(k)$ is another constant determined by the cross section of the conductors and d. The value of $ln(k)$ and $ln(\varepsilon)$ can be obtained from lookup tables in [1].

4.2 Partial Forward Coupling Inductance

The forward self coupling inductance between two adjacent segments of length l_1, l_2 on the same straight line is illustrated as:



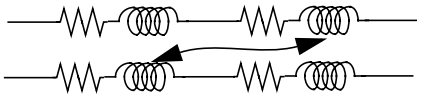
Since the total partial self inductance can be written as the sum of the self terms for each segments and the coupling terms between them,

$$L(l_1 + l_2) = L(l_1) + L(l_2) + 2M_f(l_1, l_2) \quad (7)$$

the coupling term can be computed by solving (7) for M_f and replacing the self terms by (5):

$$M_f(l_1, l_2) = \frac{\mu}{4\pi}\left(l_1 ln\left(\frac{l_1 + l_2}{l_1}\right) + l_2 ln\left(\frac{l_1 + l_2}{l_2}\right)\right) \quad (8)$$

The second type of the partial forward coupling inductance exists between two segments of length l_1, l_2 located on two parallel wires with distance d, but adjacent in the length direction:



This term can be computed similarly by decomposing the mutual inductance between the two equal parallel segments of length l_1+l_2 into parallel coupling terms and forward coupling terms.

$$M(l_1 + l_2, d) = M(l_1, d) + M(l_2, d) + 2M_f(l_1, l_2, d). \quad (9)$$

Again, the forward coupling term can be solved from (9) using the formula for mutual inductance between parallel wires (6). We have,

$$M_f(l_1, l_2, d) = \frac{\mu}{4\pi}\left(l_1 ln\left(\frac{l_1 + l_2}{l_1}\right) + l_2 ln\left(\frac{l_1 + l_2}{l_2}\right) - d\right). \quad (10)$$

To assess the relative significance of forward coupling, we compare the forward coupling terms (8) and (10) to the self inductance (5) and the parallel coupling inductance (6) respectively. For simplicity, we assume the two segments of concern are of equal lengths. The ratio of the forward coupling self term (8) to the partial self term (5) is

$$\frac{M_f}{L} = \frac{ln(2)}{ln\left(\frac{2l}{B+C}\right) + \frac{1}{2} - ln(\varepsilon)}, \quad (11)$$

while the ratio of the forward coupling mutual term (10) to the parallel mutual term (6) has a similar form.

$$\frac{M_f}{M_p} = \frac{ln(2) - \frac{d}{2l}}{ln\left(\frac{2l}{d}\right) - ln(k) - 1 + \frac{d}{l}} \quad (12)$$

There are two obvious characteristics of (11) and (12). First, for the region when the long line assumptions of $l \gg d$ and $l \gg B + C$ are valid, both ratios are always smaller than 1. Secondly, the ratios asymptotically decrease to zero as the segment length increases. Most importantly, we have the following observation:

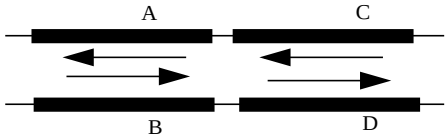
Observation 1: *Due to the logarithmic denominators of (11) and (12), the forward coupling partial inductance are* ***NOT*** *negligible.*

For example, assuming an 1μm by 1μm cross section, 2μm pitch and 1000μ*m* segment length, the above ratios are 9.4% and 11.7% respectively.

Since usually long wires contain more than two segments, each self and parallel coupling inductance should be compared with the total effect of several forward coupling terms to the up-stream and down-stream segments. The total forward coupling inductance is even larger than the numbers shown above. Clearly, the forward coupling inductance terms are not negligible numerically, though it is favorable to do so in terms of efficiency.

4.3 Loop Inductance

Inductance is ultimately a property of the current loops. In this section, we study the mutual inductance between loops using a simple model. In this model, the current loop consists of only two parallel wire segments with one delivering current and the other returning current.



First we consider the case using the two wire/two segment example. Segment A and segment B form a current loop, while segment C and segment D form the other loop as shown above. Assume the wire distance, d, is much smaller than the length of the segments l_1, l_2.

Note that each of the small current loops consists of two identical currents flowing closely in the opposite directions. Such a current pair resembles the behavior of a ***dipole***. The induced electrical field generated by the current variation on one segment due to Faraday's Law counteracts the field generated by the other. The resulting induced field drops much faster with distance than that of a monopole (each segment current alone). Consequently, we should expect the couplings between the loops to be much weaker than the coupling between the partial elements.

The forward coupling between the two loops (dipoles), also shows the cancellation effect in its expression (13).

$$M_{loop}(l_1, l_2) = (M_{AC} - M_{BC}) + (M_{BD} - M_{AD}) \quad (13)$$

For the typical case where the segment lengths of A, B, C, D are much larger than the distance of the ideal return path d, we can apply the formulas (8)(10) derived in the previous section to the partial terms in (13). It results in the following astonishing expression:

$$M_{loop}(l_1, l_2) = \frac{\mu}{2\pi} d \quad (14)$$

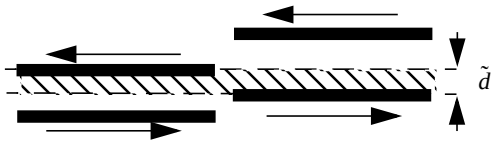
The above formula shows that the (dipole) forward coupling between the loops is (approximately) a small constant when the segment lengths are long enough. In other words, the forward coupling inductance between the loops is well approximated by a constant which only depends on the distance of the current return; when the segment lengths increase, the forward coupling inductance approaches this constant as the limit value.

For comparison, we compute the self inductance for a loop, e.g., the loop formed by segment A and B,

$$L_{loop}(l_1) = L_A + L_B - 2M_{AB} \quad . \quad (15)$$
$$= \frac{\mu}{\pi} l_1 \left(ln\left(\frac{d}{B+C}\right) + \frac{3}{2} - ln(\varepsilon) + ln(k) \right) - \frac{\mu}{\pi} d$$

Note that the loop self inductance grows linearly with the wire length. When $l \gg d$, the loop forward coupling inductance becomes negligible compared with the loop self inductance. Assume that each trace has an 1µm by 1µm cross section and the pitch between the traces is 2µm. The ratio of (14) to (15) is 0.68% when the loop length is 100um and it decreases to 0.067% when the loop length is 1000um.

More generally, in the case when the two loops are not exactly aligned in the current direction as shown below, the forward coupling between the loops is given by $\frac{\mu}{2\pi}\tilde{d}$, where $\tilde{d}$ is the overlap of the two loops in *Y* direction. When $\tilde{d}$ is zero, the forward coupling is so small that a more accurate high-order formula has to be used in place of (4) to observe it.



We can also derive the loop parallel coupling inductance in a similar fashion. For example, the coupling inductance between the loop formed by A and B and the loop formed by C and D in the figure below, is given by (16).

$$M_{loop}(l_1) = \frac{\mu}{2\pi} l_1 ln\left(\frac{R_{AD}R_{BC}}{R_{AC}R_{BD}}\right) \quad (16)$$

R_{AD}, R_{BC}, R_{AC}, R_{BD} are the geometric mean distance between the traces A, B, C, D respectively. The loop parallel coupling inductance between loops is a linear function of the wire (loop) length.

Therefore, we make the following observations.

Observation 2: *For the current loops defined above, the loop forward coupling inductance is a negligible constant* $\frac{\mu}{2\pi}\tilde{d}$.

Observation 3: *For the current loops defined above, the loop self inductance and the parallel coupling inductance between the loops are linear functions of the wire length, therefore the unit length inductance can be defined as the linear coefficients in equation (15)(16).*

Note that for partial inductance, the unit length inductance concept is invalid because the partial inductance grows superlinearly with the segment length as shown by the formulas in the previous section.

In summary, since the forward coupling terms between the loops are negligible, it doesn't matter whether they are discarded or approximated. Both 2D models will work fine in this case.

5. Impact of Current

In this section, we take a closer look at the expected on-chip current return paths and analyze the impact of the current distribution on the induced voltage due to forward coupling. Generally, for on-chip interconnects, there is no *dc* path for the current to return. The current delivered by the signal lines has to return via *ac* paths. The *ac* return paths are comprised of coupling capacitors among the parallel lines and even the cross–over metal strips in the neighboring layers.

Normally, a fully extracted RLC circuit contains two types of capacitors, coupling capacitors and grounding capacitors. The differences in the formulation of the capacitances can play an important role in the accuracy of the two–dimensional model.

Consider the current flowing to the common ground via the grounding capacitors. It virtually returns from the infinity and behaves like a monopole. On the other hand, the current can also return via the *ac* path formed by the lateral coupling capacitance and the neighboring wires or low resistive shields, and behaves like a dipole.

The reality is a mix of these two situations. Below we discuss the composite effect of the different current returns paths based on the coplanar bus structure in Fig. 1.

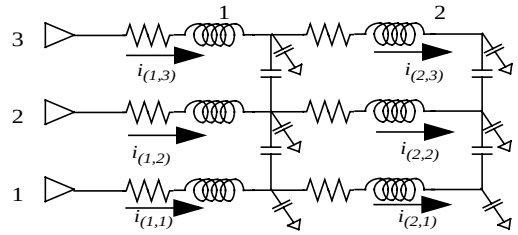


Fig. 1: A circuit model of coplanar busses

Assume that the circuit contains *N* wires and *M* segments. Denote the current flowing over the segment at the m^{th} column and the n^{th} row, *(m, n)* in Fig. 1, by $i_{(m.n)}$. This term can be decomposed into two parts,

$$i_{(m,n)} = i_{int(m,n)} + i_{ext(m,n)} \quad (17)$$

where $i_{int(m,n)}$ is the part of the current injected into *(m,n)* that returns from its parallel peers, while $i_{ext(m,n)}$ is the current returning via the ground capacitance paths.

It follows that the total induced voltage on a segment *(j,k)* by the current in stage *m*, $V_{(j,k),m}$ can be considered as the sum of the induced voltage by these two types of current.

$$V_{(j,k),m} = \quad (18)$$
$$\sum_{n=1}^{N} M_{(j,k)(m,n)} \frac{di_{int(m,n)}}{dt} + \sum_{n=1}^{N} M_{(j,k)(m,n)} \frac{di_{ext(m,n)}}{dt}$$

We compare the voltage induced by the forward coupling from its adjacent segments with the voltage induced by the self and parallel coupling inductance on this segment based on the above decomposition. Applying the general formula in terms of geometric mean distance(4), we obtain the induced voltage due to the *self and parallel coupling* inductance as follows

$$VP_{(j,k)} = VPI_{(j,k)} + VPE_{(j,k)} \tag{19}$$

$$VPI_{(j,k)} = \frac{\mu}{2\pi}\sum_{n=1}^{N}\left((-l_j ln(R_{k,n}) + d_{k,n})\frac{di_{int(j,n)}}{dt}\right) \tag{20}$$

$$VPE_{(j,k)} = \frac{\mu}{2\pi}\sum_{n=1}^{N}\left(l_j\left(ln\left(\frac{2l_j}{R_{j,n}}\right)-1+\frac{d_{k,n}}{l_j}\right)\frac{di_{ext(j,n)}}{dt}\right) \tag{21}$$

where $VPE_{(j,k)}$ and $VPI_{(j,k)}$ are the voltage responses due to parallel couplings generated by either ground capacitance (***E***xternal) current or coplanar capacitive coupling (***I***nternal) current. The above expressions are after simplification based on the Kirchoff's Current Law (KCL).

The voltage induced by the *forward coupling* inductance from the adjacent stage $m=j+1$, has the form

$$VF_{(j,k)} = VFI_{(j,k)} + VFE_{(j,k)} \tag{22}$$

$$VFI_{(j,k)} = \frac{\mu}{4\pi}\sum_{n=1}^{N}\left(-d_{k,n}\frac{di_{int(m,n)}}{dt}\right) \tag{23}$$

$$VFE_{(j,k)} = \tag{24}$$

$$\sum_{n=1}^{N}\left(\frac{\mu}{4\pi}\left(l_j ln\left(\frac{l_j+l_m}{l_j}\right)+l_m ln\left(\frac{l_j+l_m}{l_m}\right)\right)\frac{di_{ext(m,n)}}{dt}\right)$$

Comparing (20) and (21) with (23) and (24), we have the following observations.

Observation 4: *If the return current via the grounding capacitance is* negligible*, the induced voltage due to forward coupling (23) has a much smaller inductance coefficient than that due to the self and parallel inductance (20). Forward coupling inductance is comparatively negligible. The error of using 2D inductance models is small.*

Observation 5: *If the return current via the grounding capacitance is* significant*, the forward coupling impact (24) is* not *negligible compared with the self and parallel inductance impact (20) and (21). In this case, discarding the forward coupling inductance, as done in the cascaded model, will introduce error.*

Note that the return path is not the only influence on the inductance effect. The actual waveform of the current and its propagation in the wires also have an impact.

Consider the special case when the normalized model is applicable, the system consists of equal length parallel wires. For signals with large risetime and small propagation delay, due to the continuity of the current distribution along the line, at any given time the neighboring segments on the line have the same current flow approximately, i.e., $i_{(j,n)} \approx i_{(m,n)}$. The currents in the equations (23) and (24) can be approximated by the currents in the j^{th} segments themselves. Thus the induced voltage due to the forward coupling inductance can be viewed as if the forward coupling inductance terms are "folded" into the self and parallel inductance. When the assumption on the current is true, the normalized model will be a good approximation to the original 3D model regardless of the current distribution in the return paths.

6. Experiments on RLC Interconnects

The overall impact of the forward coupling inductance should be considered in the combined RLC system. Since the lumped RLC circuit is an approximation of the original distributed multiconductor system, the total error of the 2D based RLC circuit can be viewed as the composite effect of two components, the error between the original distributed system and the finite 3D PEEC model, and the error between the 3D circuit model and the 2D based models. Both errors vary with the degree of discretization, e.g., the number of the segments used to represent each conductor or the size of the segments. In this section, We compare the response characteristics of the RLC circuits based on the 2D inductance models with the same system based on the 3D model, when the degree of discretization is varying.

A 5-bit bus with one shield at each side is used as an example in this experiment. The wiring material is copper. The wires are 1μm thick and 3000μm long. The width of the signal wires is 0.5μm while the width of the shields is 1μm. The space between the neighboring wires is 0.5μm. Each signal wire is driven by a 100Ω resistor and loaded by a capacitance of 40ff. The two shields on the sides are grounded at the near end. The bus is extracted using field solver based extraction tools. The signal delay obtained via HSpice simulation of the 2D and 3D models under a 50ps finite ramp input is shown against the number of segments used to represent each conductor.

First, we force the current to return via the coupling capacitance and the in-plane return paths by zeroing the grounding capacitors. In Fig. 2a, we find the delay curves given by the 2D models fit consistently well with the delay curve obtained from the full 3D model, as expected in the previous section.

In the second experiment, the grounding capacitors are included in the simulation. Since the current is no longer limited to return within the bus, the curve from the cascaded model starts to deviate from that of the 3D model (Fig. 2b). The discrepancy increases with the number of segments (when the segment length decreases). In this case, the normalized model is still able to provide a fair approximation to the 3D model.

To further investigate the efficacy of the normalized model, we repeat the second experiment with the input signal risetime set to 10ps. On the contrary to the assumption in the previous section, the response signal has a sharp rising edge but a larger LC propagation delay. The results are shown in Fig. 3. We find that the normalized model tends to produce overestimated delay values. However, even in this case, the relative error of the normalized model is still less than 5%.

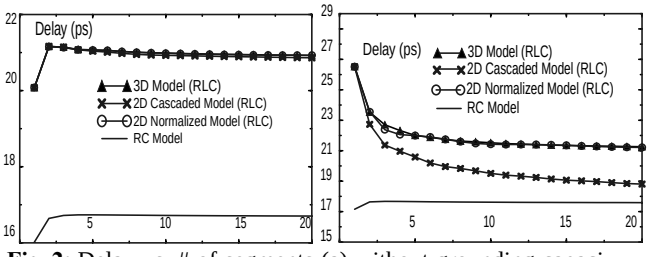


Fig. 2: Delay vs. # of segments (a) without grounding capacitors (b) with grounding capacitors

Fig. 4 shows the total extraction and simulation runtime for the full 3D model and one of the 2D model (the normalized model). Obviously, the latter is much more efficient.

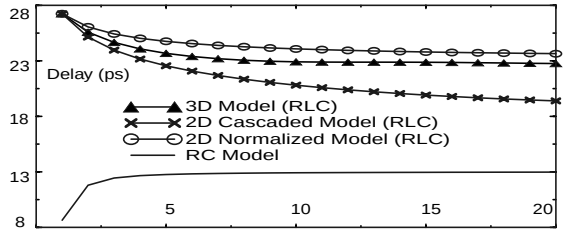


Fig. 3: Delay vs. number of segments (fast input signal)

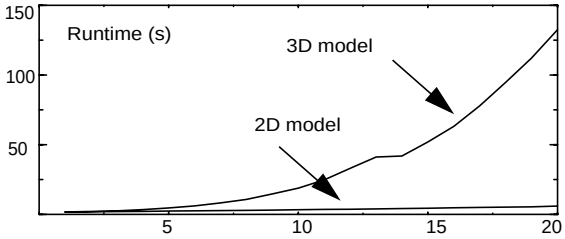


Fig. 4: Runtime vs. number of segments.

7. A Combined Methodology

Although the normalized 2D model has good consistency with the 3D model for a wide range of discretization, it is only applicable to aligned parallel wires with equal length. The cascaded model is more general and suitable for arbitrary interconnect topologies. However, from the experimental results, we observe that the cascaded 2D model could introduce significant error when the return current is not limited to close-by return paths. To solve this dilemma, we propose a general 2D inductance modeling methodology that combines the advantage of the cascaded model and the normalized model. Furthermore, it can be incorporated with other screening and sparsification techniques([16][17]) to reduce the number of parallel coupling terms.

We suggest the following methodology of RLC modeling for large on-chip interconnect systems:

1. Proceed along the X direction, divide the circuit area into sections so that all of the horizontal wires within each section span the width of the section.
2. The inductance of the equal length wires in each section is extracted using a field solver or a table-lookup based extractor.
3. Build a normalized model for each section based on the inductance matrix for the entire section.
4. Cascade the normalized models to form the 2D inductance model of the horizontal wires in the target area.
5. Repeat the above process in Y direction. Combine the results to form the complete inductance model.

It is important to note that in addition to the improvement of the modeling method, design techniques invented to reduce the inductance effect can also enhance the accuracy of the 2D models. For critical and inductance sensitive circuits, e.g. busses and clock trees, extensive shield insertion is often recommended in practice. Since the current tends to flow via the path with the lowest impedance, it will return from a close-by path when the frequency is high, thus making the forward coupling inductance as well as the effective loop inductance minimized. In other words, for well designed circuits, the on-chip interconnect structure is often of a form that can be analyzed via 2D models.

8. Conclusion

The significance of forward coupling inductance in on-chip interconnect models has been studied in detail. The impact of sparsifying the inductance matrix by truncating the forward coupling inductance was analyzed analytically and through numerical examples.

As expected, the impact of the forward coupling inductance heavily depends on the actual current distribution. The 2D inductance models are applicable whenever the return current can be restricted to local return paths. For aligned coplanar structure, the normalized model provides better accuracy then the cascaded model. The two types of 2D inductance models can be combined to provide more accurate and efficient approximations for full 3D inductance models.

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