Optimal Design of Delta-Sigma ADCs by Design Space Exploration

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ABSTRACT

An algorithm for architecture-level exploration of $\Delta\Sigma$ ADC design space is presented. The algorithm finds an optimal solution by exhaustively exploring both single-loop and cascaded architectures, with single-bit or multi-bit quantizer, for a range of oversampling ratios. A fast filter-level step evaluates the performance of all loop-filter topologies and passes the accepted solutions to the architecture-level optimization step which maps the filters on feasible architectures and evaluates their performance. The power consumption of each accepted architecture is estimated and the best top-ten solutions in terms of the ratio of peak SNDR versus power consumption are further optimized for yield. Experimental results for two different design targets are presented. They show that previously published solutions are among the best architectures for a given target but that better solutions can be designed.

Categories and Subject Descriptors

J.6 [**Computer Applications**]: Computer-Aided Engineering

General Terms

Design

Keywords

ADC, CAD, delta-sigma

1. INTRODUCTION

Among the many architectures of analog-to-digital converters (ADC), $\Delta\Sigma$ designs are used in a large class of applications ranging from low-frequency [1] and audio [2] to down-converted intermediate frequency [3] and digital video [4]. Their property to trade speed for accuracy makes them more attractive in the context of present CMOS technology evolution [5]. The spread of $\Delta\Sigma$ designs and the absence of an accurate analytical model for their non-linear behavior caused a rapid evolution of dedicated simulation software. There are a number of simulators readily available, some of them as free software toolboxes [6] and some developed in universities [7], [8]. However, even using fast, dedicated simulators, it is all but impossible for a designer to explore the entire range topology and design parameters that can yield the optimal solution for a target dynamic range (DR) or peak signal-to-noise+distortion ratio (SNDR).

This paper presents a global optimization approach which outputs a list of the best $\Delta\Sigma$ ADC architectures in terms of peak SNDR versus power consumption ratio. The optimality is guaranteed by thorough search of the entire design space, as opposed to other design automation software which only allow a user-specified architecture to be designed [8] or a set of user-designed architectures to be browsed in search for a set optimum [7], which compared to the entire design space is a local optimum.

The search is conducted in two steps. In a first step, the filter-level design, the loop filter(s) are analyzed using the linear model approximation [9] for all possible combinations of loop order, number of cascaded loops, number of bits in the quantizer, oversampling ratio and peak gain of the noise transfer function (NTF). The DR of each solution is evaluated [6] and qualifying solutions are delivered to the next step.

The second step, the architecture-level design, maps the filter-level qualified solutions on all possible system architectures. Each architecture is designed and its performance in terms of integral non-linearity (INL) [9], DR intercept, and conversion gain is analyzed from time-domain simulations. Accepted solutions are then subjected to power consumption estimation, based on the assumption of switched-capacitor (SC) differential circuit design using single-stage operational amplifiers [10], [2]. A reduced set of solutions is selected based on the peak SNDR versus power consumption ratio. Only this reduced set of solutions is subjected to Monte-Carlo analysis to optimize their yield performance with respect to process-induced mismatch of architecture coefficients.

The paper is organized as follows. Section 2 contains a description of the filter-level design step. Section 3 presents the architecture-design step with details on the performance tests and architecture-level power estimation. Experimental

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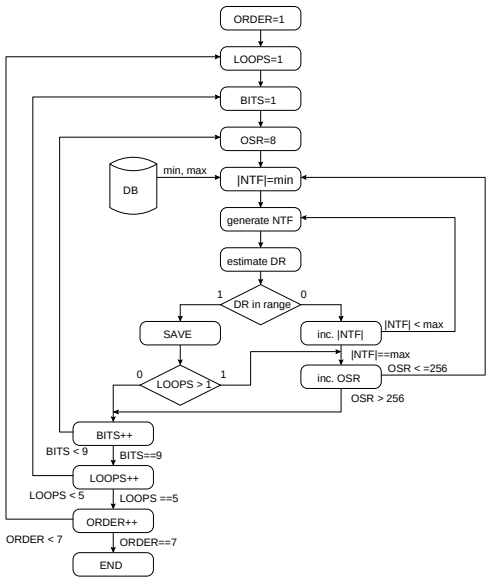

Figure 1: Design space exploration algorithm for filter level (linear model)

results are shown in Section 4 for two different targets, an audio and an xDSL $\Delta\Sigma$ ADC. The conclusions are presented in Section 5.

2. FILTER-LEVEL DESIGN

2.1 Exploration Algorithm

A fast design space exploration is performed first, using a linearized model of the $\Delta\Sigma$ ADC. The search algorithm is shown in Fig. 1. A separation is made between the *topology* design space defined by the *ORDER*, number of *LOOPS* and number of *BITS*, and the *parameter* design space defined by the oversampling ratio *OSR* and peak *NTF* magnitude. All these dimensions of the search space are browsed using constant stepping, linearly in *topology* space and exponentially in *parameter* space.

At each step a set of two filter transfer functions are generated, the NTF and the signal transfer function (STF). As a provision for direct sensor interfacing, it is possible to set the STF gain to values different from unity. Filter generation can also optimize in-band zeros for the NTF (to reduce total in-band noise power [6]) and off-band zeros for the STF (to reduce in-band gain ripple and increase off-band rejection). After the two filter transfer functions are generated the in-band noise power is calculated to estimate the DR. A test is applied with two thresholds derived from the target DR (in dB)

$$DR_{target} + DR_{lower} \leq DR \leq DR_{target} + DR_{upper} \quad (1)$$

The lower limit tests if, after the circuit (white) noise is added, the converter still reaches the target DR. The upper limit is set to reject power-hungry solutions which offer more quantization-noise DR than actually needed. If the test is passed, the solution is saved in a database.

For the single-loop solutions the algorithm stops when a combination of minimal *OSR* and *NTF* is found. For cascaded designs, however, because significant architectural details are not available at the filter level, the algorithm continues searching for solutions even after finding the first valid one. This insures that no valid solution is prematurely rejected.

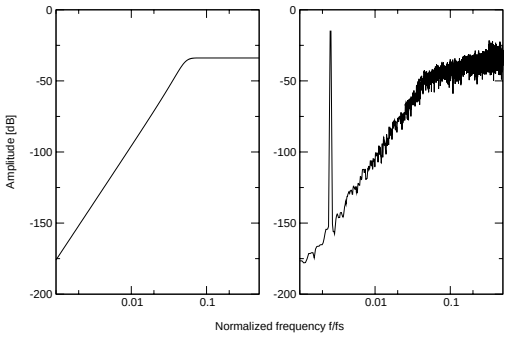

Figure 2: Estimated (*left*) and time-domain simulated (*right*) quantization noise spectrum for ORDER=4, BITS=1, LOOPS=1

2.2 Dynamic Range Evaluation

A fast yet accurate method to estimate the DR is used. It overcomes the drawbacks of both time-domain simulations, which are slow, and classical DR estimation using a formula which is inaccurate especially for high-order $\Delta\Sigma$ loops:

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} OSR^{2L+1}(2^B - 1)^2 \quad (2)$$

First the magnitude of NTF is calculated in n points equally distributed from DC to $f_s/2$

$$|NTF(Z)|_i = \left| \frac{\Sigma_{j=1}^{L} d_j Z^{-j}}{\Sigma_{k=1}^{L} n_k Z^{-k}} \right|, i = 1 \cdots n \quad (3)$$

using

$$Z^{-k}|_i = cos(k\pi i/n) - Jsin(k\pi i/n) \quad (4)$$

The total power of quantization noise is assumed to be [9]

$$P_{qn} = \frac{\Delta^2}{12} \quad (5)$$

which yields a (white) quantization noise amplitude in each bin i from DC to $f_s/2$, referred to $V_{ref} = \Delta(2^{B-1})/2$, as

$$S_{qn,Bbit} = 20log_{10}\left(\sqrt{\frac{2}{3n}}\right) - 20(B-1)log_{10}(2) \quad (6)$$

if the quantizer has B bits.

The value of the NTF magnitude, given by Eq. (3) expressed in dB, is added to the value of $S_{qn,Bbit}$ and a curve showing the quantization noise amplitude in each bin is drawn. Its integral in the band of interest yields the estimated DR value. Fig. 2 shows the estimated (*left*) and time-domain simulated (*right*) spectrum of the output of a fourth-order, one-bit, single-loop $\Delta\Sigma$ ADC. The two graphs show the good accuracy of this estimation method for high-order loops.

The DR of the fourth-order, single-loop, single-bit $\Delta\Sigma$ ADC operated at 64 times OSR is estimated to be 102dB,

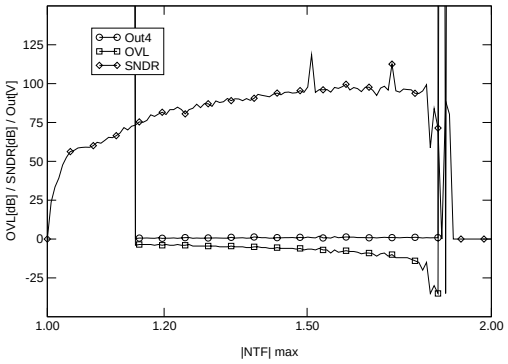

Figure 3: Peak NTF magnitude database entry example (ORDER=4, BITS=1, $V_{clip}/V_{Ref} = 1$)

which is only 3dB different from the time-domain simulated result of 105dB. As a comparison, the formula in Eq. (2) yields 134dB, due to the idealized NTF expression used to derive it [9]. The evaluation is fast, finding all 200-plus possible solutions which can yield 100dB DR in approximately 10 minutes on a 1GHz computer.

2.3 Peak NTF Magnitude Database

The one parameter of $\Delta\Sigma$ ADCs which cannot be predicted accurately by linear modeling is the overloading level (OVL) [9]. In the algorithm presented here, the overloading levels for each single-loop $\Delta\Sigma$ ADC in the entire range of loop orders and quantizer bits are computed once from time-domain simulations and stored in a database. The peak magnitude of NTF is varied in a range from 1.0 (0dB) to 16.0 (24dB). Each single-loop $\Delta\Sigma$ ADC is designed and optimized in a range of input signal values for each NTF peak magnitude. The overloading level is detected as the input signal which causes integrator clipping.

Fig. 3 shows the entry in the peak NTF database for the single-bit, fourth-order $\Delta\Sigma$ ADC. It shows the variation of overloading level *OVL*, peak output of the last integrator *Out4* and the peak *SNDR* in the NTF range where the loop can be stabilized.

Because there is a tight relationship between the *OVL* value and the ratio of the clipping voltage over reference voltage, the database has to be generated for each different ratio of V_{clip}/V_{Ref}. This takes about 24 hours on a 1GHz computer but the same database can be used for any target DR (SNDR) design as long as the V_{clip}/V_{Ref} ratio does not change.

3. ARCHITECTURE-LEVEL DESIGN

3.1 Exploration Algorithm

The architecture-level exploration algorithm evaluates the performance of the filter-level solutions mapped on a specific architecture, as shown in Fig. 4. If a single-loop solution is processed, an architecture is generated (the feedforward and feedback connectivity can be specified by the user) and its coefficients are calculated. A wide range of input signal amplitudes is then used to detect the overloading level. The input signal applied at this stage is a pulse (a busy signal [9]) with a fundamental frequency three times lower than the signal bandwidth.

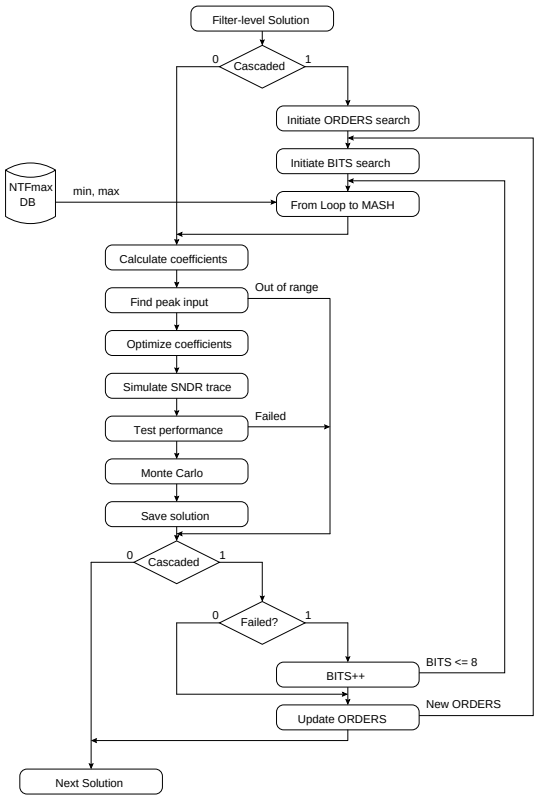

Figure 4: Design space exploration algorithm for architecture level

The next step is the coefficient optimization, which is performed at the OVL previously detected. The SNDR and DR variations as a function of the input signal are then simulated. The two curves are tested for performance and passing solutions are subject to a Monte-Carlo (MC) analysis to test the architecture's tolerance to coefficient mismatch. The solution is then saved for further processing.

For the cascaded $\Delta\Sigma$ ADCs the only architectural details predefined at filter level are the number of loops and the number of bits in the last loop. Therefore, the filter orders of individual cascaded loops are generated as one additional design space dimension named *ORDERS* in Fig. 4. Another new design space dimension is the number of *BITS* in the first loop of the cascade. For simplicity, the last $n-1$ loops in a cascade of n loops have the same number of bits as the last one. Each derivative of the input solution in the extended design space is analyzed as an independent solution.

3.2 Performance Test

Performance testing is based on statistics of SNDR and DR curves as functions of input signal level. Linear regressions are performed on each curve, from SNDR zero-crossing to the overloading level. The slope of SNDR is tested to be within 10% of the desired conversion gain (typically unity). A slope outside this range shows a strong dependency of quantization noise power of the input signal level, which is not desired. The mean of the DR curve is then tested against the target DR value to insure the target DR is attained. Finally, the peak regression residual of the DR curve is tested

to be lower than 6dB (1 bit) to insure the required integral non-linearity (INL). Finally, the overloading level is tested to be larger than -15dB.

$SNDR(V_{in})$ and $DR(V_{in})$ curves for an architecture rejected by the performance test algorithm are shown in Fig. 5. The dotted lines are the linear regression fitted values for both simulated curves. The drop in DR at high input levels (larger than -20dB) shows that the peak NTF value needed to reach the target DR is too high so premature clipping occurs [6]. The peak SNDR which still keeps a good overall INL is about 85dB instead of almost 95dB, as shown by its absolute peak value. But the detection of this effect requires a set of linear regressions with each point in the curve used as higher limit, which would increase the computation time tenfold. Instead, because the decrease in peak SNDR already disqualifies this solution, the simple yet effective criterion of peak regression residual limiting is used as rejection reason. The slope of DR fitted line shows that the test for SNDR slope also works towards rejecting the solution, even if the curves would pass the DR mean value test.

3.3 Power Estimation

The power of each solution accepted by the performance tests explained in the previous sub-section is evaluated considering a switched-capacitor design approach. Fully differential circuits are considered, with independent paths for input and DAC signal integration, as shown in Fig. 6. The charge in the sampling capacitor C_s and in the feedback capacitor C_{fb} are both integrated on the integration capacitor C_i during half or the clock cycle (integration phase).

The power consumption of such an integrator can be expressed as a function of the amplifier's input stage transconductance g_m, which is designed considering the settling requirements for specific linearity performance [2], [10]. The capacitive load driven by g_m is derived from noise performance of each integrator. Considering a one-stage amplifier, the total noise power at the input of the integrator is

$$P_n = 4KT\left(\frac{1}{C_s}\left(1+\frac{C_{fb}}{C_s}\right)+\frac{1}{3\pi C_{load}}\right) \tag{7}$$

with

$$C_{load} = C_s + C_{fb} + C_l + \frac{C_l(C_s+C_{fb})}{C_i} \tag{8}$$

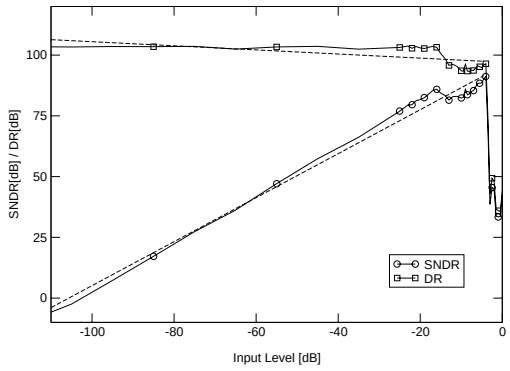

Figure 5: Example of SNDR and DR curves for a rejected architecture (ORDER = 3, OSR = 32, BITS = 2, LOOPS = 3 [1,1,1], 2 bits in the first loop)

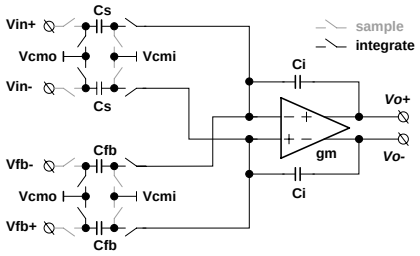

Figure 6: Schematic of a typical switched-capacitor integrator

where C_l is a fraction of the integration capacitor (parasitic capacitance of C_i) connected at the opamp's output. The first part of the noise power in Eq. (7) is the noise of the switch on-resistance and the second part is the noise of the g_m in the opamp. This power is referred at the input of the $\Delta\Sigma$ converter as

$$P_i = \left(P_n \frac{1}{\Pi_{j=1}^{i-1}\left(\frac{C_{sj}}{C_{ij}}\right)} \frac{\pi^{2(i-1)}}{(2i-1)OSR^{2i-1}}\right)_i \tag{9}$$

with i the order of the integrator in the $\Delta\Sigma$ converter.

All the capacitors are calculated from the required noise power of each integrator. The g_m is then calculated from the required settling performance, considering a slewing followed by settling model [2]

$$g_m = \frac{C_{load}\,(N_\tau - 1)}{\frac{T_{CK}}{2} - V_{fb}\frac{C_{load}}{I_0}} \tag{10}$$

The feedback voltage at the input of the opamp after the charge re-distribution phase [2], V_{fb}, can be calculated in the worst-case as

$$V_{fb} = V_{out,max}\left(1+\frac{C_l}{C_i}\right)\frac{C_s+C_{fb}}{C_{load}} \tag{11}$$

The number of needed time constants, N_τ in Eq. (10), is given by the settling required to reach B bits of linearity [10] as $N_\tau = Bln(2)$. The required linearity of an integrator is determined by allocating equal distortion power to each integrator and considering the loop gains to input-refer individual distortion powers, with the sum of the distortion powers set to 3dB (0.5 bit) below the target DR.

Considering MOS transistors operated in weak inversion are used in the input stage of the opamp, $g_m = 10I_0$ and a compact expression for g_m is obtained

$$g_m = \frac{2}{T_{CK}} C_{load}\left((N_\tau - 1) + 10V_{out,max}\left(1+\frac{C_l}{C_i}\right)\right) \tag{12}$$

The noise power of each integrator is allocated based on exploration of noise power distribution across the converter. A part of the noise power of the previous integrator is allocated to the next in the loop

$$(P_n)_i = R\,(P_n)_{i-1} \tag{13}$$

and the value of R is chosen to minimize total power consumption. Fig. 7 illustrates the dependence of power consumption of noise power allocation through the ratio R. The top curve is the power (expressed as the supply current) consumed for the total g_m for a fifth-order, 3-loop, 2-2-1 architecture, with 5 bits in the first loop and 3 bits in the

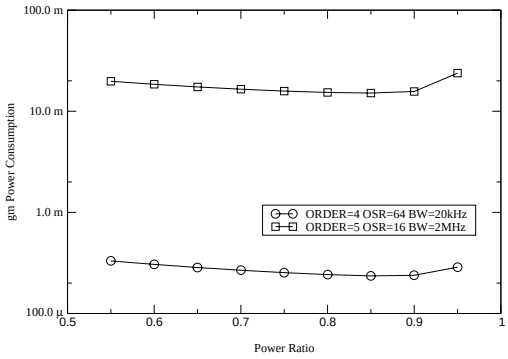

Figure 7: Power consumption for g_m as function of noise power ratio R

other two loops. It is operated at 16 times OSR for a signal bandwidth BW of 2MHz, as in [4]. It is worth noting the 25% reduction in current consumption by optimization of R and the fact that the minimum current, of 14mA, is well related to the reported consumption of 36mA if folded cascode amplifiers are used [2]. The second curve in Fig. 7 is the current consumption for a fourth-order, one-bit single-loop $\Delta\Sigma$ ADC for audio applications (BW=20kHz). The supply current estimated in the best case also matches the design reported in [2].

3.4 Yield-Based Optimization

The accepted solutions are passed to the MC analysis which varies the $\Delta\Sigma$ ADC coefficients using a user-supplied distribution. The user can specify, for each integrator, a spread 3σ value along with the coefficient-to-coefficient mismatch 3σ value. A required minimal capacitor is specified for the latter 3σ value. A few hundreds of Monte-Carlo simulation steps are run for the top-ten solutions and the performance tests explained in Subsection 3.3 are applied. The single-loop solutions can be designed from the early stages to give 100% yield with relaxed matching requirements. However, for cascaded solutions which do not attain an yield larger than 90%, the number of bits in the first loop in the cascade is increased and another Monte-Carlo yield analysis iteration is started.

4. EXPERIMENTAL RESULTS

Two examples are presented to show the effectiveness of global optimization through exhaustive design-space exploration. The first one is an audio $\Delta\Sigma$ ADC biased at 1.5V with rail-to-rail input and 1.5V reference voltage. A designed circuit has been reported [2] which consumes 0.95mW (only the analog part, without voltage reference buffers) for a DR of 98dB and peak SNR of 89dB at a signal bandwidth of 20kHz. The second one is an ADC for xDSL applications, biased at 2.5V, also with rail-to-rail input and reference voltage equal to the supply voltage. The signal bandwidth is 2MHz. A design has been reported which consumes 90mW in the analog circuits to attain 95dB DR and 90dB peak SNR.

The designs mentioned above are state-of-the art examples. The results presented here show that other architectures can offer better peak SNDR versus supply power consumption ratios (FOM) but these designs are still among the best options. The yield optimizations have been conducted assuming a 1% (fair capacitor/capacitor matching) coefficient-to-coefficient mismatch for single-loop architectures and 0.5% (good capacitor/capacitor matching) for cascaded architectures.

Table 1: Global solutions for Audio $\Delta\Sigma$ ADC

ORDER	LOOPS	BITS	OSR	SNDR	FOM
4	2 (2-2)	2 (6)	32	97.5	119.8
4	3 (2-1-1)	2 (5)	32	97.3	119.5
5	3 (2-1-2)	1 (7)	32	98.5	120.2
5	2 (2-3)	4 (7)	32	98.5	119.8
5	2 (2-3)	5 (7)	32	98.1	119.5

Table 2: Audio ADCs with LOOPS=1

ORDER	BITS	OSR	SNDR	FOM
3	6	16	95.3	117.6
3	8	16	96.3	117.8
3	4	32	95.5	118.4
4	8	8	95.6	116.4
4	5	16	96.0	117.8
5	4	16	95.4	116.5
5	6	16	96.2	115.9

4.1 Audio Delta-Sigma ADC

The search for an optimal audio $\Delta\Sigma$ has been first performed in the entire design space, to find the global optimum. In order to compare with previously reported state-of-the-art solution, restricted sets in terms on number of loops and number of bits have been analyzed. The global optimization results are shown in Table 1. It is worth noting the massive presence of cascaded solutions. The column *LOOPS* shows each cascaded loop's order in parentheses, while the column *BITS* contains the number of bits in the first loop in parentheses. The solutions have virtually the same figure-of-merit *FOM*. All solutions have OSR=32 and a large number of bits in the first loop, which increases the FOM value by increasing the overloading level with no power costs.

Table 2 contains the optimization results for a set of solutions restricted by the number of loops (LOOPS=1). The best solution is the third order, 4-bit loop, again working at OSR=32. This solution is also remarkable by its low number of bits compared to the other top performers. This shows that, for audio frequencies, high-OSR is still a good option.

Further design space restriction to 1-bit single-loop architectures yields only the state-of-the-art fourth-order, single-loop solution with OSR=64 reported in [2]. The 1-bit DAC is often needed for its inherent linearity but it requires a larger OSR. The solution is chosen from a set of four possible, three of which do not pass the yield test.

4.2 Delta-Sigma ADC for xDSL Applications

The results of global optimization for a 4MS/s $\Delta\Sigma$ ADC are shown in Table 4.

Again a third-order solution with OSR=32 and 4-bits quantizer has good performance, but most of the solutions operate at 16 times oversampling. They also have large number of bits in the (first loop) quantizer to attain high

Table 3: Global solutions for xDSL $\Delta\Sigma$ ADC

ORDER	LOOPS	BITS	OSR	SNDR	FOM
3	1	4	32	96.5	102.7
4	2 (2-2)	4 (8)	16	97.4	103.1
4	3 (2-1-1)	4 (7)	16	98.1	102.7
5	2 (2-3)	3 (8)	16	96.6	102.1
5	2 (2-3)	4 (6)	32	97.1	101.7
6	3 (2-2-2)	2 (8)	16	97.4	102.6

overloading levels. The FOM values are 20 dB smaller than the ones obtained with the audio ADCs because of increased sampling frequency.

To avoid solutions like the ones requiring 32 times OSR, the designer can conduct the search in a limited space, for example for (ORDER=5, OSR=16). Furthermore, the number of bits can be limited, for example to 6, to keep a low DAC complexity. The solutions for this search are shown in Table 4. They are all cascaded $\Delta\Sigma$ ADCs except two which, even with their low-FOM, can be good choices for low-voltage, mismatch-tolerant designs.

The best are the three-loops with a 2-2-1 configuration. The state-of-the-art solution reported so far [4] is among them. During initial optimization stages, only 3 bits were needed in the first loop, but yield optimization reached the 5-bit solution reported in [4], the increase being needed to accommodate capacitor/capacitor mismatch effects.

An overview of all fifth-order solutions operated at 16 times OSR is given in Fig. 8. The total biasing current g_m required by each of the 21 solutions is depicted with a different symbol for different number of loops. For the same number of cascaded loops there are multiple solutions with different combinations of orders for the loops in the cascade. A 3-bit solution needs the lowest power and generally the 2-loops solutions are the best performers. There are eleven 2-loops solutions, nine 3-loops and one 4-loops.

5. CONCLUSIONS

An exhaustive design-space exploration algorithm for global optimization of $\Delta\Sigma$ ADC design has been presented. The algorithm examines all possible solutions in two steps to increase overall speed. The large total number of possible solutions is only explored by the fast filter-level design step

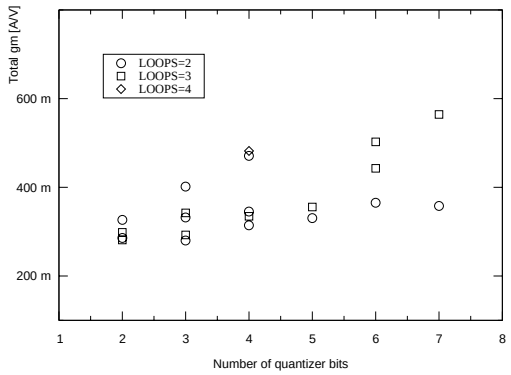

Figure 8: Total g_m for ORDER=5, OSR=16 solutions

Table 4: xDSL ADCs with ORDER=5, OSR=16

LOOPS	BITS	SNDR	FOM
2 (4-1)	2 (5)	93.1	98.0
3 (2-2-1)	2 (6)	97.1	102.6
3 (2-2-1)	3 (5)	95.7	101.0
3 (2-2-1)	4 (6)	97.8	102.5
1	5	96.6	100.4
3 (2-2-1)	5 (5)	98.1	102.6
1	6	96.5	99.6
3 (2-2-1)	6 (6)	98.2	101.7

which rejects the ones which can not attain the required dynamic range. A reduced set of solutions is forwarded to the architecture-level design step which evaluates their behavior by time-domain simulations. The power of each solution is estimated and only ten solutions are subjected to the time-consuming yield analysis. The generation of the entire set of possible solutions takes approximately 24 hours on a 1GHz computer. Yield analysis can be run on sub-sets of solutions to find only architectures with required properties. Experimental results show that previously published state-of-the-art solutions are among the best designs but not necessarily the best.

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