

Modeling and Analysis of Regular Symmetrically Structured Power/Ground Distribution Networks[†]

Hui Zheng and Lawrence T. Pileggi

Carnegie Mellon University, Department of Electrical and Computer Engineering
5000 Forbes Avenue

Pittsburgh, PA 15213

{hzheng, pileggi}@ece.cmu.edu

ABSTRACT

In this paper we propose a novel and efficient methodology for modeling and analysis of regular symmetrically-structured power/ground distribution networks. The modeling of inductive effects is simplified by a folding technique which exploits the symmetry in the power/ground distribution. Furthermore, employment of susceptance [10,11] (inverse of inductance) models enables further simplification of the analysis, and is also shown to preserve the symmetric positive definiteness of the circuit equations. Experimental results demonstrate that our approach can provide up to 8x memory savings and up to 10x speedup over the already efficient simulation based on the original sparse susceptance matrix without loss of accuracy. Importantly, this work demonstrates that by employing limited regularity, one can create excellent power/ground distribution designs that are dramatically simpler to analyze, and therefore amenable to more powerful global design optimization.

Categories and Subject Descriptors

B.7.2 [Integrated Circuits] Design Aids - *verification*

General Terms

Design, Verification

Keywords

Power/Ground Distribution, Susceptance, Folding Technique, Design Regularity

1 INTRODUCTION

The role of a power/ground distribution network is to supply stable voltage references to the on-chip circuitry. Due to the large amount of time-varying current surges, however, designing a reliable power/ground distribution is one of the most challenging design problems due to IR drops, Ldi/dt noise and electromigration [2-9]. Consequently, as the current requirement goes up due to the increasing density of VLSI chips, power/ground distribution networks require more precise design considerations and more stringent noise budgets -- particularly as voltage supply levels are scaled to control power dissipation.

[†]This work was supported by Semiconductor Research Corporation (SRC) under contract 2000-TJ-778.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

DAC 2002, June 10-14, 2002, New Orleans, Louisiana, USA.

Copyright 2002 ACM 1-58113-461-4/02/0006...\$5.00.

Traditionally, the on-chip power/ground distribution network is modeled as a resistive network for IR drop analysis. For static/DC analysis, only current sources modeling the average current consumption are attached to the network. For dynamic/transient analysis, there are time-varying current sources modeling the switching activity of circuit blocks, and capacitors that model decoupling and intrinsic capacitance to simulate the dynamic behaviors. To accommodate the millions of resistors in such power/ground network models, hierarchical approaches [5] and multigrid-like techniques [6] have been developed. An obvious solution to the IR drop problem is to size up the wires in a power/ground distribution network. However, as the width and thickness of the wires increase, the inductance effect becomes evident for the on-chip metal layers. Furthermore, for high-performance systems such as microprocessors, the C4 packaging technology dictates the combined analysis of on-chip power grid and packaging. There has been some work which attempts to address inductance for power grid analysis, but the power grid models are generally oversimplified by either assuming tree structures or only considering self inductance [7,8,9].

In this paper we propose a novel and efficient methodology for modeling and analysis of regular symmetrically structured power/ground distribution networks. Based on a folding technique and the susceptance concept [10,11], very simple circuit models can be used to accurately capture magnetic couplings for very large power/ground distribution networks. As we will explain in detail, such modeling and analysis simplification requires certain *regularity* of a power/ground distribution network. However, imposing *some* forms of design regularity may be just what is needed to address the increasingly difficult verification problem for large power/ground distribution networks. Such forms of regularity seem to be imperative in general for closing the ever increasing "design productivity gap" [1] that is making application-specific IC design less affordable. In addition, the simplifications brought on by regularity may facilitate powerful global optimizations -- which otherwise would be impossible for more complicated models -- that ultimately produce a superior design.

This paper is organized as follows. Section 2 presents a folding technique which exploits the symmetry in power/ground distribution and is applicable both for inductance and susceptance-based models. Section 3 shows that for certain power/ground configurations, based on the properties of the susceptance matrix, the S-based model can be further simplified to facilitate much more efficient simulation without compromising the accuracy. In Section 4, the validity and efficacy of our approach is verified by the experimental results and some discussions of regularity are also provided. Section 5 draws our final conclusions.

2 FOLDING TECHNIQUE

A typical circuit model of a power/ground distribution consists of two linear networks representing the Vdd and Gnd supply respectively. The circuit macroblocks between the two networks are modeled as time-varying current sources and capacitance (including decoupling and intrinsic capacitance.) Due to the inherent symmetry, when the model does not include mutual inductive couplings, it is easy to decouple the Vdd and Gnd networks through current source transportation and capacitance splitting. We will further show here, however, that even in the presence of mutual inductance, the symmetry in power/ground distribution still enables us to reduce the circuit size by half via a circuit folding technique.

Referring to Fig. 1, suppose L_{D1} and L_{G1} correspond to two symmetrical segments in the Vdd and Gnd networks, and L_{D2} and L_{G2} correspond to a second pair. Since the self inductances and mutual inductances of the segments can be evaluated with close-form formulas which are functions of geometrical parameters, the geometrical symmetry in power/ground distribution guarantees that $L_{D1} = L_{G1}$, $L_{D2} = L_{G2}$, $M_{DD} = M_{GG}$ and $M_{DG11} = M_{DG22}$. $M_{DG12} = M_{DG21}$ approximately holds under certain conditions. Our results will show that the slight difference between M_{DG12} and M_{DG21} does not affect the accuracy of our approach to any discernible level. Therefore, for notational simplicity, we assume M_{DG12} and M_{DG21} are exactly the same for now. In summary, the geometrical symmetry results in the circuit symmetry, which further leads to the symmetry in current distribution, i.e., $I_{D1} = -I_{G1}$ and $I_{D2} = -I_{G2}$. As a result, the voltage across L_{D1} can be represented as:

$$\begin{aligned} V_{D1} &= \frac{dI_{D1}}{dt}L_{D1} + \frac{dI_{D2}}{dt}M_{DD} + \frac{dI_{G1}}{dt}M_{DG11} + \frac{dI_{G2}}{dt}M_{DG21} \\ &= \frac{dI_{D1}}{dt}(L_{D1} - M_{DG11}) + \frac{dI_{D2}}{dt}(M_{DD} - M_{DG21}) \end{aligned}$$

which exemplifies that the magnetic couplings between Vdd and Gnd networks can be folded into the self-inductances and mutual inductances inside one of the networks.

More generally, the entire inductance matrix can be formed as:

$$L = \begin{bmatrix} L_{DD} & L_{DG} \\ L_{DG}^T & L_{GG} \end{bmatrix}, \text{ where } L_{DD} \text{ and } L_{GG} \text{ represent the inductance}$$

matrices for the Vdd and Gnd networks respectively and are identical; L_{DG} models the mutual inductances between the Vdd and Gnd networks and where ideally $L_{DG} = L_{DG}^T$. Thus, the folding technique for L can be understood as follows:

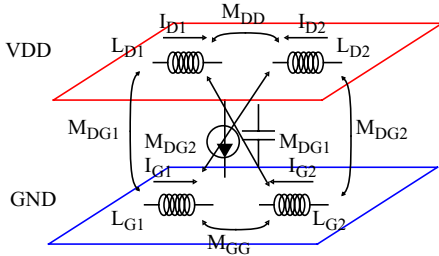


Fig. 1. Symmetry in Power/Ground Distribution

$$\begin{bmatrix} V_{DD} \\ V_{GG} \end{bmatrix} = \begin{bmatrix} L_{DD} & L_{DG} \\ L_{DG}^T & L_{GG} \end{bmatrix} \begin{bmatrix} I_{DD} \\ -I_{DD} \end{bmatrix} = \begin{bmatrix} L_{DD} - L_{DG} & 0 \\ 0 & L_{GG} - L_{DG}^T \end{bmatrix} \begin{bmatrix} I_{DD} \\ -I_{DD} \end{bmatrix} \quad (1)$$

Obviously, it holds that $V_{DD} = -V_{GG}$.

Importantly, this folding technique also works for the susceptance matrix [10, 11], since S is also a *block symmetric* matrix:

$$S = L^{-1} = \begin{bmatrix} L_{DD} & L_{DG} \\ L_{DG}^T & L_{GG} \end{bmatrix}^{-1} = \begin{bmatrix} S_{DD} & S_{DG} \\ S_{DG}^T & S_{GG} \end{bmatrix} \quad (2)$$

where

$$S_{DD} = S_{GG} = (L_{DD} - L_{DG}L_{DD}^{-1}L_{DG})^{-1} \quad \text{and}$$

$S_{DG} = S_{DG}^T = -L_{DD}^{-1}L_{DG}(L_{DD} - L_{DG}L_{DD}^{-1}L_{DG})^{-1}$ which can be derived from the formulas in [13]. Similarly, the decoupling of the Vdd and Gnd networks in terms of S can be shown as:

$$\begin{bmatrix} I_{DD} \\ I_{GG} \end{bmatrix} = \begin{bmatrix} S_{DD} & S_{DG} \\ S_{DG}^T & S_{GG} \end{bmatrix} \begin{bmatrix} V_{DD} \\ -V_{DD} \end{bmatrix} = \begin{bmatrix} S_{DD} - S_{DG} & 0 \\ 0 & S_{GG} - S_{DG}^T \end{bmatrix} \begin{bmatrix} V_{DD} \\ -V_{DD} \end{bmatrix} \quad (3)$$

Thus, a susceptance-based modeling flow can be devised, and the substantial benefits that it provides will be described in the following sections. First, the window technique [10,11] is applied to extract half of the whole S matrix, namely S_{DD} and S_{DG}^T . Then the folded S matrix is calculated as $S_{fold} = S_{DD} - S_{DG}$. We can further construct the circuit for the Vdd portion by adding the extracted resistors, transported current sources and split capacitors. The voltage waveforms on the Gnd nodes can be deduced from the simulation results using the corresponding nodes in the Vdd portion.

3 FOLDED S IS NEARLY DIAGONAL FOR REGULAR, SYMMETRICAL STRUCTURE

As presented in section 3, the folding technique can reduce the simulation effort by cutting the circuit size by half. However, this speed-up is not sufficient for the analysis improvement that is required for large power/ground distribution networks. Fortunately, we can further simplify the simulation formulation by exploiting the fact that the folded susceptance matrix is nearly diagonal when the symmetrical wires in the Vdd and Gnd distribution are very close. It should be further stressed that this is also a guideline for creating good power/ground distribution designs in general.

To illustrate our point we use the power/ground configuration shown in Fig. 4. In Fig. 2 and Fig. 3, the magnitude maps of the original and folded susceptance matrices extracted from a 5x4 power/ground distribution network are shown. In order to contrast the magnitudes more clearly, an S matrix is normalized with regard to its diagonal elements, and every entry in the matrix is then replaced by the absolute value of its logarithm. In this way, we can easily find out how many orders of magnitude the off-diagonal elements are smaller than the diagonals. In the magnitude map of the original S matrix, we can clearly see the four block matrices as in Eq. (2). It is worth noting that all the entries in S_{DG} and S_{DG}^T are negative, and because of the shielding effect of susceptance elements, the diagonal entries in S_{DG} and S_{DG}^T which model the susceptive couplings between physically close symmetrical Vdd and Gnd segments have much bigger magnitudes than the other off-diagonal elements in S.

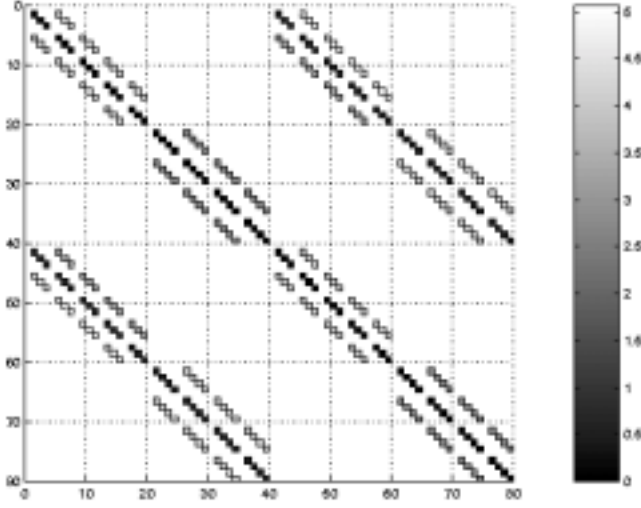


Fig. 2. Original S Matrix (normalized)

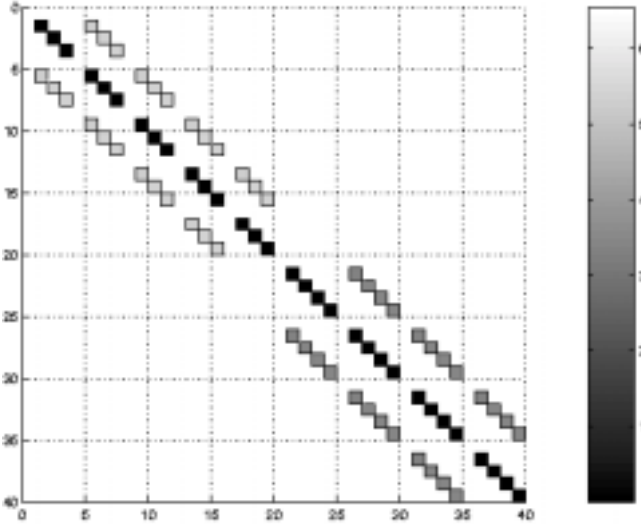


Fig. 3. Folded S Matrix (normalized)

The magnitude map in Fig. 3 shows that the folded S becomes extremely diagonally dominant. The reason is that the positive diagonal entries in S_{DD} become bigger after subtracting the negative diagonal entries in S_{DG} , while other off-diagonal elements become smaller. Therefore, it becomes possible to ignore the off-diagonal entries in the folded S without sacrificing too much accuracy for a symmetrical design such as the one in Fig. 4. However, the folding technique does not have the same effect on the inductance matrix as it does to the susceptance matrix. First of all, the original inductance matrix is not as sparse as an equivalent susceptance matrix, and it has been demonstrated that inductance is notoriously difficult to localize. Secondly, all of the terms in an inductance matrix are positive, therefore, the folding technique actually reduces the diagonal entries in the folded L matrix, which does not necessarily lead to a very diagonally dominant L matrix.

There are several benefits to using a diagonal S matrix in a transient simulation. In the extracted circuits modeling power/ground distributions, each segment is modeled as a resistor in series with an inductor or susceptor. For transient simulation, the Backward-

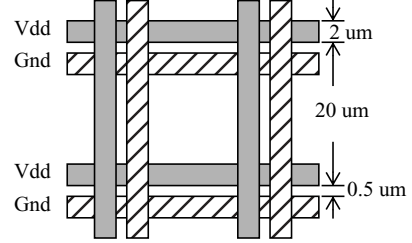


Fig. 4. Top View of Power Grid

Euler (BE) companion model for a segment, when there is no mutual susceptance, can be transformed into a combined companion model through a Norton-to-Thevin equivalent circuit transformation. This enables elimination of one node for each segment. Also, it opens the door for further speedup through either a hierarchical [5] or a multigrid-like approach [6], since the symmetrical positive definiteness of the simulation formulation which previously existed only for RC circuits, is preserved for RCS circuits here [12].

4 EXPERIMENTAL RESULTS AND DISCUSSIONS

In order to test the methodology presented in Section 2 and 3, we created power grids following the configuration shown in Fig. 4. All of the wires have a width of 2 microns and a thickness of 1 micron, and the pitch for the Vdd and Gnd wire pairs in each layer is 20 microns. To generate power grids of different sizes, varying numbers of rails are used in each layer. Current sources modeling the circuit blocks and decoupling capacitors are inserted between the symmetric Vdd and Gnd nodes on the lower layer.

Note that the distance between two immediately adjacent Vdd and Gnd lines is very small (0.5 microns) compared to the pitch. As pointed out earlier, this choice is essential to the success of our methodology, since it not only guarantees the validity of the folding technique for S_{DG} is very close to S_{DG}^T as in Eq. (2), but also maximizes the shielding effects of susceptance elements which justifies the exclusion of the mutual coupling terms. After all, this configuration turns out to be a good design since the increased capacitance between Vdd and Gnd grids due to the small spacing becomes a valuable resource of decoupling capacitance.

Table 1. Comparison of Memory Usage and Runtime

	Original S			Folded S with Mutuals					Folded S without Mutuals				
	#nodes #nonzero	Memory (Mb)	Runtime (sec)	#nodes #nonzero	Memory (Mb)	Runtime (sec)	Memory Saving	Speed up	#nodes #nonzero	Memory (Mb)	Runtime (sec)	Memory Saving	Speed up
20x20	3003 102137	13.3	48.5	1722 26348	5.9	16.6	2.2x	2.9x	882 3444	3.3	4.8	4.0x	10x
40x40	11603 409937	49.0	249.1	6642 105508	18.0	91.8	2.7x	2.7x	3362 13284	6.7	22.2	7.3x	11.2x
60x60	25803 923337	110.8	650.1	14762 237468	40.3	249.2	2.7x	2.6x	7442 29524	12.5	56.9	8.9x	11.4x

With an extraction tool that implements the windowing technique [10], we generate the original and folded circuit netlists for power grids with size 20x20, 40x40 and 60x60. Then, a special simulator which supports susceptance elements [12] is used for simulating the power grid circuits. The runtimes and memory usages are tabulated in Table 1. For all simulations, a fixed time step is used and the number of time points is 500. All the statistics are from runs on an IBM Model 7042/7043 AIX machine. As we can see, the simulations based on folded and diagonal S models

speed up by up to 10 times and save up to 8 times memory usage compared to the simulations based on original S matrices.

Fig. 5 shows several simulated voltage waveforms on a node based on different susceptance models: (1) original S; (2) folded S with mutual terms; (3) folded S without mutual terms; (4) no S. We can see a very good match among the three waveforms. However, the fourth waveform, which comes from a simulation based on a RC model, clearly deviates from the results that include inductance effects. This demonstrates the necessity of modeling inductance for top-level on-chip power grid.

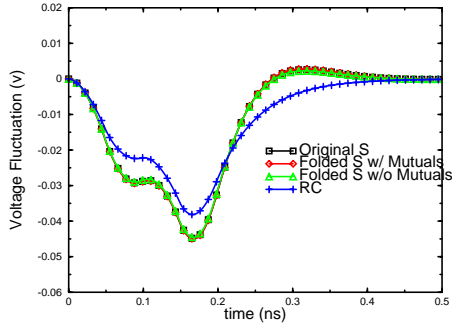


Fig. 5. Comparison of Voltage Waveforms ($d = 0.5\mu\text{m}$)

To explore the efficacy of regular symmetrically structured designs, we further analyze this structure by attempting to violate the required regularity and symmetry by distances. We change the spacing between the Vdd and Gnd lines from 0.5 microns to 8.0 microns, which is the worst violation of the symmetry. As shown in Fig. 6, there is some visible discrepancy now among the new simulated waveforms from different susceptance models. Coincidentally, there seems to be a close match between the waveforms from the original S and the diagonal folded S, which is not true in general. Also note that the waveforms from the case of 0.5-micron distance show a smaller voltage drop, which can be attributed to the bigger coupling capacitance between the Vdd and Gnd lines.

Now the important question is: given a power/ground distribution network, how do we find out whether it is regular enough for our approach to work? We can find the answer by checking the diagonal dominance of the folded susceptance matrix. More importantly, having seen the great benefit from the simplified model, we may be able to turn around to ask a question from the design point of view: given a set of technology parameters, what regularity should we impose on the power/ground distribution design in order for it to be accurately analyzed by our methodology? Clearly such a methodology can be used to select proper design rules and spacings. By experimenting with susceptance matrices associated with small-scale power/ground distribution

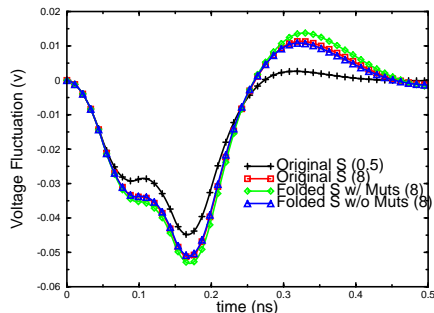


Fig. 6. Comparison of Voltage Waveforms ($d = 8\mu\text{m}$)

networks with different topologies, we can generate some design rules which can guarantee the accuracy of our modeling technique. In addition, the power/ground distribution designs, which follow those design rules, can be readily optimized by some of the existing powerful algorithms.

5 CONCLUSIONS

We have presented a new and efficient methodology for modeling and analysis of regular symmetrically-structured power/ground distributions. Unlike other approaches which either ignore inductance or use oversimplified inductance models, our approach models the magnetic couplings in a realistic manner. The powerful combination of a folding technique and the susceptance concept results in extremely simple circuit models for regular symmetrically structured power/ground distributions, which not only speeds up transient simulation significantly, but also opens the door for further speedup through either a hierarchical [5] or a multigrid-like approach [6]. Furthermore, in order to take advantage of the greatly simplified verification offered by our approach, certain design rules can be generated for power/ground distribution design, and such designs can be further optimized which would be otherwise impossible with more complicated models.

6 REFERENCES

- [1] Semiconductor Industry Association, "The International Technology Roadmap for Semiconductors: Design," 1999 Edition
- [2] H. Chen and D. Ling, "Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design," in Proc. 34-th DAC, pp. 638-643, June 1997.
- [3] A. Dharchoudhury, et. al. "Design and Analysis of Power Distribution Networks in PowerPC Microprocessors," in Proc. 35-th DAC, pp. 738-743, June 1998.
- [4] G. Steele, et. al. "Full-Chip Verification Methods for DSM Power Distribution Systems," in Proc. 35-th DAC, pp. 744-749, June 1998.
- [5] M. Zhao, et. al. "Hierarchical Analysis of Power Distribution Networks," in Proc. 37-th DAC, pp. 150-155, June 2000.
- [6] S. R. Nassif and J. N. Kozhaya, "Fast Power Grid Simulation," in Proc. 37-th DAC, pp. 156-161, June 2000.
- [7] T. Chen and C. Chen, "Efficient Large-Scale Power Grid Analysis Based on Preconditioned Krylov-Subspace Iterative Methods," in Proc. 38-th DAC, pp. 559-562, June 2001
- [8] H. Su, K. Gala and S. S. Sapatnekar, "Fast Analysis and Optimization of Power/Ground Networks," in Proc. IEEE ICCAD, pp. 477-480, Nov. 2000.
- [9] S. Zhao, K. Roy and C-K Koh, "Frequency Domain Analysis of Switching Noise on Power Supply Network," in Proc. IEEE ICCAD, pp. 487-492, Nov. 2000.
- [10] M. Beattie and L. Pileggi, "Efficient Inductance Extraction via Windowing," in Proc. DATE, pp. 430-436, March, 2001
- [11] A. Devgan, H. Ji, and W. Dai., "How to Efficiently Capture On-Chip Inductance Effects: Introducing a New Circuit Element K," in Proc IEEE ICCAD, pp. 150-155, Nov. 2000
- [12] H. Zheng, et. al. "Window-based Susceptance Models for Large-Scale RLC Circuit Analyses," in Proc. 2002 DATE, pp. 628 - 633, March, 2002
- [13] W. H. Press, et. al. *Numerical Recipes in C*, 2nd Edition, pp. 77, Cambridge University Press, 1992