

HiPRIME: Hierarchical and Passivity Reserved Interconnect Macromodeling Engine for RLKC Power Delivery

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ABSTRACT

This paper proposes a general hierarchical analysis methodology, HiPRIME, to efficiently analyze RLKC power delivery systems. After partitioning the circuits into blocks, we develop and apply the IEKS (Improved Extended Krylov Subspace) method to build the Multi-port Norton Equivalent circuits which transform all the internal sources to Norton current sources at ports. Since there is no active elements inside the Norton circuits, passive or realizable model order reduction techniques such as PRIMA can be applied. To further reduce the top-level hierarchy runtime, we develop a second-level model reduction algorithm and prove its passivity. Experimental results show 400-700X runtime improvement with less than 0.2% error.

1. INTRODUCTION

With the UDSM (Ultra Deep Sub-Micron) technology, several features about today's chips (faster operating frequencies, larger amount of transistors, smaller feature size and lower power voltage) have pushed the power delivery noise analysis onto the list of the designer's high-priority concerns. Basically, power delivery noise consists of IR-drop, Ldi/dt drop and resonance fluctuations. IR-drop has been widely discussed and extensively studied in the literature [7], [8] and [9]. Due to the roaring clock frequency, increasing current consumption, and even the clock gating feature, Ldi/dt noise is quickly emerging into another power fluctuation concern [8]. Power delivery noise, which causes the power voltage greater or lower than the ideal value, can degrade the performance severely and even make the gate function wrong. Therefore, extensive analysis of RLKC power delivery systems are required to ensure they meet the targeted performance and reliability goals.

Generally speaking, one of the major difficulties for power delivery analysis is size explosion. Tens of millions of devices and parasitics are required to be modeled and simulated for over a long time period. The traditional circuit simulation

engine such as SPICE [11] can not fulfill the demanding task in a timely manner. For this reason, hierarchical simulation algorithms have been proposed by David, Sachin, et al [8].

Model order reduction techniques have also been extensively studied in the literature [6]. Starting from AWE (Asymptotic Waveform Evaluation) [5] to PRIMA (Passive Reduction Interconnect Macromodeling Algorithm), model order reduction techniques have been successfully extended to consider inductance effects in a reasonable accuracy. Later, [7] develops an EKS (Extended Krylov Subspace) method to simulate large scale power delivery circuits with many current sources. To resolve the source waveform modeling issues, EKS has to perform moment shifting procedures to recover the proper moments.

In this paper, we propose a novel hierarchical power delivery analysis methodology. The contributions of our method are as follows: First, we establish a novel hierarchical power delivery macromodeling methodology, which integrates multiple-port Norton equivalent theorem with model order reduction algorithm to generate compact and accurate model and achieve significant runtime improvement. Secondly, we enhance the EKS method such that it no longer needs to perform moment shifting for source waveform modeling. Therefore, highly accurate simulation results are observed. Finally, to further reduce runtime, we develop a multiple level passive model reduction algorithm and prove its passivity.

The outline of this paper is as follows. In section 2, we introduce the basic power delivery network modeling, circuit formulations and model order reduction. In section 3, we present our hierarchical and passive order-reduced macromodeling methodology. In the last section, we present the experimental results.

2. PRELIMINARY

RLKC elements are applied to model power delivery system as shown in Figure 1. To reduce the simulation runtime, we decouple the linear simulation from the nonlinear simulation. Once the nonlinear simulation has been done, we use current sources and capacitors to model gate current consumption and the diffusion and gate capacitance, respectively. Therefore, the power grid analysis problem is reduced to simulate a linear RLKC network with linear time-varying current sources and measure the voltage drop at each grid. A linear RLKC circuit can be represented as a set of Modified Nodal Analysis (MNA) circuit equations as following:

$$Gx + C \frac{d}{dt}x = Bu, \quad (1)$$

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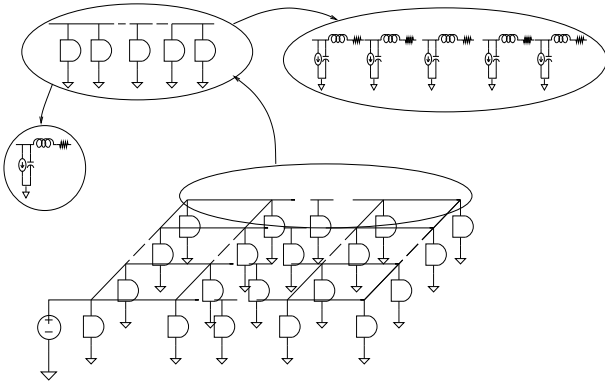


Figure 1: Modeling of the power grid network

where x is MNA variable vector, u denotes a vector of the port voltage sources and internal current sources.

$G = \begin{bmatrix} N & E \\ -E^T & 0 \end{bmatrix}$, $C = \begin{bmatrix} Q & 0 \\ 0 & H \end{bmatrix}$, $X = \begin{bmatrix} v \\ i \end{bmatrix}$ where v and i corresponds to the voltages at nodes and branch currents flowing through inductors and voltage sources. G and C matrices represent the conductance and susceptance matrices respectively. N, Q and H contain the stamping of the resistors, conductors and inductors. Note that H contains both self and mutual inductors (K elements). E corresponds to MNA current variables' contribution to the KCL equations.

Model order-reduction generates an analytic model which is a compact description of original circuits by matching their moments or poles. Circuit equations as shown in Equation 1 can be transformed to Laplace domain.

$$GX + CXs = BU \quad (2)$$

To illustrate the idea of moment matching, we expand both sides of the Equation (2) in a Taylor series around zero frequency

$$(G + sC)(m_0 + m_1s + m_2s^2 + \dots) = B(u_0 + u_1s + u_2s^2 + \dots)$$

where m_i and u_i , the coefficients of the i_{th} term in the Taylor series, are known as the i_{th} moment of x and u respectively. The basic idea of moment matching is to represent the finite unknown moments of the left hand side of the above equation in terms of the known moments of the right hand side. In PRIMA, the sources are assumed to be impulse sources in the moment matching process in order to preserve the input-output transfer characteristics. The impulse sources are constant in the frequency domain. So the Taylor expansion can be modified as

$$(G + sC)(m_0 + m_1s + m_2s^2 + \dots) = Bu_0$$

This produces an iterative relationship between the moments of the $x(s)$ and $u(s)$: $Gm_0 = Bu_0$, $Gm_i + Cm_{i-1} = 0$. This explicit moment matching method is seldom used for the reason that it has numerical stability problem, especially in the higher order iterations. To avoid the numerical errors, a set of orthogonal bases is built to span the same subspace as spanned by the finite moments of $x(s)$. The orthogonal bases V , or Krylov subspace, of matrix $A = -G^{-1}C$ and matrix $R = G^{-1}B$ is defined as $K_q(A, R) = \text{colsp}(R, AR, A^2R, \dots, A^{q-1}R)$. The dimension of the full description circuit(G, C, B) is reduced because the

rank of V is much smaller than the original matrix A . This order-reduced model can be obtained by projecting the original model (G, C, B) onto this Krylov subspace using congruent transformation. The reduced MNA matrices are denoted as $\tilde{G} = V^T G V$, $\tilde{C} = V^T C V$ and $\tilde{B} = V^T B$. Thus the compact model in the time domain are represented in MNA equations as:

$$\tilde{G}\tilde{x} + \tilde{C}\frac{d}{dt}\tilde{x} = \tilde{B}u$$

3. HIERARCHICAL AND PASSIVE ORDER-REDUCED MACROMODELING

Our hierarchical and passive model order reduction analysis consists of three steps. First we partition power grid networks into multiple blocks. Each block may contain RLC interconnect network and multiple internal switching currents. The second step is to generate Norton equivalent order-reduced model for each block. This step is divided into three phases: The first phase is to find the passive order-reduced model for the RLC interconnect network of this block. The second phase is to find the Norton equivalent current of the internal current sources. In the last phase of the second step, we attach the Norton equivalent currents at the ports of the order-reduced RLC model. At the third step, we apply integration algorithm to the macro-models generated by the first two steps and apply top level simulation.

The outline and flowchart of our algorithm are shown in Figure 2 and Figure 3, respectively. In the following subsections, we will discuss step A2.1, step A2.2 and step A3 in Figure 2.

- Algorithm:** HiPRIME (Hierarchical and Passivity Reserved Interconnect Macromodeling Engine)
- A1.** Partition the given circuit into multiple blocks
 - A2.** For each block, we generate multiport Norton equivalent order reduced circuits by the following procedure:
 - A2.1** Zero all the active sources and perform passive model order reduction for the linear circuit using any passivity guaranteed model reduction algorithm such as PRIMA.
 - A2.2** Activate all sources and short all the ports nodes to ground and find out the Norton equivalent sources at each port by IEKS or SPICE simulation.
 - A2.3** Form the Norton Equivalent circuit by attaching the the Norton equivalent sources at each port to the reduced circuit generated by the model reduction algorithms in Step A2.1.
 - A3.** Form the integrated circuit by combining all the reduced modules. Perform higher level of model order reduction such as IEKS or PRIMA when necessary.

Figure 2: HiPRIME Algorithm

3.1 Passive Reduced-Order Macromodeling of RLC Networks

After a power grid network is partitioned into multiple blocks, each block may contain passive RLC interconnect and internal switching current sources. In order to obtain a passive order-reduced model, we simply disconnect all the internal current sources to make this block a passive RLC network. The effect of these current sources on grid voltages will be considered later. We may apply a conventional passive model order reduction algorithm, PRIMA, to each simpli-

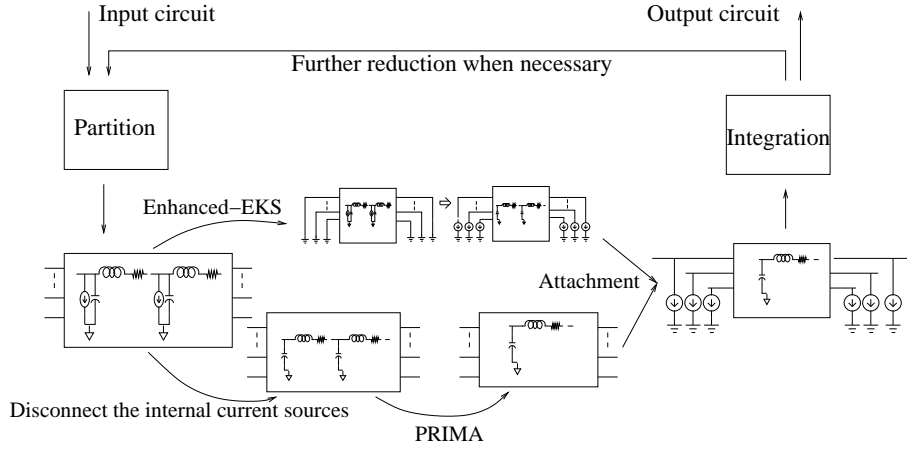


Figure 3: Flowchart for the hierarchical and passivity reserved interconnect macromodeling engine

fied block. The MNA equations for the RLC interconnect network of the i th block is as:

$$G_i X_i + C_i \frac{d}{dt} X_i = B_i u_i \quad (3)$$

where u_i is the port voltage vector of the i th block. The result of PRIMA is that, by the transfer matrix V_i , G_i , C_i and B_i are transformed into \tilde{G}_i , \tilde{C}_i and \tilde{B}_i , whose dimension are reduced. The compact MNA equation to describe this block is as:

$$\tilde{G}_i \tilde{X}_i + \tilde{C}_i \frac{d}{dt} \tilde{X}_i = \tilde{B}_i u_i$$

The benefits of model order reduction after partition include: 1) Model order reduction algorithms handle much smaller input circuit size, which means the limit of memory might be eased; 2) It also makes parallel order reduction for different blocks possible, by which the speed is improved.

3.2 Efficient Way of Finding the Norton Equivalent Current

In this section, we consider the effects of the internal current sources on grid voltages which are ignored in the previous procedure. Norton equivalent theory is used to find out the equivalent current sources at the ports and replace all the internal current sources so that the port responses of each block are preserved. To distinguish the port voltage sources from the internal current sources, we modify Equation (3) as

$$G_i X_i + C_i \frac{d}{dt} X_i = [B_i B'_i] \begin{bmatrix} v_i \\ i_{gi} \end{bmatrix} \quad (4)$$

where v_i and i_{gi} denote the independent voltage sources and the internal switching current sources in the i th block respectively. B_i and B'_i denote the position of the voltage sources and the current sources relative to the whole network. The procedure of calculating the equivalent at the ports is illustrated in Figure 4. As shown, the port currents with the port voltages set to zeros are the Norton equivalent current sources. Also as we know, port currents can be obtained by $i_{Ni} = B_i^T X_i$. To solve Equation (4) with the voltage sources u_i set to zeros, different algorithms can be applied. In our algorithm, we applied IEKS, an improved version of EKS such that no moment shifting is necessary which will be described in next session.

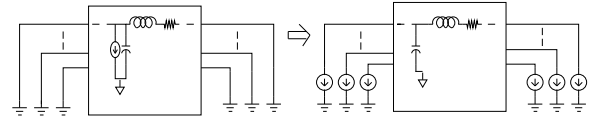


Figure 4: Finding the equivalent current of internal sources

3.2.1 Improved Extended Krylov Subspace

Developed by Janet, et al. at [7], EKS directly calculates the orthogonalized moments of the response when multiple sources are turned on at the same time. Therefore, unlike PRIMA whose runtime is heavily dependent on the port number, the runtime of EKS is independent of that. EKS models a Piece-Wise-Linear(PWL) independent source as a sum of delayed ramps in the Laplace domain:

$$u(s) = \frac{1}{s^2} \sum_{i=1}^K r_i \exp(-\beta_i s)$$

This expression contains $1/s$ and $1/s^2$ terms. Unfortunately the traditional Krylov subspace methods start the moment matching from the 0_{th} moment. EKS extends the Krylov subspace by shifting the moments toward right in the frequency spectrum.

This moment shifting in EKS is tedious and error-prone. Fortunately, we develop an improved moment calculation method which ensure the -1_{st} and -2_{nd} order moments are all zero for arbitrary finite time PWL waveform and hence the moment shifting process can be removed. Since for simulation purpose we are only interested for a specific time period, the finite-time assumption is quite general. We believe this procedure is numerically more sound than the original method.

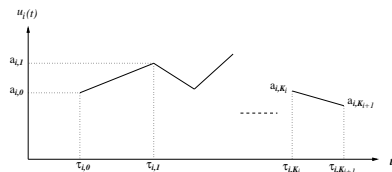


Figure 5: Waveform of the source

LEMMA 1. Given a finite-time PWL source, IEKS calculates a moment representation with -1_{st} and -2_{nd} order moments to be zero.

PROOF. Given an finite-time PWL source $u_i(t)$ as described in Figure 5, we have

$$u_i(t) = \sum_{j=0}^{K_i} \{ [a_{i,j} + \gamma_{i,j}(t - \tau_{i,j})] E_{(t-\tau_{i,j})} - [a_{i,j+1} + \gamma_{i,j}(t - \tau_{i,j+1})] E_{(t-\tau_{i,j+1})} \} \quad (5)$$

where $\gamma_{i,j} = (a_{i,j+1} - a_{i,j})/(\tau_{i,j+1} - \tau_{i,j})$, and $E_{(t-\tau_{i,j})}$ is the unit-step function with $\tau_{i,j}$ delay. By taking the Laplace transform of Equation (5) and Taylor expansion, we now have

$$\begin{aligned} \mathcal{L}(u_i(t)) &= \frac{1}{s^2} \sum_{j=0}^{K_i} \left\{ a_{i,j} s \sum_{l=0}^{\infty} (-1)^l \frac{\tau_{i,j}^l}{l!} s^l + \gamma_{i,j} \sum_{l=0}^{\infty} (-1)^l \frac{\tau_{i,j}^l}{l!} s^l \right. \\ &\quad \left. - a_{i,j+1} s \sum_{l=0}^{\infty} (-1)^l \frac{\tau_{i,j+1}^l}{l!} s^l - \gamma_{i,j} \sum_{l=0}^{\infty} (-1)^l \frac{\tau_{i,j+1}^l}{l!} s^l \right\} \end{aligned}$$

Let $\tilde{u}_{i,j}$ denote the coefficient of the s^j term. The moment representation of $\mathcal{L}(u_i(t))$ can be simplified to

$$\mathcal{L}(u_i(t)) = \{ \tilde{u}_{i,-2} s^{-2} + \tilde{u}_{i,-1} s^{-1} + \tilde{u}_{i,0} + \tilde{u}_{i,1} s + \tilde{u}_{i,2} s^2 + \dots + \tilde{u}_{i,m} s^m + \dots \} \quad (6)$$

When calculating the first two coefficients, we conclude

$$\begin{aligned} \tilde{u}_{i,-2} &= \sum_{j=0}^{K_i} (\gamma_{i,j} - \gamma_{i,j}) = 0 \\ \tilde{u}_{i,-1} &= \sum_{j=0}^{K_i} (a_{i,j} - \gamma_{i,j} \tau_{i,j} - a_{i,j+1} + \gamma_{i,j} \tau_{i,j+1}) \\ &= \sum_{j=0}^{K_i} (a_{i,j} - a_{i,j+1} - \gamma_{i,j} (\tau_{i,j} - \tau_{i,j+1})) = 0 \end{aligned}$$

□

The first two terms are eliminated and Equation (6) can be rewritten as a moment representation starting from the 0_{th} moment:

$$\mathcal{L}(u_i(t)) = \{ \tilde{u}_{i,0} + \tilde{u}_{i,1} s + \tilde{u}_{i,2} s^2 + \dots + \tilde{u}_{i,m} s^m + \dots \}$$

Table 1 summarizes the process of IEKS to calculate the first M moments.

3.2.2 System solution by IEKS

IEKS generates a system transform matrix V_i , by which the original system is transformed into a compact description.

$$\tilde{G}_i \tilde{X}_i + \tilde{C}_i \frac{d}{dt} \tilde{X}_i = [\tilde{B}_i \tilde{B}_i'] \begin{bmatrix} 0 \\ i_{gi} \end{bmatrix} \quad (7)$$

The compact form can be solved quickly in the time domain by standard integration algorithms. The solution of the original system can be recovered by $X_i = V \tilde{X}_i$. But we are only interested about the port currents in the solution. The port currents are directly obtained by $i_{Ni} = B^T X_i = \tilde{B}_i^T \tilde{X}_i$.

Algorithm: IEKS Moments Calculating Algorithm

Input: N PWL sources, $\{a_{i,0} \dots (K_i+1), \tau_{i,0} \dots (K_i+1)\}_{i=1}^N$
M, the number of moments to calculate

Output: $u_{i,m} = \{[u_{i,1} \ u_{i,2} \ \dots \ u_{i,M}]\}_{i=1}^N$,
the first M moments of the N PWL sources

Begin

for $i = 1 : N$

for $j = 0 : K_i$

$$\gamma_{i,j} = \frac{(a_{i,j+1} - a_{i,j})}{(\tau_{i,j+1} - \tau_{i,j})}$$

end

for $m = 1 : M$

$$\beta_{i,j}^{(m)} = \frac{(-\tau_{i,j})^m}{m!}$$

end

$$u_{i,m-1} = (a_{i,0} - \gamma_{i,0} \frac{\tau_{i,0}}{m}) \beta_{i,0}^{(m-1)} - \sum_{j=0}^{K_i-1} (\gamma_{i,j} - \gamma_{i,j+1}) \beta_{i,j+1}^{(m)} - (a_{i,K_i+1} - \gamma_{i,K_i} \frac{\tau_{i,K_i+1}}{m}) \beta_{i,K_i+1}^{(m-1)}$$

end

end

End

Table 1: IEKS Moments Calculating Algorithm

3.3 Macromodel Integration and Top Level Reduced-Model Simulation

After the A2 step of HiPRIME (Figure 2), we transform a block consisting of RLC segments and internal PWL currents into a passive order reduced block with current sources attached only at the ports. The new macromodel of each block is illustrated in Figure 6. The port response of the original block is preserved. We generate such macromodel

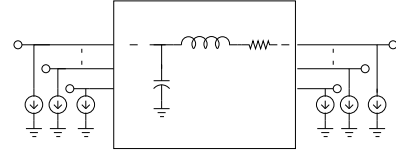


Figure 6: Equivalent circuit for each block

for each block and the entire network is integrated by combining these macromodels together. Considering each block as a node of the integrated network, we stamp them into the MNA equation of the entire network. The combination of i_{th} block and j_{th} are given in Equation (8).

$$\begin{bmatrix} \tilde{G}_i & 0 & -\tilde{B}_{ij} \\ 0 & \tilde{G}_j & -\tilde{B}_{ji} \\ \tilde{B}_{ij}^T & \tilde{B}_{ji}^T & 0 \end{bmatrix} \begin{bmatrix} \tilde{X}_i \\ \tilde{X}_j \\ u_{ij} \end{bmatrix} + \begin{bmatrix} \tilde{C}_i & 0 & 0 \\ 0 & \tilde{C}_j & 0 \\ 0 & 0 & 0 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \tilde{X}_i \\ \tilde{X}_j \\ u_{ij} \end{bmatrix} = \begin{bmatrix} \tilde{B}_{ii} & 0 & 0 & 0 \\ 0 & \tilde{B}_{jj} & 0 & 0 \\ 0 & 0 & E_i^T & E_j^T \end{bmatrix} \begin{bmatrix} u_i \\ u_j \\ i_{Ni} \\ i_{Nj} \end{bmatrix} \quad (8)$$

In this formulation, u_{ij} denotes the voltages at the common ports belonging to both the i_{th} and j_{th} blocks. u_i and u_j stand for the voltages at the ports of the i_{th} and j_{th} blocks, which are not connected with each other. B_{ii} and B_{jj} denote the connection of the internal nodes to the ports which are exclusive of each other. B_{ij} denotes the connection of internal nodes of i_{th} block to j_{th} block and B_{ji} denotes the connection of internal nodes of j_{th} block to i_{th} block. i_{Ni} and i_{Nj} stand for the equivalent port currents, which are extracted from the inside of the i_{th} and j_{th} block respectively. E_i and E_j record the connection of the internal nodes to the equivalent port currents for i_{th} block and j_{th} block.

Given this glued macromodels in Equation (8), we can further apply model order reduction and simulation techniques such as PRIMA or IEKS to the top level to save runtime. There may be more than 2 hierarchical levels and the higher level model order reduction is introduced as the following. Let us define some block system matrices for

i th and j th blocks. Define $G' = \begin{bmatrix} \tilde{G}_i & 0 & -\tilde{B}_{ij} \\ 0 & \tilde{G}_j & -\tilde{B}_{ji} \\ \tilde{B}_{ij}^T & \tilde{B}_{ji}^T & 0 \end{bmatrix}$, $C' = \begin{bmatrix} C_i & 0 & 0 \\ 0 & C_j & 0 \\ 0 & 0 & 0 \end{bmatrix}$ and $B' = \begin{bmatrix} \tilde{B}_{ii} & 0 \\ 0 & \tilde{B}_{jj} \\ 0 & 0 \end{bmatrix}$, with the internal current sources disconnected, the system is described as

$$G' \begin{bmatrix} \tilde{X}_i \\ \tilde{X}_j \\ u_{ij} \end{bmatrix} + C' \frac{d}{dt} \begin{bmatrix} \tilde{X}_i \\ \tilde{X}_j \\ u_{ij} \end{bmatrix} = B' \begin{bmatrix} u_i \\ u_j \end{bmatrix} \quad (9)$$

Use $[V_1 V_2 V_3]^T$ represent the orthogonal basis of the subspace spanned by the moments of $[\tilde{X}_i \tilde{X}_j u_{ij}]^T$ and denote $\tilde{G}' = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}^T G' \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$, $\tilde{C}' = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}^T C' \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$ and $\tilde{B}' = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}^T B' \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$, the MNA equation generated by the higher level order-reduction is noted as

$$\tilde{G}' \tilde{Z} + \tilde{C}' \frac{d}{dt} \tilde{Z} = \tilde{B}' \begin{bmatrix} u_i \\ u_j \end{bmatrix}$$

3.4 Preservation of Passivity

In order to apply PRIMA or EKS to the already reduced model as described in previous session, we need to be sure that the higher level order-reduced models are also passive. The following theorem gives us the warrant.

THEOREM 1. *During the hierarchical order reduction, the passivity of the higher level order-reduced macromodel is also preserved. That is to say, the transfer function of the higher level order-reduced system $Y(s)$ satisfies*

1. $Y(s^*) = Y^*(s)$ for all complex s .
2. $Y(s)$ is a positive matrix, that means, $Z^{*T}(Y(s) + Y^T(s^*))Z \geq 0$ for any complex s satisfying $\text{Re}(s) > 0$ and for any complex vector z .

PROOF. With the impulse voltages active at ports and applying Laplace transform to Equation (10), the transfer function can be obtained as

$$Y(s) = \tilde{B}'^T (\tilde{G}' + s \cdot \tilde{C}')^{-1} \tilde{B}'$$

For the system matrices are all real, the first condition is met naturally. To prove the second condition is also met, we start from

$$\begin{aligned} & Z^{*T}(Y(s) + Y^T(s^*))Z \\ &= Z^{*T}(\tilde{B}'^T (\tilde{G}' + s \cdot \tilde{C}')^{-1} \tilde{B}' + \tilde{B}'^T (\tilde{G}' + s^* \cdot \tilde{C}')^{-T} \tilde{B}')Z \\ & \text{Setting } w = (\tilde{G}' + s^* \cdot \tilde{C}')^{-T} \tilde{B}' z \text{ and } s = j\omega + \sigma \text{ yields} \\ & Z^{*T}(Y(s) + Y^T(s^*))Z \\ &= w^{*T} [(\tilde{G}' + (j\omega + \sigma) \cdot \tilde{C}') + (\tilde{G}' + (j\omega - \sigma) \cdot \tilde{C}')^T] w \\ &= w^{*T} (\tilde{G}' + \tilde{G}'^T) w + w^{*T} \cdot \sigma \cdot (\tilde{C}' + \tilde{C}'^T) w \end{aligned}$$

Since C_i and C_j are symmetric, $C_i^T + C_i = 2C_i$ and $C_j^T + C_j = 2C_j$. Along with the fact that C_i and C_j are nonnegative definite, it yields

$$w^{*T} \cdot \sigma \cdot (\tilde{C}' + \tilde{C}'^T) w$$

$$\begin{aligned} &= \sigma \cdot w^{*T} V_1^T V_i^T 2C_i V_i V_1 w + \sigma \cdot w^{*T} V_2^T V_j^T 2C_j V_j V_2 w \geq 0 \\ & \text{for any complex vector } z \text{ and positive } \sigma. \text{ Since } N_i \text{ and } N_j \\ & \text{are symmetric nonnegative definite matrices, we have} \\ & w^{*T} (\tilde{G}' + \tilde{G}'^T) w \\ &= w^{*T} V_1^T V_i^T (G_i^T + G_i) V_i V_1 w + w^{*T} V_2^T V_j^T (G_j^T + G_j) V_j V_2 w \\ &= w^{*T} V_1^T V_i^T \begin{bmatrix} 2N_i & 0 \\ 0 & 0 \end{bmatrix} V_i V_1 w \\ & \quad + w^{*T} V_2^T V_j^T \begin{bmatrix} 2N_j & 0 \\ 0 & 0 \end{bmatrix} V_j V_2 w \geq 0 \end{aligned}$$

for any complex vector z . From the above, we can conclude that the second passivity condition is satisfied. \square

4. EXPERIMENTAL RESULTS AND FUTURE WORK

In this section, the speed and accuracy of HiPRIME and IEKS are demonstrated and compared with other methods. We use mesh networks to model the power delivery network, which consist of lumped RC/RLC segments with many current sources attached inside. The typical values for each lumped RC/RLC segment are $R = 0.2\Omega$, $L = 1.0pH$ and $C = 0.024fF$.

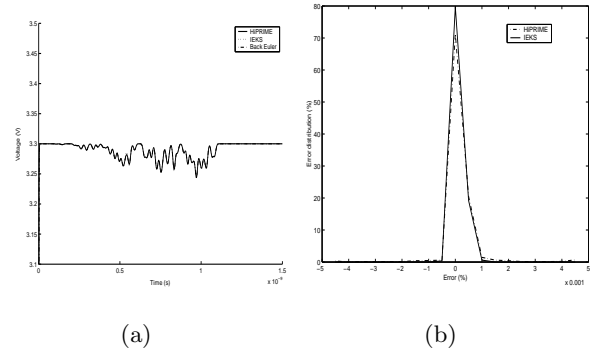


Figure 7: Accuracy analysis of RC circuit case: (a) waveform result of HiPRIME, IEKS and Back Euler (b) error spectrum of HiPRIME and IEKS

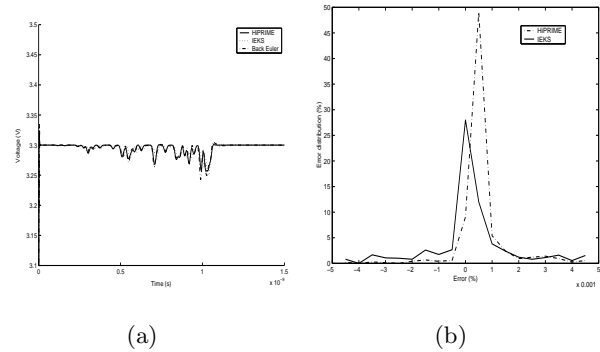


Figure 8: Accuracy analysis of RLC circuit case: (a) waveform result of HiPRIME, IEKS and Back Euler (b) error spectrum of HiPRIME and IEKS

The voltage waveforms of HiPRIME are compared with those of IEKS and Back Euler. The cases of RC circuit and RLC circuit are tested and the results are shown in Figure 7 and Figure 8 respectively. In the RC case, the waveforms are indistinguishable and the errors for 80% time intervals are within 0.001%. In the RLC case, the waveforms by HiPRIME and IEKS approximate the one by Back Euler

method very well and the errors for 50% time intervals are within 0.001%.

We implement IEKS in C code and test it on a PIII 933MHZ machine. The result is compared with our time domain solver InductWise [10] and Spice. Table 2 summarizes the runtime results and the runtime comparisons are shown in Figure 9. Significant speed improvement, 700X faster than Spice, is observed and the same tendency that the speed up increases with larger circuit size is shown.

Circuit Size	IEKS (s)	InductWise (s)	Speedup (X)	Spice (s)	Speedup (X)
7861	1.46	14.76	10.1	697.13	477.48
14081	3.88	29.77	7.67	2728.18	703.14
43541	13.49	107.05	7.93	—	—
89201	35.33	244.95	6.93	—	—

Table 2: Runtime of IEKS, InductWise and Spice

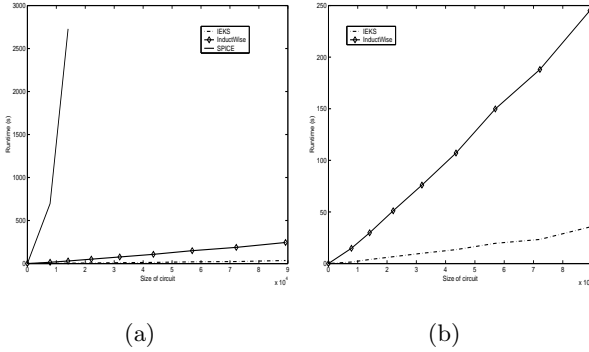


Figure 9: Runtime Analysis of (a) IEKS, InductWise and Spice (b) IEKS and InductWise

We also implement HiPRIME, flat IEKS and Back Euler in Matlab and test them on Sun Ultraspac V. Table 3 and 4 summarize the runtime results and the runtime comparisons are shown in Figures 10 and 11 for RC and RLC circuits respectively. From the figures, we can see the tendency that the speed up is more impressive when the circuit size increases.

Circuit Size	HiPRIME (s)	IEKS (s)	Speedup (X)	Back Euler (s)	Speedup (X)
203	2.52	0.89	0.36	17.1	6.79
803	2.98	1.97	0.66	78.3	26.3
2403	4.39	6.17	1.40	288.9	65.8
5003	7.93	13.18	1.66	760.1	95.8

Table 3: Runtime of RC circuit case

Circuit Size	HiPRIME (s)	IEKS (s)	Speedup (X)	Back Euler (s)	Speedup (X)
443	2.76	1.29	0.47	29.5	10.7
1883	3.87	5.08	1.31	129.8	33.5
3843	6.72	12.94	1.92	276.9	41.2
5803	11.81	27.15	2.29	427.2	36.6

Table 4: Runtime of RLC circuit case

Since the runtime of PRIMA is proportional to number of ports, we plan to investigate realizable model order reduction algorithm whose runtime is ports size independent. Also we would like to point out that the focus of this paper is not on the partition algorithms. However, a good partition algorithm is important for the performance of the hierarchical and passive model order reduction algorithm.

5. ACKNOWLEDGEMENTS

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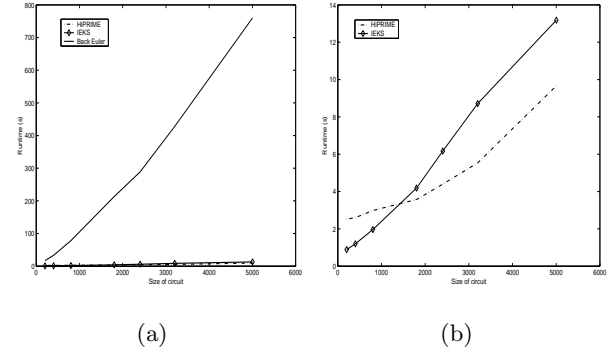


Figure 10: Runtime analysis of RC circuit case: (a) runtime of HiPRIME, IEKS and Back Euler (b) runtime of HiPRIME and IEKS

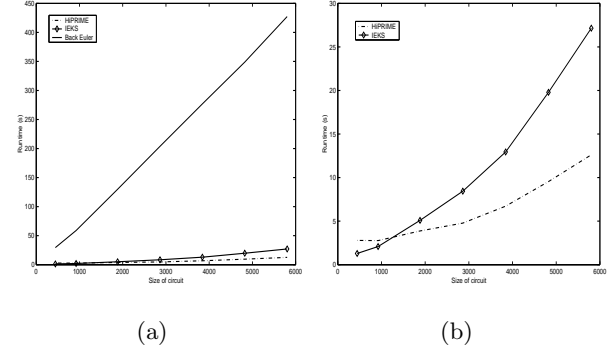


Figure 11: Runtime analysis of RLC circuit case: (a) runtime of HiPRIME, IEKS and Back Euler (b) runtime of HiPRIME and IEKS

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