A Novel Wavelet Transform Based Transient Current Analysis for Fault Detection and Localization *

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ABSTRACT

Transient current (IDD) based testing has been often cited and investigated as an alternative and/or supplement to quiescent current (IDDQ) testing. While the potential of IDD testing for fault detection has been established, there is no known efficient method for fault diagnosis using IDD analysis. In this paper, we present a novel integrated method for fault detection and localization using wavelet transform based IDD waveform analysis. The time-frequency resolution property of wavelet transform helps us detect as well as localize faults in digital CMOS circuits. Experiments performed on measured data from a fabricated 8-bit shift register and simulation data from more complex circuits show promising results for both detection and localization. Wavelet based detection method shows superior sensitivity than spectral and time-domain methods. The effectiveness of the localization method in presence of process variation, measurement noise and complex power supply network is addressed.

Categories and Subject Descriptors

B.8.2 [**Hardware**]: Performance and Reliability—*Reliability, Testing, and Fault-Tolerance*

General Terms

Algorithms, Reliability, Experimentation

Keywords

Transient current (IDD), wavelet transform, fault localization

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1. INTRODUCTION

While many solutions have been proposed to deal with background leakage elevation in IDDQ testing, IDD or transient current based testing has emerged as an alternative and/or supplementary testing method. A number of research work [3, 4, 1, 13, 8, 7, 10, 11, 6, 5] have been targeted to establish that IDD waveform analysis is an effective technique to detect many of the defects that can occur in ICs, including defects such as resistive opens and weak transistor defects, which may not be detected by conventional IDDQ testing methods.

In 1987, Frenzel and Marinos [3] investigated a small TTL and described the complete power supply current as a signature of the DUT. Hasizume et al. [4] addressed the issue of analyzing the spectral content of the IDD current under normal and faulty conditions. Beasley et al. [1] applied simultaneous pulsing on the power supply rails and analyzed the temporal and/or spectral characteristics of the transient currents. Vinnakota [13] considered dynamic power dissipation of a circuit to detect faults. Plusquellic et al. [8] proposed the concept of Transient Signal Analysis (TSA) with distributed measurement points. Su et al. [12] applied dynamic current monitoring techniques on SRAMS using extensive DFT strategy. De Paul et al. [7] used the accumulated charge (computed by numerical integration of a current waveform) for signature comparison. In the method of Sachdev et al. [10] one sample per IDD test pattern at pre-determined instance is used as signature. Muhammad et al. [6] developed DFT based signature comparison to detect faults and an integrator based approach to extract delay information, which gives an idea about the depth where the fault resides. Their method works well only for levelized circuits and the localization is susceptible to problems like *aliasing*.

In this paper, we present a novel integrated approach for fault detection and diagnosis using wavelet transform of IDD signal. Wavelet transform has the potential to resolve a signal in both time and frequency domain simultaneously. For detecting fault, the complete set of wavelet coefficients for the IDD waveform can be used as signature to compare a faulty circuit with a fault-free one and to make pass/fail decisions. Once a fault is detected, we use time-domain information in the wavelet coefficients to localize it using delay measurement technique. Multiple number of input vectors are applied to the Device Under Test (DUT) to narrow down the faulty region.

Our experimental results are based on measured current data from a 8-bit shift register and transient response obtained from *HSpice* simulation of an 8 bit Arithmetic Logic Unit (ALU) and an 8x8 Wallace tree multiplier. Wavelet based method is shown to be much superior to other techniques in terms of detection sensitivity. Time domain information extracted from wavelet coefficients is used to efficiently locate fault in the test circuits. The effectiveness of the method on fabricated chip proves its potential for practical application.

The rest of the paper is organized as follows. Section 2 gives an overview of the wavelet transform and its basic properties; Section 3 deals with the fault detection and localization using wavelet analysis; Section 4 contains experimental results; Section 5 addresses some important issues concerning practical application of the method and Section 6 concludes the paper.

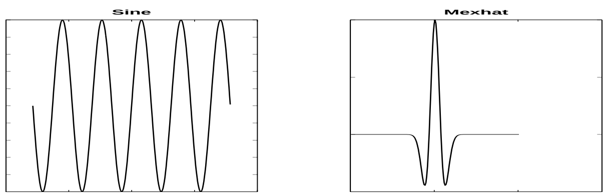

Figure 1: Basis functions for Fourier and wavelet transforms

2. AN OVERVIEW OF WAVELET TRANSFORM

Fourier analysis has a serious drawback since it transforms signal in frequency domain losing all information on how the signal is spatially distributed. Wavelet transform of a signal, on the other hand, decomposes signal in both time and frequency domain [2][9], which turns out to be very useful in fault detection and localization. In wavelet transform we take a real/complex valued continuous time function with two main properties - a) it will integrate to zero, b) it is square integrable. This function is called the mother wavelet or wavelet. Property (a) is suggestive of a function which is oscillatory or has wavy appearance and thus in contrast to a sinusoidal function, it is a small wave or wavelet (figure 1). Property (b) implies that most of the energy of the wave is confined to a finite interval. The CWT or the Continuous Wavelet Transform of a function $f(t)$ with respect to a wavelet $\Psi(t)$ is defined as:

$$W(a,b) = \int_{-\infty}^{\infty} f(t)\Psi^*_{a,b}(t)dt \quad (1)$$

$$\text{where } \Psi_{a,b}(t) = \frac{1}{\sqrt{|a|}}\Psi\Big(\frac{t-b}{a}\Big) \quad (2)$$

Here a,b are real and $*$ indicates complex conjugate. $W(a,b)$ is the transform coefficient of $f(t)$ for given a, b. Thus the wavelet transform is a function of two variables. For a given a, $\Psi_{a,b}(t)$ is a shift of $\Psi_{a,0}(t)$ by an amount b along time axis. The variable b represents time shift or translation. Since a determines the amount of time-scaling or dilation, it is referred to as *scale* or dilation variable. If $a > 1$, there is stretching of $\Psi(t)$ along the time axis whereas if $0 < a < 1$ there is a contraction of $\Psi(t)$ (figure 2). Each wavelet coefficient $W(a,b)$ is the measure of approximation of the input waveform in terms of the translated and dilated versions of the mother wavelet. Figure 1 compares the basis signals of DFT and wavelet transform. The mother wavelet shown in figure 1 is called *Mexican hat* wavelet. Figure 2 shows the translated and dilated mother wavelet used to approximate an IDD waveform of a test circuit.

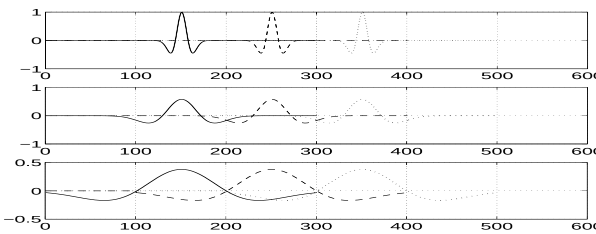

Figure 2: Translated and dilated mother wavelet (*mexican hat*) used in the wavelet decomposition

3. IDD ANALYSIS USING WAVELET TRANSFORM

3.1 Fault Detection

The Fault Detection strategy is based on comparing current signature of the DUT with the signature of the golden (fault-free) device. Input test stimuli are chosen randomly in our detection process. For each stimulus applied to the DUT, we compute the wavelet coefficients of the transient current and compare them with those for the golden device with the same input. The comparison in our case, is made by calculating the Mean Square Error (MSE) between the two sets of wavelet coefficients. Mean Square Error is chosen for comparison because it is a simple metric that can effectively detect faults. The pass/fail criterion can be decided by comparing the value of the MSE with a pre-selected test margin. Since the signature is based on wavelet coefficients, we take into account both the time and frequency components simultaneously in the transient current signature. This gives us better sensitivity in fault detection than methods based on only spectral [4] [10] [6] or only time-domain components [13] [6].

For comparing the effectiveness of our detection scheme with existing methods based on pure spectral and pure time domain contents of the IDD signal, we used a common metric referred as $normRMS$ which is defined in equation 3. It computes the root mean square of the difference between the coefficients for golden circuit response (G_i) and those for the DUT (F_i) as a fraction of the golden circuit coefficient(G_i) and can be considered as the direct measure of sensitivity. For the time domain method, we used the charge integration (as discussed in [7]) for comparison.

$$normRMS = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\Big(\frac{F_i - G_i}{G_i}\Big)^2} \quad (3)$$

3.2 Fault Localization

An important advantage of wavelet based analysis of the transient current is its ability to efficiently localize fault.

For a faulty device, we can observe the wavelet coefficients and determine the delay at which the response of the faulty circuit deviates significantly from that of the fault-free one. We then use this information to identify region where the fault resides. There are two advantages of identifying the faulty region. First, it may be possible to improve the process and yield. Second, we can use this information either for fault tolerance, or to isolate a small portion of the circuit containing the fault.

Figure 3 depicts a simple test circuit consisting of a set of inverters in cascade. We use this circuit to explain how we measure delay and how it can be used to localize faults. First we apply input stimuli to the fault-free inverter chain as shown in the figure 3 and monitor the IDD waveform. We then introduce a metal bridge of resistance 1kΩ between T3 and supply line and obtain the IDD response. We repeat the same procedure for a similar fault at position T5. Figure 4 shows the plot of IDD for these three cases. Figure 5 shows the wavelet coefficients for the IDD waveform at four different scales. The faulty responses deviate from the fault-free case at some time instant after the transition in the primary input. We call this delay between the input transition and the point of deviation in the time axis as T_d (Figure 6). This is due to the propagation delay through the cells, since the fault is not activated until the effect of an input transition propagates to it. Since the propagation delay to T5 is more than that to T3, the point of deviation for fault at T5 is shifted right in time axis from the point for fault at T3.

One interesting observation we can make here is that T_d can be used as a measure of depth in the circuit at which the fault resides. Since T_d is the propagation delay to the point where the fault is located, we can calculate minimum and maximum propagation delay along each path in the DUT in which the effect of an input transition propagates and compare that to T_d to select a set of potential faulty cells.

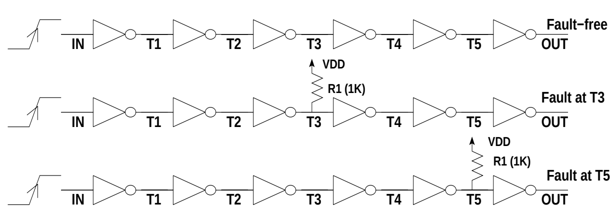

Figure 3: Inverter chain with bridging fault at T3 and T5

Figure 4: IDD Waveforms for the inverter chain with and without fault

Wavelet coefficients give us a more efficient way to calculate T_d than using simple integration [6] or a point-by-point comparison of the IDD signal. Wavelet transform can resolve a signal in time axis at different scales or frequencies. Hence we can compute T_d for multiple frequency components simultaneously using wavelet decomposition. This helps us to automatically get rid of the DC component in IDD. We can also avoid the *aliasing* effect, which may be present in the integration based method. By *aliasing* we mean that two sufficiently varying IDD waveform may have same area under the IDD curve which can lead to wrong delay computation. Since we can compute T_d at different scales in wavelet analysis, there is barely any chance of *aliasing*.

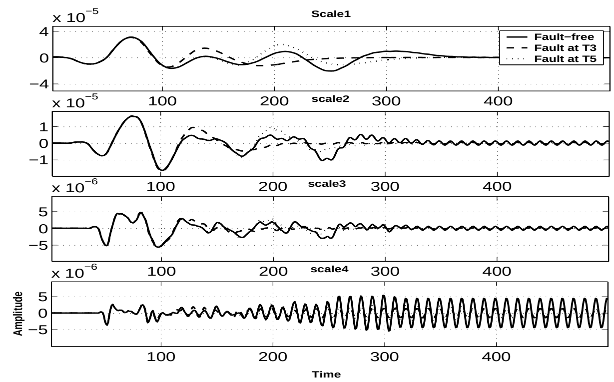

Figure 5: Plot of Wavelet coefficients at different scales for the IDD waveform in figure 4

Table 1: Fault localization steps

Locate-fault (DUT, Golden Device, Cell Delays)
1. Initialize set S with all cells in DUT 2. Apply a random transition $I_0 \rightarrow I_1$ to both the DUT and golden device. Check if a fault is detected by wavelet based method 3. If detected, compute the delay (T_d) by comparing wavelet coeffs of DUT and golden device, else go to step 2 4. If $T_d > 0$, *Partition* the circuit into set of faulty (Sf) and fault-free cells (Sff) for the input and delay, else go to step 2 5. Set $S = S \cap Sf$ 6. If terminating condition satisfied, exit, else go to step 2

The fault localization algorithm is depicted in table 1. We start by initializing S, the set of potential faulty cells at a particular iteration, with all cells in the DUT. If a fault is detected for an input transition $I_0 \rightarrow I_1$, we compute the delay. The delay computation unit compares wavelet coefficients of the fault-free and faulty response at different scales and determines the point in time axis where the wavelet components of faulty response vary by a pre-determined threshold from those of the fault-free response. We discard the high frequency components for delay computation.

Partition is a method for dividing the cells in the DUT into two non-overlapping sets to distinguish faulty cells from the non-faulty ones based on input transition and T_d. The partitioning algorithm traverses the cells in topological order and checks if a particular cell can be potentially faulty based on the min-max propagation delay to the cell. We can narrow down the faulty region by applying more input transitions and by taking intersection between previous faulty set and the current one.

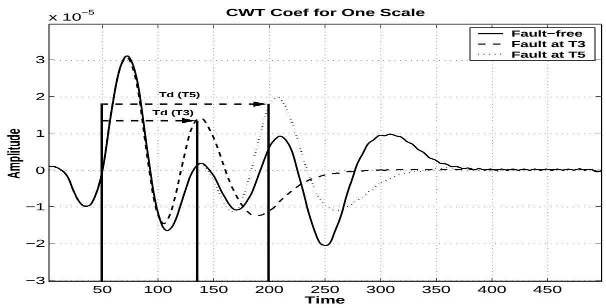

Figure 6: Plot of Wavelet coefficients for one scale showing measurement of delay

4. EXPERIMENTAL RESULTS

The detection and localization algorithm was implemented in *C*. We used *Matlab* toolbox for wavelet to perform wavelet decomposition of the IDD signl. Mother wavelet used in wavelet transform was *db2* [2]. The algorithms were tested on the measured data from the fabricated test chip for a 8-bit shift register. Detection and localization methods were also tested on simulation data from more complex circuits.

4.1 Results for a fabricated 8-bit shift register

The experiments used a 8-bit shift register in which several mask defects were designed. Transmission gates were connected to selected nodes of the circuit to emulate the presence of open defects. When a transmission gate is off, the corresponding open defect is activated. The circuit was designed with ES2 n-well dual metal 1.0μ technology. Current was measured by sensing the voltage drop at a very low inductive MP930 Caddok 300Ω resistor with a Tektronix P6247 1 GHz bandwidth differential probe. For testing the wavelet based detection and localization method, we worked with open defects preventing clock propagation from the defect site to the register.

Table 2 presents comparative results for the detection sensitivity of the wavelet, FFT and charge integration based method. The fault K_i implies that transmission gate between clock line and i-th register is open. It can be observed that the sensitivity for the wavelet based method is order of magnitude higher than either FFT or charge integration method. This difference is plotted in figure 7 in logarithmic scale. The superior sensitivity of wavelet can be attributed to its decomposition of the IDD signal in both time and frequency axis. Higher sensitivity makes wavelet a better candidate for fault detection in digital CMOS circuits, especially for parametric faults which are more difficult to detect.

Table 3 presents the localization results for the open defects in table 2. The delay T_d to each node K_i is computed from *Hspice* simulation of the extracted layout, which is then compared with the delay obtained from comparing the wavelet coefficients of the measured current and that obtained from simulation. The localization of fault, depends on how accurately we can measure the delay. The delay obtained from the measured data varies below 8% on average which is good enough to identify the fault location, i.e. which transmission gate is open.

Table 2: Comparison of sensitivity of wavelet based detection with FFT and charge integration techniques

Fault	$normRMS$ (Wavelet)	$normRMS$ (FFT)	$normRMS$ (Charge)
K2	166.910	1.599	0.973
K3	109.921	1.508	0.948
K4	108.130	1.342	0.922
K5	215.780	1.293	0.872
K6	225.603	1.757	0.813
K7	313.904	5.097	0.698
K8	418.470	5.065	0.544

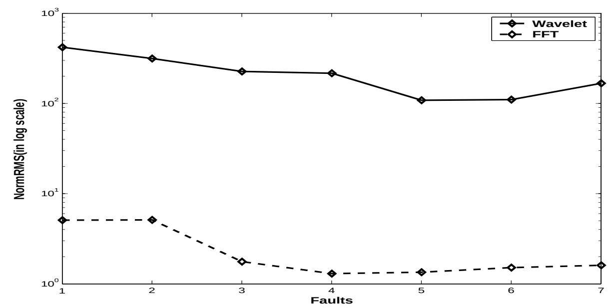

Figure 7: Comparison of fault detection sensitivity for the fabricated chip

Table 3: Localization results (in terms of delay) from the test chip

Fault	Delay from measured data (ns)	Delay from simulation (ns)	% Variation
K2	2.50	2.20	13.6
K3	7.00	7.60	7.8
K4	11.50	12.00	4.1
K5	14.20	15.53	8.6
K6	16.25	17.83	8.9
K7	19.50	19.88	1.9
K8	21.75	20.00	8.8

4.2 Simulation results for more complex circuits

Wavelet based methods were tested on simulation data from more complex circuits. Fault detection was performed for an 8x8 Wallace tree multiplier with around 800 cells and an 8-bit integer ALU with around 1000 cells, while for testing the localization method we used the 8-bit integer ALU. The circuits consisted of cells from the LEDA library for which the delay of each cell was known for different input conditions. We introduced different types of faults in the circuit and simulated the circuit with HSpice for a 0.25μ

TSMC technology library. Random input stimuli were applied to detect and localize faults.

Table 4 demonstrates the superiority of wavelet based detection compared to FFT and charge based technique. Resistive shorts and opens as well as parametric faults are used for comparison. For all the cases wavelet has a much higher sensitivity than current based techniques, proving its effectiveness for larger circuits.

Table 5 shows how our fault localization method converges as more and more test vectors are applied. The partitioning algorithm identifies a potential faulty set of cells for each test vector activating the fault. It uses the delay information obtained from wavelet coefficients. Concentrating on the common set of identified cells in two iterations of *Partition*, we norrow down our selection of cells. For the results in table 5, we inserted a metal bridge in the test circuit and applied a set of random vectors. Column 2 is the number of cells in the region identified as faulty at a specific run of partitioning. As we apply more number of vectors this region is narrowed down to almost 1% of total cells.

Table 4: Comparison of sensitivity for ALU and Wallace tree multiplier circuit

Design	Fault	$normRMS$ (Wavelet)	$normRMS$ (FFT)	$normRMS$ (Charge)
8-bit ALU	Bridge (Vss)	147.189	0.275	0.244
	Open	21.482	0.068	0.158
	Vth (10%)	255.378	0.093	0.189
	Bridge (Vss)	58.688	0.174	0.247
WTM (8x8)	Bridge (Vss)	46.566	0.215	0.283
	Bridge (Vdd)	304.322	0.276	0.209
	Open	477.436	0.034	0.083
	Vth (10%)	701.924	0.119	0.184

Table 5: Convergence of localization with increasing number of test vectors

# vectors	Cells in faulty region	% of total cells
1	398	39.25
3	112	11.05
7	59	5.82
12	33	3.25
17	10	0.99

Table 6 shows our experimental results for different types of faults injected in the test circuit at random locations. We successfully detected and localized faults in all the cases. How narrowly we can identify the faulty region largely depends on the number of input stimulus applied. We terminated our localization process if either we were able to localize the fault in 10% of the total cells or we have run 20 iterations of *Partition*. This was to limit the enormously slow *Hspice* run. Column 3 lists the number of random test vectors used (tests that detect the fault). Column 4 shows the number of cells in the identified region, which measures how accurately we can localize the faults. Column 5 lists the number of cells in the faulty region as percentage of total cells in the circuit.

Table 6: Fault Detection and Localization result for an 8-bit ALU

Fault	Detected/ Located	# vectors	Cells in faulty region	% of total cells
Metal bridge (with VDD)	Yes/Yes	13	71	7.00
Metal bridge (with GND)	Yes/Yes	7	91	8.88
Gate oxide short	Yes/Yes	16	52	5.13
Open	Yes/Yes	3	72	7.10
Metal bridge (with GND)	Yes/Yes	4	62	6.11

5. FACTORS AFFECTING LOCALIZATION

5.1 Effect of Power Supply Network

Our experiments assume that the circuit consists of only one module that is directly connected to the power supply pin. But in real chip, power supply network is usually designed as a mesh-like grid with different modules connected at different points on the grid. Wavelet based localization method can be extended to general mesh-like power-supply network. It can be observed that our localization method can be effective if we can ensure that the occurrence of a fault in a module does not significantly affect the current waveform in others. We simulated a power grid described as a RLC mesh with three different modules: an adder, a multiplexer and a comparator, connected to different points of the grid. It is observed that IDD waveform for fault-free modules does not suffer significant changes for a fault in another module, which verifies the applicability of localization for mesh-like power network.

5.2 Mother Wavelet Selection

Choice of mother wavelet is another issue that may affect computation of the T_d and thus localization. One of the advantages of wavelet transform is that it is adaptive i.e. we can selct a mother wavelet which can best approximate the input waveform. We experimented with a number of mother wavelets e.g. *db2*, *morlet, Mexican hat, haar* [2] [9] etc. and observed how T_d differs for different wavelets for a particular bridging fault in the ALU. Localization, as depicted in table 7, is best for *db2* and hence, we can use it as mother wavelet for testing the ALU.

Table 7: Localization results using different mother wavelets

Mother wavelet	# vectors	Cells in Faulty Region
db2	7	90
morl	7	101
mexh	12	98
haar	17	113

5.3 Effect of Sampling Frequency

The sampling rate at which the IDD waveform should be monitored is important because it affects the measurement noise and applicability of the method in real time. Ideally we need to sample the IDD waveform at above the Nyquist rate (i.e. twice the maximum frequency) to keep all the frequency components in the sampled data. However for detecting a fault, it has been observed that we do not need high sampling frequency [11]. This holds true for localization too because we can localize effectively without considering the high frequency spectral components of the IDD waveform. It is observed that we can sample the current waveform at as low as 50ps interval and still get a localization area less than 10% of the total cells for the test circuit.

5.4 Process Variation

The impact of process variation has to be taken into account in determining test margin for detection. Process variation also affects the delay along a path primarily because individual cell delays vary with process parameter changes. We modeled the process variation as transistor threshold (Vth) variation [14]. We have observed that if we compute test margins (the pass/fail limit and the delay threshold) based on 10% Vth variation, we can still detect and localize faults effectively. The impact of process variation on the localization is in terms of the resolution of the faulty region. Table 8 lists our experimental results with variations in Vth for a particular bridging fault in the ALU.

Table 8: Effect of process variation on localization

Vth change		# vectors	Cells in faulty region
NMOS	PMOS		
0%	0%	7	90
5%	5%	7	92
5%	-5%	7	92
-5%	5%	7	95

5.5 Effect of Measurement Noise

The hardware used to measure IDD waveform has some fixed resolution and introduces error in the measured waveforms. Typically the current waveform measured off-chip loses some high frequency components due to the presence of decoupling capacitance. As observed from the experimental results on the test chip, our method does not suffer significantly from measurement noise. This is also established from the results from simulation runs with the larger circuits, since, we consider only low frequency components of the waveform and still get efficient detection and localization.

6. CONCLUSIONS AND FUTURE WORK

A novel wavelet based IDD waveform analysis for fault detection and location is presented. Wavelet based delay computation method has been shown to withstand IDD waveform changes due to process and measurement noise due to its ability to do multi-resolution analysis of the IDD signal. Experimental results for measured data from a chip as well as for simulation data from larger circuits validates the technique's practical application.

Generation of optimal set of input stimuli for fault detection and localization is necessary to make the testing process more efficient. Test vectors for fault detection will be similar to that for IDDQ test. However, for localizing faults, automatic generation for optimal set of input vectors is non-trivial. Our approach to fault detection and localization can also be effective for pure analog or mixed-signal circuits. Currently, we are working on these aspects.

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