PANEL: Whither (or Wither?) ASIC Handoff?

Chair: Michael Santarini, EE Times, San Mateo, CA

Organizers: Sudhakar Jilla, Synopsys, Mountain View, CA and Mark Miller, Tera Systems, Campbell, CA

Abstract

The traditional ASIC netlist handoff is changing - but to what? Is RTL handoff finally a reality? Or, will a placement-based handoff model emerge? Are differences among underlying tool technologies and methodologies only cosmetic? Or, are there fundamental business and IP distinctions? These and other questions will be discussed as the panel examines the future of the designer - ASIC vendor - EDA vendor relationship.

Panelist Statements

Tommy Eng
Tera Systems, Campbell, CA

Complex ASIC designs are encountering production delays and multifaceted design closure issues, caused largely by the need to consider physical-design-induced performance factors brought on by DSM effects of the latest manufacturing processes. These factors must now be modeled in the front-end of the design flow to ensure design closure. The EDA industry has reacted by developing a new generation of Physical Synthesis tools taking physical modeling effects into account during synthesis and optimization. Unfortunately, its application is resulting in challenges for system designers and their ASIC vendors by driving mandatory methodology changes, i.e., moving the sign-off point up to the RT level, or down into the physical domain with the inclusion of placement data. This is further complicated by a shortage of physical design expertise within system design teams and the need for better RTL handover methodologies and tools for ASIC vendor support teams. One thing is abundantly clear: higher quality RTL will result in faster chips, sooner. Visibility into downstream implications of RTL, early in the design process, has enormous impact on design convergence and on-time schedule performance.

Sandeep Khanna
Synopsys, Mountain View, CA

Timing closure is becoming a mainstream problem for most designs for technologies at 0.18µm and below. Timing closure, the main value proposition of the new generation of Physical Synthesis tools such as Physical Compiler from Synopsys, eliminates the surprises between actual and expected interconnect loading and coupling at different stages in the design process that manifest themselves as chips failing to meet the target speeds. This is achieved by considering physical effects much earlier in the design process. The traditional netlist based signoff model has also similarly evolved to a placement based signoff model where customers hand off netlist and placement to the vendors, who complete detailed routing and are seeing a strong correlation with the earlier predictions made during Physical Synthesis. Customers are already beginning to experience benefits in the form of performance and productivity boosts. Vendors also see the benefit in being able to deliver silicon on time and eliminating the painful iterations between synthesis (customers) and routing (vendors). Some models are extending placement-based signoff to RTL or floorplan stages. By definition, a pure RTL signoff model involves handing off RTL instead of netlist and/or placement. The challenge is to develop tools that can give an indication of the ability to close timing without actually synthesizing or doing any physical design. If and when such tools become a reality, certain classes of designs can benefit from an RTL signoff. Placement signoff is here today while RTL signoff still remains a pipe dream.

Kamalesh Ruparel
Cisco, San Jose, CA

It is no longer an illusion. The verdict is in: timing closure is and continues to be a formidable challenge in today's ASIC designs. This is because as we increasingly soak ourselves in VDSM technologies, physics presents all manner of difficulties in physical design, signal integrity, wild defect mechanisms, etc. The sudden downturn in the economy has only exacerbated the situation by making these problems even costlier to surmount. High end (8 million gate and above) ASIC design is no longer an exclusive club – even medium sized ASICs (3 to 7 million gates) are getting to experience the spicy sauces of VDSM.

At a broad level, ASIC designs can be broadly bucketed into three major groups: the very high-end (die sizes of 18+ mm on a side, 500+ MHz clock frequency), mid-range (die sizes of 10 - 15mm on a side, 125 - 500 MHz), and the low end (die sizes of <10mm on a side, < 100 MHz).

In the low end ASIC design, RTL sign-off is possible, but ultimately ends up becoming an ASSP product. For mid-range to high-end ASIC designs, we see the RTL sign-off model as a complete misfit. Intricate dependencies between external versus internal IP, tools and methodologies, logical and physical design processes, functional verification and AC-signoff, ASIC/EDA/customer partnerships, die-size sweet spots and needed packaging technologies, TTM and yield/volume ramp-ups, and so on make it practically impossible for a true RTL-signoff to become a reality.

For these upper-tier ASIC designs, the only prayer to a reasonable turnaround time (TAT) and a predictable timing closure is some form of a placement based ASIC handoff. In order to achieve such a handoff with any significant value, all the necessary dependencies mentioned above need to be carefully managed while at the same time leveraging the best available technologies such as virtual prototyping and physical synthesis. Forcing designers and architects to view physical design as an integral and necessary part of the design process has now become inevitable. Wirability, congestion, power and clock planning have to be dealt

with weeks before RTL gets frozen. What was a paradigm shift a couple of years ago is now becoming mainstream: physical synthesis has effectively conquered the land of the inadequate statistical WLM. As if this were not enough, a thorough SI analysis of the routed netlist is mandatory before final tapeout. All of this has not only increased the number of iterations between the logical and physical worlds, but has also squeezed the requirements of overall TAT windows available for design development.

RTL signoff, then, is another way of throwing the problem over the wall... just a little sooner. Unfortunately, there is a tendency on the part of the vendors to promise a single panacea to a customer's timing closure and other ASIC engineering challenges. The sheer nature and complexity of the problem prevents a single EDA or ASIC-process solution from achieving success across all designs. So, while a particular technical solution/tool may seem to provide a great solution for one class of designs, it will most likely fall apart in a different class of designs. The required results can only be achieved with a multitude of solutions, a disciplined methodology, steadfast execution and carefully managed three-way partnerships between EDA, ASIC and design houses.

Tom Russell
IBM ASIC, Burlington, VT

ASIC methodology must evolve to adapt to advances in process technology and EDA tools. The widespread acceptance of physical, timing/placement-driven synthesis, coupled with the advent of a new breed of powerful architectural RTL-stage design planning tools, is surely driving a shift away from today's traditional netlist signoff for ASICs. For many ASIC customers, this will drive them to take on more of the back-end, lower-level activities prior to sign-off, but for another class of customers - perhaps less cutting edge in their needs and unwilling to invest in mastering deep sub-micron effects – an RTL signoff model will be both efficient and economically attractive. For these reasons, signoff engagement models will be migrating in both directions and ASIC vendors are responding today to meet these changing customer needs by offering flexible engagement models.

Kazu Yamada
NEC Electronics Inc., Santa Clara, CA

Rapid and consistent changes in the technical landscape have forced the diminishing of the traditional definition of ASIC hand-off. It is critical and important to have a clear and comprehensive hand-off definition that defines boundary conditions among design stages in today's complex ASIC design projects. However, hand-off no longer means "event horizon" for both the ASIC user and the ASIC vendor. In a way, there is no hand-off any more, in that the absolute boundary has become a matter of job sharing. An ASIC user can "interface" his designs to the ASIC vendor at C language level or all the way down at GDSII level, depending on the user's preference. However, level of involvement or interaction between system/chip designer and ASIC provider always starts from design definition, and lasts to deep inside of the physical implementation stage. Only the magnitude of interaction varies from project to project, primarily due to the choice of balance between time-to-market and level of optimization to the silicon technology. ASIC vendors should be capable of handling this multi-level or continuous hand-off process in order to provide the most value to their customers. Besides, the higher the interface level, the more value-add from the ASIC vendor point of view, resulting in a better chance to lock in customers.