PANEL: Analog Intellectual Property: Now? Or Never?

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Abstract

There is considerable controversy as to whether or not the trade in analog intellectual properties (IP) will ever represent a viable business opportunity. One school of thought suggests that analog design will always be too specialized to constitute a major market; another school of thought says this will be big business if certain nagging technical problems are solved. While the demand for analog interface components is high, the ability of IP creators to render it in a tradable format is limited. And the ability of digital design teams to successfully utilize analog IPs — without a considerable amount of handholding — is similarly limited. EDA tools here are looked upon as both culpable and offering the best hopes for the future.

This panel of experts — representing analog designers, analog EDA tool providers, silicon foundries and analog IP vendors — bring their own points of view on some of the business and technology issues which need to be resolved to provide the context for analog IP development and trade. Among the open questions:

- Is IP created and validated within the design environment for re-use a more productive approach than imported IP? How many 'traditional' analog designers would admit they are still using kit parts and breadboards — maybe even SPICE and manual IC layout techniques — today in their every-day job?

- What CAD tools are needed to help analog designers? Are newly emerging EDA technologies, designed to enhance analog design productivity, maturing rapidly enough to be accepted by designers?

- What is the future of analog designs at the very low voltage-swings coming with sub-100nm CMOS?

- Though silicon foundries need to process a wide set of external IP offerings in order to allow their users to build complete systems, are foundries seeing enough activity in analog IP designs to justify specialized fab runs or the kind of process tuning that would allow analog and digital IPs to coexist on the same chip?

- How likely – and how soon – can we get to analog IP development and trade?

Technology Issues

Process scaling has enabled unprecedented levels of integration. The most advanced systems-on-chip (SoC) now embodies 200 million transistors on one IC, and that number is expected to increase exponentially over the next decade. Rather than create new designs from a blank slate, design teams are reusing previously-designed blocks and importing the work of other design teams into their efforts. As a consequence, analysts have predicted an exponential growth in the market for IPs — that functional IC blocks will be traded externally, and well as between design departments of a large IC company. Though ARM and MIPS CPU cores now constitute the largest number of blocks traded between companies, analysts project that future trade will include other CPU and DSP cores, memories, communications protocol controllers and multimedia decoders, as well as bus interface components.

With more and more SoC makers hoping to include analog functional blocks as a means of differentiating their designs, it is therefore tempting to believe that analog IP can be created, traded and integrated with the same tools and methodologies with which digital IP are moved about. But analog has a different heritage and calls forth a different set of design issues. The simple act of moving a high-speed digital signal off-chip (the use of an analog line driver) can produce more heat and noise, and utilize more power than the SoC design team is prepared to cope with. The problem becomes more complex with the sophistication of the analog blocks that are incorporated: cable drivers and bus interface components present one level of difficulty; operational amplifiers and phased locked loops present another level; data converters and RF interfaces put most digital design teams into uncharted territory.

Currently, every manufacturer who licenses an analog IP must provide an engineer (or an engineering team) along with the IP just to get it working properly in the customer's design. There are two reasons for this: First, analog designs are typically process-specific and do not scale with shrinking CMOS geometries. Unlike digital circuits that can appear to gain performance in a process shift from (say) 0.18-microns to 0.13-microns, analog circuits can loose performance and, in some case, cease working entirely. Dynamic range is severely curtailed with submicron CMOS, and parasitics (like interconnect resistivity and gate capacitance) play a much larger role. Analog functions must frequently be entirely redesigned in the move from one process environment to another, but there are limitations on the extent to which redesign will help. Participants in panels at this year's International Solid States Circuits Conference (ISSCC), for example, were openly terrified of the leakage currents that would appear at 100- and 90-nm CMOS geometries. Second, analog functional blocks — performing well in isolation — will often be disabled on a digital SoC substrate. Digital switching noise, bubbling up through the substrate, is frequently identified as the culprit.

Newly emerging EDA technologies, designed to enhance analog design productivity, provide some relief. There are two sets of tools needed: One set would enable designers — regardless of whether their primary expertise is analog or digital — to create analog IP cell blocks more rapidly. The expression "analog synthesis," analysts agree, has been abused because it will not (on the near horizon) offer the same kind of movement from high-level language description to gate-level implementations. However, there are many new-generation model-generating, circuit-resizing and optimization tools — many available from silicon foundries — that will speed the process of moving analog functions from one geometry to another. Some new tools provide "design tuning" that allows IPs to verified within the design environment where they are created. The second set of tools —

speedier full chip simulators — would allow analog IPs to verified in the same environment with digital IPs.

But the question remains whether the tools will develop rapidly enough to satisfy analog IP creators. Even among digital design teams, there seems to be trepidation and concern whether the tools will continue to give trustworthy information at 100-nm and below. And these concerns will keep analog designers on their toes — well before the 100-nm mark.

The Positions summarized

Mike Brunoli, Chief Technology Officer, Nurlogic Design, Inc., San Diego, CA
Mike Brunoli retains a steadfast focus on the silicon, particularly new-generation CMOS. Analog IP trade is viable but difficult because of the scaling imposed by each new process generation. The newest challenge, for example, is current leakage from devices within 100-nm circuits. The can be repaired with dual oxides, Brunoli suggests, but the circuits won't offer much head room at 1V. Better tools and methodology are required to provide openness and access to data. Without them, even a minor tweak becomes a major roadblock, he says.

Masao Hotta, Director Advanced Analog Technology Division, Hitachi Ltd., Tokyo, Japan
One of Hitachi's keys to success is in cooperation among its design teams. Hitachi has worked on consumer video devices with hundreds of millions of transistors. The transfer of intellectual property is not only feasible, but also necessary — at least among departments in the same company. This has required the coordinated efforts of large engineering teams, as well as use of specialized signoff tools.

Felicia James, VP, IC Technology, Cadence Design Systems, Inc, San Jose, CA.
Felicia James is on a mission: As a mixed-signal IC designer (analog and communications products) in a large IC company, she would be constantly bumping up against the limitations of the EDA tools. These would entail broken design flows, netlists that would not translate from one operation to the next, simulators that would stall, and IC design tools that did not have the capacity to help large designs with the latest design rules. In her current role, she is working to ensure that EDA tools offer thorough support for IP creation and its integration with larger systems-on-chip.

Rudy Koch, Director R&D, Wireless Products, Infineon Technologies AG, Munich Germany
Does EDA understand RF? Dr. Koch worries. If any designer has had criticism of analog IC design tools, their faults are magnified by their application to radio frequency projects. The traditional challenges of simulating transistor-level behavior are complicated by their application to GHz wavelengths. Dr. Koch has been critical of the EDA industry for its attention to large digital circuits and IP blocks, a focus that typically neglects analog and RF. The industry's new focus on signal integrity and substrate coupling issues do not address the voltage and current concerns of analog designers, nor the waveguide geometry issues of those who work in RF.

Roy McGuffin, President and CEO, Antrim Design Systems, Inc., Scotts Valley, CA
As someone involved in the creation and transfer of analog intellectual property, Roy McGuffin looks at the manpower requirement. He says it is difficult to ship a softcoded IP with considerable engineering handholding and support. Selling analog intellectual property has become synonymous with renting out your design time, he jests. There is some help that can be provided by next-generation EDA tools in terms of capturing the physics of the silicon, the behavior of analog circuits and the engineering know-how to integrate analog and digital function blocks.

Andrew J. Moore, Ph.D Design Services Marketing (EDA) TSMC, North America.
Select from prototypes, Moore recommends. From a foundry perspective, the most important guarantor of success in analog semiconductor design is siliconized components; that is, working analog IPs. To that end, TSMC provides dozens of affordable analog prototyping shuttles per year. There is one per month for users of the TSMC 0.18 um MM/RF process, for example. The majority of IP vendors who use these shuttles are analog IP vendors, who have taped out hundreds of components on more than 20 test chips in the last year. From 3rd party vendors and internal teams, there is a selection of siliconized, "off-the-shelf" IPs for analog, including A/D, D/A, PLL, and LVDS components.