Few Electron Devices: Towards Hybrid CMOS-SET Integrated Circuits

Adrian M. Ionescu, Michel J. Declercq
Santanu Mahapatra
Swiss Federal Institute of Technology Lausanne
CH-1015 Lausanne, Switzerland
+41 21 693 3978 / 3974 / 4609
{adrian.ionescu, michel.declercq,
santanu.mahapatra}@epfl.ch

Kaustav Banerjee
Center for Integrated Systems
Stanford University
Stanford, CA 94305, USA
001 650 724 2909
kaustav@cis.stanford.edu

Jacques Gautier
CEA-DRT – LETI/DTS – CEA/GRE
17 avenue des Martyrs
38054 Grenoble cedex 9, France
33 4 38 78 48 56
jgautier@cea.fr

ABSTRACT
In this paper, CMOS evolution and their fundamental and practical limitations are briefly reviewed, and the working principles, performance, and fabrication of *single-electron transistors* (SETs) are addressed in detail. Some of the unique characteristics and functionality of SETs, like unrivalled integration and low power, which are complementary to the sub-20 nm CMOS[1], are demonstrated. Characteristics of two novel SET architectures, namely, *C-SET* and *R-SET*, aimed at logic applications are compared. Finally, it is shown that combination of CMOS and SET in hybrid ICs appears to be attractive in terms of new functionality and performance, together with better integrability for ULSI, especially because of their complementary characteristics. It is envisioned that efforts in terms of compatible fabrication processes, packaging, modeling, electrical characterization, co-design and co-simulation will be needed in the near future to achieve substantial advances in both memory and logic circuit applications based on CMOS-SET hybrid circuits.

Categories and Subject Descriptors
B.7 INTEGRATED CIRCUITS
B.7.1 Types and Design Styles – *Advanced Technologies*

General Terms
Design, Experimentation, Measurement, Performance

Keywords
Nanoelectronics, Single-Electron Transistors, Ultimate CMOS, Hybrid CMOS-SET Circuits, Low power, Inverter, Quantizer.

1. INTRODUCTION

The modern low power electronics originated with the invention of the bipolar transistor in 1947 as an extension of the vacuum tube: the requirements for several watts of tube power and several hundred volts for its anode were replaced by unrivalled tens of mW [1]. Next breakthroughs, related to the first MOS transistor and then, CMOS circuit in 1963, [2], have pushed these limits even further. Is this story going to repeat? The Single-Electron-Transistor (SET), [3, 4], is finally nothing more than somewhat similar evolution or natural extension of the three-terminal MOSFET. Will SET replace it at the nanometer scale? Or will SET have to co-exist with CMOS in the near foreseeable future? This paper attempts to propose some answers and to trace some perspectives *without the ambition of any prophecy*.

1. PUSHING CMOS LIMITS: *The 10 nm WALL*

During the last several years the International Technology Roadmap for Semiconductors (ITRS) has experienced continuous accelerations and revisions, bringing forward the advent of new generation of devices in industrial production (Fig. 1) In its recent 2001 version [5], ITRS projects the introduction of 45 nm-node CMOS devices into production by 2010. This requires transistor gate lengths in the sub-25 nm range operating at extremely low supply voltages (~0.7-0.8V). Scaling MOSFET below 50 nm exacerbates multiple challenges like the control of *short channel effects* (SCE) and the increase of I_{on} (>700μA/μm, at room temperature) while keeping I_{off} acceptably low (1000pA/μm, at room temperature, for low operating power logic). Conventional MOSFET architecture fails to provide such performance for feature sizes below 20 nm due to the simple fact that control of SCE results in severe limitations in the current drive capability.

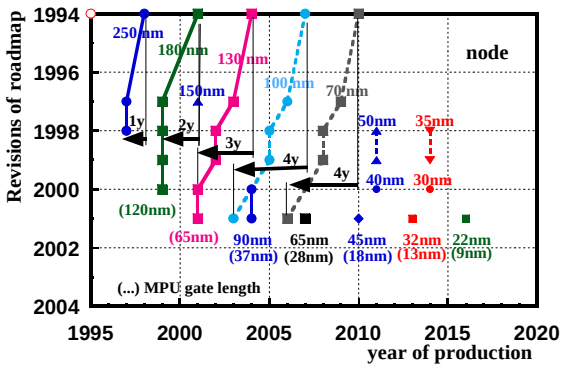


Figure 1. Frequent revisions of the semiconductor roadmap related to fast advancement have resulted in a more-than-4-year shift in terms of projected gate length.

[1] It is worth noting that these comments uniquely refer to present status of reported device principles and architectures.

DAC 2002, June 10-14, 2002, New Orleans, Louisiana, USA.

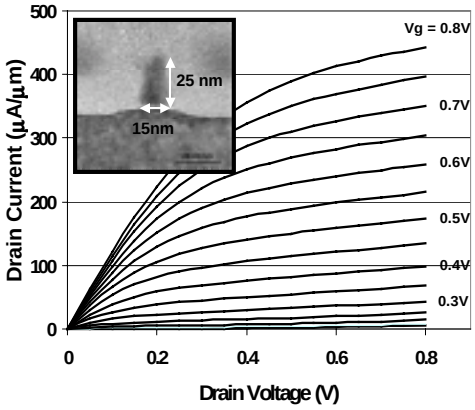


Figure 2. Intel's 15 nm channel length MOSFET. Courtesy of George Sery, Intel Corporation, Santa Clara, USA.

Until now, the microelectronics industry has almost continuously identified innovative methods for aggressive MOSFET scaling to increase performance. Recently, Intel has proposed both a bulk THz MOSFET [6] with gate length of 15 nm (Fig. 2) and a "depleted substrate" architecture that combines some key modifications of the traditional CMOS architecture: *ultra-thin SOI film* instead of bulk silicon, and, *high-k dielectric* instead of the traditional SiO_2 gate dielectric. It is worth noting that even with these solutions, fundamental limitations, expected for the nm dimensions, are not really addressed. Some of the new key fundamental problems [3, 5] of MOSFET-inspired devices for sub-10nm channel length are expected to be: (i) *electrostatic limits*, (ii*) source-to-drain tunnelling*, (iii) *carrier mobility* (iv) *process variations, and* v) *static leakage*. Simultaneously, and perhaps even more critical is the *power scaling concern*. It appears that *emerging device architectures* (outlined in the next Section) can offer CMOS more lifetime and provide solutions to continue scaling into the nanometer range, or at least until the *10 nm wall* is reached.

2. EMERGING DEVICE ARCHITECTURES

2.1 Double/Multi-Gate and FinFETs

Double/multi-gate MOSFETs [7] or FinFET [8] (Fig. 3), with ultrathin Si-film, are expected to constitute mainstream nanometer CMOS technology. Their key advantages, [9], are *excellent scalability* due to superior immunity against SCE effects, near-ideal subthreshold slope, high near-ballistic drive-current and transconductance, and low subthreshold intrinsic capacitance. The design of optimal multi-gate MOSFET requires new insights into the underlying physics and especially the quantum mechanics of the carriers confined in sub-10 nm films, [9].

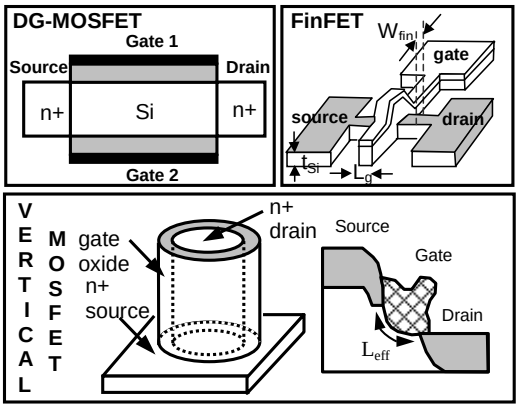


Figure 3. Emerging MOSFET device architectures.

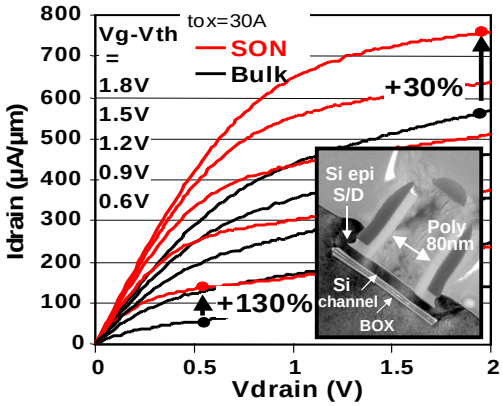


Figure 4. ST's 80 nm Silicon-On-Nothing (SON) transistor. Courtesy of Th. Skotnicki, ST Microelectronics, Crolles, France.

FinFET (Fig. 3) is a successful alternative inspired by DG-MOSFET that uses e-beam lithography for fin patterning. Recent realizations [8] with 20 nm gate length, less than 10 nm Si-film and 2.1 nm gate oxide, have shown (for W_{fin}=40 nm) NMOS and PMOS drive currents of 500 µA/µm and 380 µA/µm, respectively, which with *conventional* definition of double-gate means 1000 µA/µm and 760 µA/µm, respectively. The associated FinFET I_{off} is less than 1nA/mm.

2.2 Silicon-On-Nothing (SON)

Silicon-on-nothing (SON) [10, 11] is an innovative process that *provides "super-SOI" using bulk-silicon*, with a quasi-total suppression of SCE and DIBL and excellent electrical performances due to an extremely thin silicon (5-20 nm) and buried dielectric (10-30 nm). In sharp contrast to any SOI technology (SIMOX, BESOI, Smart Cut, ELTRAN, ELO, etc.), SON's nano-scale silicon film and buried insulator are defined by epitaxy on a bulk substrate. The buried oxide is not continuous (contrary to conventional SOI) and is located only under the gate and the spacers (Fig. 4). Compared to SOI, the advantages of such solutions are reduced series resistance and easier silicidation. 80 nm channel length SON NMOS (Fig. 4), with significant gain compared to similar devices made on pure bulk silicon (drain current of 750 µm/µm and 25 nA/µm I_{off} with 150 mV DIBL), have been recently demonstrated, [11].

2.3 Vertical MOSFET

The vertical MOSFET configuration [12, 13] provides other new device options for higher levels of functional integration. Its vertical channel is *lithography quasi-independent*, using vertically formed pillars (Fig. 3). Arbitrary doping profiles, heterojunctions and multiple devices (epitaxially grown) can also be incorporated into the vertical channel structure, [12].

2.4 Ballistic MOSFET

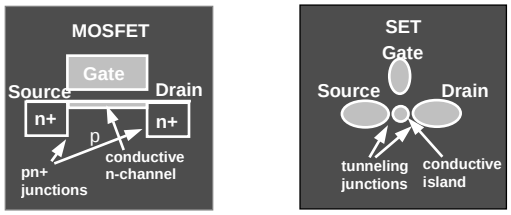
For dimensions less than 10 nm, CMOS-inspired architectures enter ballistic transport, which, hopefully, is advantageous. *Channel length less than carrier mean free path* defines the basis of ballistic transport, where, with no collisions, carrier mobility does not make any sense and significant current increase is experienced. Low doped thin device bodies are suitable for ballistic MOSFET (also eliminating parameter fluctuations related to discrete/random doping). New conduction mechanisms, [14, 15]: *thermo-ionic emission* and *quantum tunneling* have to be considered. However, the notion that reduction of L allows the voltage/power to be scaled does no longer holds for ballistic devices because the current is limited by electron supply at source.

With all these new emerging devices, there are, of course, many exciting opportunities and developments; however, they do not include any disruptive modification of MOSFET basic principle for which real fundamental limitations arrive below 10 nm gate length.

3. Single-Electron Transistors: *A Not So Different World*?

3.1 Principles: C-SET versus R-SET

The history of *few-electron electronics* [4] probably started in 1951 when C. Gorter explained for the first time the Coulomb blockade phenomenon. Only much later, in 1985, D. Averin and K. Likharev [16, 17] formulated the 'orthodox theory' of single-electron tunneling that describes the charge transport under the influence of Coulomb blockade and allows the exploitation of Single-Electron Transistor (SET). The *capacitive* C-SET architecture (Fig. 5) is similar to the MOSFET; it has a source (S), a drain (D) and a gate (G), the main difference being that the MOS channel is replaced by an ultra-small *conductive island* separated by *two tunnel barriers* from source and drain. The operation of SET exploits the discreteness of the number of electrons in their conductive island, which is in contrast with the MOSFET where, because of the highly transparent boundaries between S/D and the inversion channel, single electron charging is not experienced.



(a) (b)

Figure 5. Schematic of: (a) MOSFET and (b) C-SET.

Thus, proper SET operation needs *opaque barriers* in order to localize electrons in the quantum dot (or island). Application of the energy uncertainty principle results in a tunnel resistance R_T that should satisfy:

$$R_T > h/e^2 = R_Q \cong 26k\Omega \qquad (1)$$

With condition (1) satisfied, the quantum mechanical uncertainty of electron location is covered up. In order to have full functionality, the charging energy of the island must be larger than the thermal fluctuations:

$$E_C = e^2/2C_\Sigma > k_B T \qquad (2)$$

This condition can be fulfilled either by working with low temperature, T, and/or with very small island to ground capacitance, C_Σ. SET operation can now be briefly explained: at low V_{DS} there is no drain current (the current suppression being called *Coulomb blockade*, CB) since any tunneling would lead to an increase in the total energy and at low enough temperatures tunneling is rather low (Fig. 6). There are two ways to overcome CB: one is to increase the V_{DS} voltage up to a threshold voltage, V_T, where the current starts to rise with V_{DS}. The second is, of course, to increase the temperature (Figs. 6, 7). A key property of SET is that V_T is a periodic function of V_{GS} (Figs. 7, 8) providing the specific SET signature called Coulomb oscillations. They relate to the fact that at some external biasing:

$$Q_0 = C_G V_G = e(n + 1/2) \qquad (3)$$

one electron can tunnel from source to the island and then to the drain even at negligible V_{DS}. It appears that the SET transconductance, $g_m=dI_D/dV_{GS}$, can have *both positive and negative values* (Fig. 8), depending uniquely on the gate voltage, which is a key difference with respect to MOSFETs. This is a real advantage if one aims to mirror CMOS circuit architectures in SET, because the *equivalent SET circuits would require the use of a unique type of device*. On the other hand, the drawback of SET lies on its low voltage gain that is limited by the capacitance ratio C_G/C_Σ (lower than few units at room temperature, [3, 4].

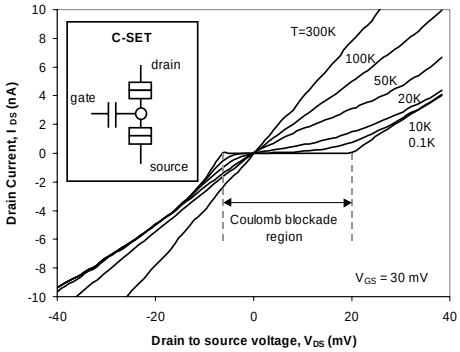


Figure 6. I_{DS}-V_{DS} characteristics of C-SET for various temperatures, T, highlighting Coulomb blockade.

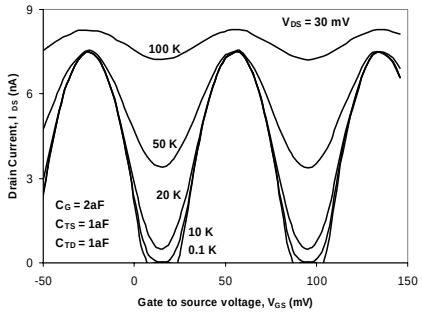


Figure 7. SET typical oscillations of I_{DS} versus V_{GS}, (periodic peaks and valleys) at various operating temperatures, T.

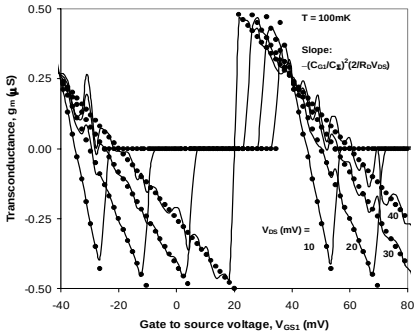


Figure 8. C-SET transconductance, g_m, vs. V_{GS} with V_{DS} as parameter at T=100mK: simulated with SIMON (solid line) and with our recent analytical model, MIB [24] (symbols).

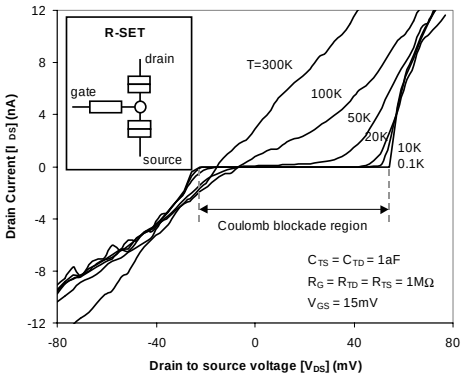


Figure 9. R-SET I_{DS}-V_{DS} simulated [18] characteristics for various temperatures, T, highlighting Coulomb blockade.

Note that SET principle can apply not only to well known C-SET (with capacitive gate), but also to R-SET (Fig. 9) for which the gate architecture is resistive. As shown by Korotkov [18] and demonstrated by Fig. 10, Coulomb blockade can be successfully experienced by R-SET, and even if its I_D-V_{GS} characteristics are no longer periodic, its usefulness for logic applications exists.

3.1.1 Dimensions for Room Temperature Operation

SET operation at room temperature is conditioned by the possibility to provide a very small C_Σ capacitance associated with the quantum dot. The plot reported in Fig. 10 exploits Kirihara's criteria, [19]: $T_{max}<e^2/(40kC_\Sigma)$, to deduce the maximum temperature at which SET can properly operate under Coulomb blockade. It is clearly shown that, for room temperature operation (300 K), SET needs total capacitance of less than around 0.2aF and an island radius less than 0.5nm. These are real challenges for SET device and circuit technology that are briefly described under §3.1.4.

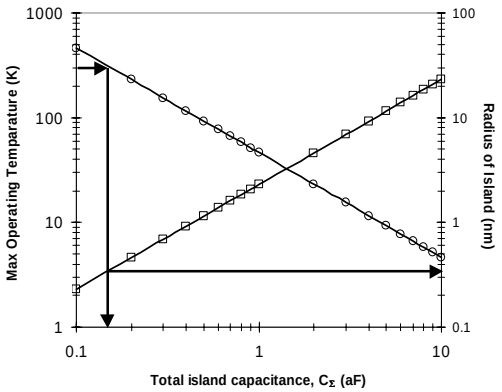


Figure 10. Maximum C-SET operating temperature, T_{max}, (with Kirihara's criteria [19]) vs. total island capacitance, C_Σ.

3.1.2 Background Charge Sensitivity

One of the drawbacks usually mentioned for C-SET is its high sensitivity to background charge that could jeopardize its proper functionality in digital circuits [3]. Materials quasi-free of impurities, R-SET-inspired device architectures (insensitive to background charge because of the resistive-gate coupled to the SET island), variable C-SET or compensation by refresh adapted cycles [4], *at device level*, and neural network architectures that cope with intrinsic errors*, at circuit level*, are some possible answers to this question.

3.1.3 SET Simulation and Modeling

It is clear that a deeper comprehension of SET underlying physics and its high potential for new functionality could help the take off of this new device. Simulation of SET devices and circuits has been proposed via (I) *Monte Carlo* (MC) simulators like SIMON [20], MOSES [21] and CAMSET [19], (II) *macro-modeling* [22] and (III) *analytical models* [23, 24]. More advanced analytical models and related electrical characterization are eagerly needed. Recently, the MIB has been proposed [24], a quasi-analytical model that enables SET co-simulation with CMOS up to a temperature $T=e^2/(40kC_\Sigma)$. MIB is founded on the "orthodox" theory of single electron tunneling and is able to model both symmetric and asymmetric SETs, with single- or double-gate. In MIB both SET drain current and (trans)conductance are analytically modeled via two separated current components: the *harmonically-connected* S/D tunneling currents (considered independent of temperature) and the *thermal* current. For accurate simulation, MIB model requires that interconnect capacitance be much larger than C_Σ and $|V_{DS}|<e/C_\Sigma$.

3.1.4 SET co-Fabrication with CMOS

First experimental SETs were fabricated by Fulton and Dolan [4], and, Kuzmin and Likharev, [17]. Various solutions have since been developed and reported [4], such as: shadow evaporation (Al/Al_2O_3 process), nano-imprint, use of STM/AFT tips for nano-oxidation, deposition of sub-10 nm thick films with nano-grains and self-assembly techniques. One key successful technology that *enables SET and CMOS electronics to co-exist* with encouraging performance is PADOX [25] (or its evolution into V-PADOX [25]). It exploits the pattern dependent (because of gradients of mechanical stress) oxidation of silicon in order to provide sub-lithographic dimensions (<10 nm) of SET islands in simple or twin architectures. Fabrication of SETs for both logic and memory with undulated ultra-thin (<5 nm) polysilicon film on SOI is another successful technique [26] (Fig. 11). Recently, LETI [27] has shown a MOS-inspired alternative to fabricate SETs, called MOS-SET. It exploits Coulomb oscillations (Fig. 12) due to dopant fluctuations in ultra-short MOSFET channel and/or S/D potential barriers (provided by adapted doping in source and drain regions) that act as opaque tunneling junctions.

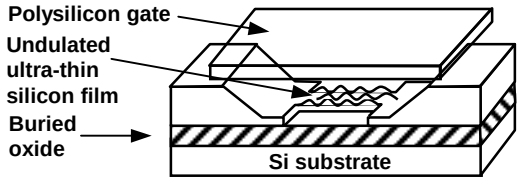


Figure 11. SOI-SET with undulated ultra-thin SOI film [26].

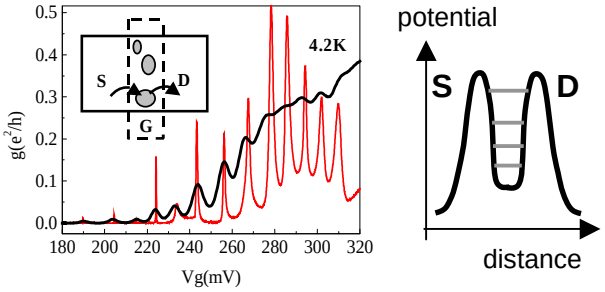


Figure 12. Typical conductance oscillations observed in LETI's [27] MOS-SET, revealing Coulomb blockade.

3.2 **Digital SET:** *To Mimic or Not to Mimic CMOS?*

One key question for SET logic circuit applications is about the efficiency of a CMOS-like circuit approach. Many successful logic applications have been reported by mimicking CMOS, but real competing performance with CMOS still remains to be demonstrated. A different, eccentric yet exciting, alternative is the *wireless* SET logic [28] where *external* electrical fields are used for both operation and power supply (thus, *no interconnect wires are required*); however, such a realization has not yet been experimentally verified.

3.2.1 C-SET and R-SET Few-Electron Inverters

In the following, performances of the C-SET inverter and, *for the first time*, R-SET inverter are briefly analyzed. Fig. 13 depicts typical V_{out}-V_{in} of realistic C-SET inverter as a function of temperature, *T*. With similar parameters and high-resistive gate (R_G=10 MΩ), we report a fully functional R-SET inverter (Fig. 14). We demonstrate here that C-and R-SET inverter performances are rather different. Figs. 15a and 15b depict the inverter gain, dV_{out}/dV_{in},, which highlights the first key difference: R-SET inverter has a much higher gain than C-SET, but degrades much faster with temperature. Noise margins (defined using CMOS criteria, $|dV_{out}/dV_{in}|=1$) are calculated and plotted together with thermal voltage, kT/q, in order to find out the domain for which real functionality can be expected (negligible thermal fluctuations). A

remarkable feature of C-SET inverter is that the point at which $dV_{out}/dV_{in}=-1$, is insensitive to the temperature (Fig. 15). R-SET has better noise margins at low temperature, but their degradation with T is much faster than for C-SET. Fig. 16 demonstrates that with C_Σ in the range of aF, inverter functionality is expected up to few tens of K. The crucial advantage of SET is its low power consumption (on the orders of 10^{-10}-10^{-8}W/gate) supported by manipulation of single electrons with low voltages/currents (mV/nA); C-SET consumes even less power than R-SET. SET logic circuits can be source of surprising behavior: Fig. 14 demonstrates that SET inverter currents behave totally different than for CMOS: their "transition" region has negligible current/consumption (degrading with T). It follows that dynamic power of SETs is quasi-negligible and their ultra-low power consumption is mainly static, in contrast with ideal CMOS.

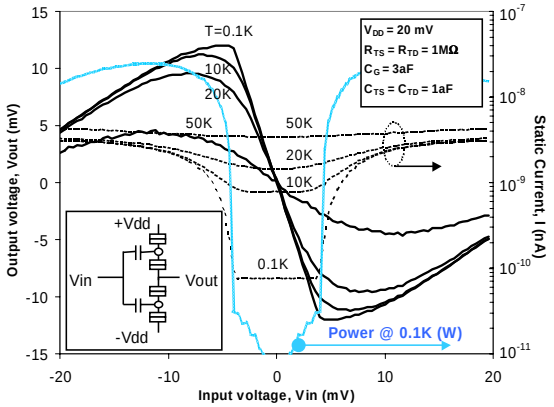


Figure 13. C-SET inverter static characteristic, V_{out} vs. V_{in}.

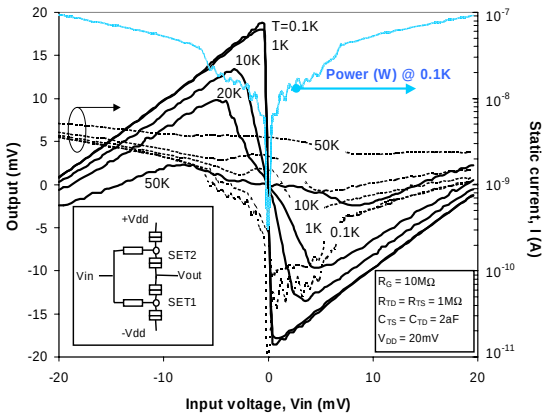


Figure 14. R-SET inverter static characteristic, V_{out} vs.V_{in}.

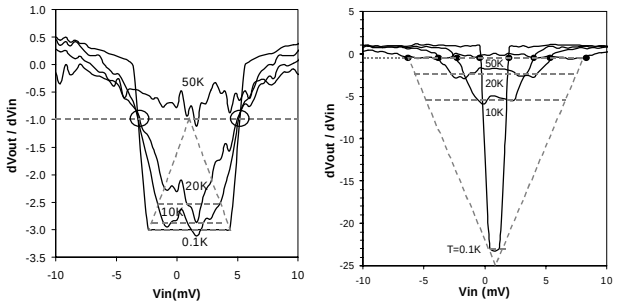


Figure 15. dV_{out}/dV_{in} of C-SET and R-SET at various T.

In Fig. 17a the transient characteristics of a C-SET inverter are reported. SET performance at high frequency is not limited by their intrinsic speed (electron tunneling is a fast process, with time constant of the orders of 10^{-15}s), but by the limited ability to drive high capacitance loads, C_L (Fig. 17b). Based on rather surprising observation that, in terms of current density, SET is not inferior to CMOS (with a size of 1 nm, the SET current density can be as high as a few of 100 μA/μm), we demonstrate in Fig. 17b that with (only three) parallel connected SET-inverters to drive C_L, the delay can be improved by a factor of 2 to 5 (depending on C_L). This parallel driving architecture requires practically ideal clock-skew that can be obtained with a symmetrical design of the interconnect-to-input gates. Its integration with a VPADOX-like process could result in quasi-identical parallel-connected inverters with smaller size than CMOS.

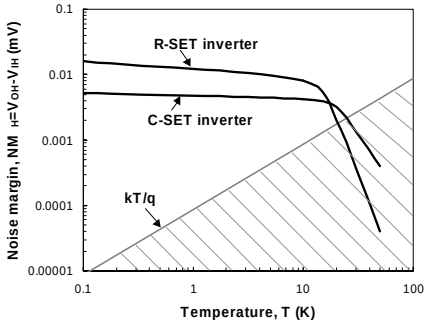
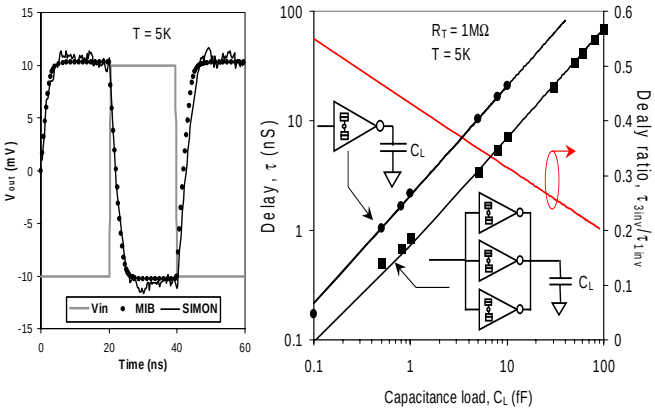


Figure 16. C- and R-SET inverter noise margins, NM_H, vs. T.



(a) (b)

Figure 17. (a) C-SET inverter transient and (b) Delay, τ, vs. capacitance load, C_L, with 1 and 3-parallel driving inverters.

3.2.2 Single Electron Devices for Ultimate Memory

Ultimate memory with single/few electron devices reflects the possibility *to store one bit of information by the trapping/de-trapping of one single electron*. Their advantages are clear: better than 10^{11}-10^{12} bits/cm^2 storage density with ultra-low power (less than 10^{-9} W/gate). With the few reported successful realizations, it turns out that single electron memories are very close to a major breakthrough in this field. Yano's [29] memory with nanogranular thin polysilicon film, Tiwari's [30] memory with nanocrystals included in MOSFET's gate oxide, and some other SET/FET hybrid few-electron memory architectures have shown reliable operation at room temperature with outstanding integration/power. For the mid-term, prior to ultimate single-electron memory, some other new memory concepts have been proposed, like the *non-volatile random access memory* (NOVORAM) [31] that exploits crested barriers and, with the use of SOI technology, has excellent potential for nanometer scaling.

4. **Hybrid CMOS-SET Architectures:** *Illusion or Useful Compromise?*

We think it is now time for the "old" extraordinary, high-performance CMOS and the "novel", still-promising SET, to start exploring a common, joint evolution. Recent reports demonstrate some new, unique functionality and high performance that cannot be achieved by any other alternative than combining CMOS and SET in hybrid CMOS/SET IC architectures (Fig. 18). Uchida et al., recently reported a future foreseeable hybrid SET/CMOS ULSI (Fig. 19) [26], which exploits the particular advantages of SETs and CMOS and, when possible uses CMOS to compensate for SET drawbacks. Nonvolatile single-electron memory (NVM) circuits for *programmable SET/FET logic* [26, 32], *multiple-valued* logic/SRAM [33, 34], new *quantizer* circuits [34, 35] and other applications that exploit the negative-resistance SET blocks [4] have also been proposed. It appears that a *triple effort* is required for the success of hybrid CMOS/SET: (I) first, is on the development of common technological platform, (II) second, is on enabling advanced SET/CMOS co-simulation and design, and, (III) third, on innovative development/demonstration of new functionality of hybrid IC architectures tolerant to background charge effects (and - why not? - with new types of logic).

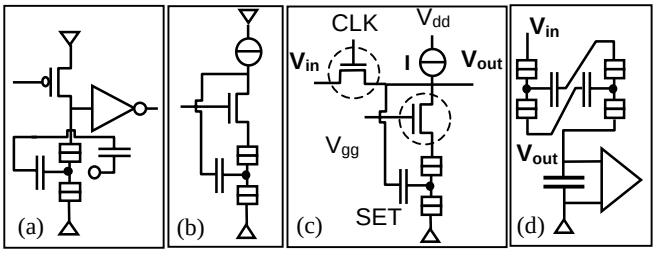


Figure 18. Hybrid SET/CMOS ICs: (a) NVM circuit for programmable logic (undulated-film SET) [26], (b) multiple-valued SRAM cell (PADOX) [32], and (c, d) quantizers [34, 35].

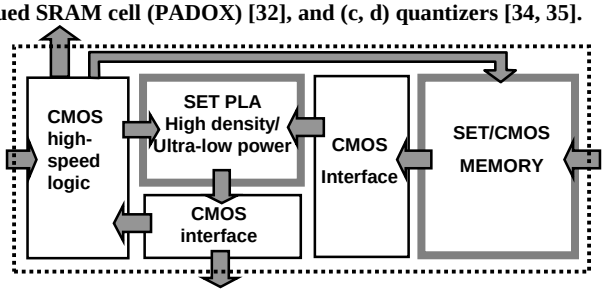


Figure 19. Hybrid SET/CMOS ULSI architecture, after [26].

5. CONCLUSIONS

Tremendous progress in microelectronics has pushed the MOSFET dimension towards the 10 nm limit, which is expected to impact basic working principles of MOSFETs. In the near future it is then probable that CMOS will need to share its domination on modern ICs with fundamentally new devices that use a few electrons, like SETs. It appears that CMOS and SETs are rather complementary: SET is the *champion of low-power consumption* and of new functionality while CMOS advantages like high-speed, driving, voltage gain and input impedance can compensate exactly for SET's intrinsic drawbacks. Moreover, *unrivalled integration with high performance and new functionality* are expected for *hybrid CMOS-SET architectures*.

6. REFERENCES

[1] J. D. Meindl, "A history of low power electronics: how it began and where it's headed", *Proc. of Int. Symp. Low Power El. and Design*, pp. 149 -151, 1997.

[2] J. D. Meindl, "Low power microelectronics: Retrospect and prospect", *Proceedings of IEEE*, vol. 83, no. 4, pp. 619–635, 1995.

[3] K. Likharev, "Sub-20nm Electron Devices", Advanced Semiconductor and Organic Nano-Techniques", Ed. H. Morkoc, *Academic Press*, 2002.

[4] C. Wasshuber, "Computational Single-Electronics", *Springer Ver.*, Wien, 2001.

[5] The International Technology Roadmap for Semiconductors (ITRS), 2001 Eds.

[6] Private communications, George Sery, Intel Corporation.

[7] Y. Taur et al., "CMOS scaling into the nanometer regime", *Proceedings of IEEE*, vol. 85, no. 4, pp. 486-504, 1997.

[8] Y. Choi et al., "Sub-20nm FinFET Technologies', *Technical Digest IEDM*, pp. 421-424, 2001.

[9] L. Ge and J.G. Fossum, "Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs", *IEEE Trans. on El. Dev.*, vol. 49, no. 2, pp. 287-294, 2002.

[10] M. Jurczak et al., "Silicon-On-Nothing (SON) - an innovative process for adv. CMOS", *IEEE Trans. on El. Dev.*, vol. 47, no. 11, pp. 2179-2187, 2000.

[11] S. Monfray et al., "First SON (Silicon-On-Nothing) MOSFETs with perfect morphology and high electrical performance", *IEDM Technical Digest*, pp. 645-648, 2001.

[12] J.D. Plummer, "Silicon MOSFETs (conventional and non-traditional) at the scaling limit", *Proc. of Device Research Conference 2000*, pp. 3-7, 2000.

[13] T. Schultz et al., "Short-channel vertical sidewall MOSFETs", *IEEE Trans. on El. Dev.*, vol. 48, no. 8, pp. 1783-1788, 2001.

[14] M. Lundstrom and Z. Ren, "Essential Physics of Carrier Transport in Nanoscale MOSFETs", *IEEE Trans. on El. Dev.*, vol. 49, no. 1, pp. 133-141, 2002.

[15] D. Munteanu, J.L. Autran, "Two-dimensional Modeling of Quantum Ballistic Transport in Ultimate Double-Gate SOI Devices". *Proc. of ULIS 2002*, Munich, Germany, pp. 119-122, 2002.

[16] D. Averin and K. Likharev, "Single electronics: a correlated transfer of single electrons and Copper pairs in systems of small tunnel junctions", in *Mesoscopic phenomena in solids*, pp. 173-271, 1991.

[17] K.K. Likharev, "Single-electron devices and their applications", *Proceedings of IEEE*, vol. 87, Issue 4, pp. 606 -632, 1999.

[18] A.N. Korotkov, "Single-electron transistor controlled with a RC circuit", *Phys. Rev. B*, vol. 49, pp. 16518-16522, 1994.

[19] M. Kirihara, N. Kuwamura, K. Taniguchi, and C. Hamaguchi, "Monte Carlo study of single-electronic devices," in *Ext. Abst. Int. Conf. on Solid State Devices and Materials*, Yokohama, Japan, 1994, pp. 328–330.

[20] C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON - A Simulator for Single-Electron Tunnel Devices and Circuits", *IEEE Transactions on Computer Aided Design of IC and Systems*, vol. 16, no. 9, pp. 937-944, 1997.

[21] R. H. Chen, A. N. Korotkov, and K. K. Likharev, "Single-electron transistor logic", *Appl. Phys. Lett.*, vol. 68, pp. 1954–1956, 1996.

[22] Y. S. Yu, S. W. Hwang, and D. Ahn, "Macromodeling of single electron transistors for efficient circuit simulation", *IEEE Trans. on El. Dev.*, vol. 46, No. 8, pp 1667-1671, 1999.

[23] K. Uchida et al.,"Analytical single-electron transistor (SET) model for design and analysis of realistic SET circuits", *Jpn. J. Appl. Phys.*, vol. 39, Part 1, No. 4B, pp. 2321-2324, 2000.

[24] S. Mahapatra, A.M. Ionescu and K. Banerjee, "A Quasi-Analytical SET Model for Few Electron Circuit Simulation", *IEEE El. Dev. Lett.*, to appear, 2002.

[25] Y. Takahashi et al., "Silicon single-electron devices and their applications", *Proc. of IEEE International 2000 Symposium on ISMVL*, pp. 411 -420, 2000.

[26] K. Uchida et al., "Programmable single-electron transistor logic for low-power intelligent Si LSI", *Digest of ISSCC 2002*, pp. 206-207, 2002.

[27] M. Sanquer et al., "Coulomb blockade in low-mobility nanometer size Si MOSFET's", *Phys.Rev.*, B 61, pp.7249-7252, 2000.

[28] A.N. Korotkov, "Wireless single-electron logic by alternating electric field", *Appl. Phys. Lett.*, vol. 67, pp. 2412-2414, 1995.

[29] K. Yano et al., "Single-electron memory for giga-to-terra bit storage", *Proceedings IEEE*, vol. 87, pp. 633-651, 1999.

[30] S. Tiwari et al., "A silicon nanocrystals based memory", *Appl. Phys. Lett.*, vol. 68, pp. 1377-1379, 1996.

[31] K.K. Likharev, "Riding the crest of a new wave in memory [NOVORAM]", *IEEE Circuits and Devices Magazine*, vol. 16, pp. 16-21, 2000.

[32] K. Uchida et al., "Room operation of multifunctional single-electron transistor logic", *Tech. Digest IEDM*, pp.863-865, 200.

[33] H. Inokawa, A. Fujiwara and Y. Takahashi, "A multiple-valued single-electron SRAM by the PADOX process", *Proc. 6th Int. Conf. on Solid-State and IC Technology*, pp.205 -208, 2001.

[34] H. Inokawa, A. Fujiwara and Y. Takahashi, "A multiple-valued logic with merged Single-Electron and MOS Transistors", *Tech. Digest IEDM*, pp. 147-150, 2001

[35] S. Mahapatra, A. M. Ionescu, K. Banerjee and M. Declercq, "A SET Quantizer Circuit Aiming at Digital Comm. System", *ISCAS 2002,* (to appear), 2002.