Technological Innovations to Advance Scalability and Interconnects in Bulk and SOI

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Introduction

With technology scaling rapidly, there is increased need for improved performance. While improved performance can be achieved with lower threshold voltages, leakage will be a major issue at technologies below 0.1µm. Interconnect scaling is not expected to keep up with component scaling, resulting in higher capacitance losses and challenges in signal routing. We consider how scaling will impact design for low power and high performance applications. SOI may be a solution for some issues like SER due to the presence of buried oxide. Performance can be enhanced by SOI technology due to the absence of junction capacitance (figure 1). The combination of short gate length technologies and PD-SOI can mitigate performance degradation due to interconnect capacitances and leakage.

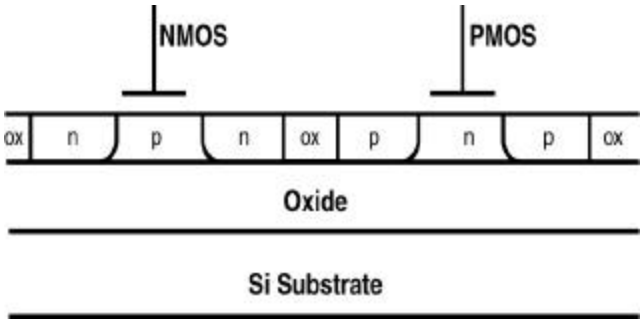

Figure 1: Cross section of SOI, showing CMOS sources and drains surrounded by thick oxide.

Scaling transistor size lowers capacitance, and permits shorter routing between logic blocks. This reduces interconnect capacitance and resistance. However interconnects does not scale at the same rate as components, resulting in higher capacitance losses and challenges in signal routing. This non-linear scaling particularly impacts on designs for low power and high performance.

The Role of SOI

Silicon on Insulator is being used for high performance applications such as microprocessors, where a performance boost can be achieved without significant lithography changes [1]. The use of SOI can lead to die area reduction of between about 5 and 30 percent, due to reduced isolation (improved packing density) requirements of SOI, and the ability to better position critical path components in SOI.

Transistor Doping Profiles

The sources and drains of SOI devices have shallow junction depths compared to junctions in bulk material. The use of SOI results in a well-defined source/drain, which is relatively easy to maintain with technology scaling. This is not the case with bulk material, where junction scaling becomes more difficult as geometries reduce. Reduction in volume of the SOI source/drain does, however, tend to lead to higher resistance transistors than their bulk counterparts due to their shallower diffusions

When high velocity carriers flow from source to drain, impact ionization induced electron-hole pairs are generated. The threshold that impact ionization occurs depends on many device characteristics, including gate oxide thickness, doping profile and supply voltage. Impact ionization causes hole charging of the body, which reduces with gate length scaling. However, while impact ionization reduces, gate leakage increases due to the thinner gate oxides, which are required for the shorter channel lengths. One solution to reduce gate leakage is to use high dielectric constant (high-K) gate dielectrics, though this has limitations. Parasitic bipolars can be tuned to minimize device gain. This is achieved through a combination of source doping and channel doping to reduce emitter efficiency and gain. There is general agreement that SOI provides an improvement in terms of operating frequency for digital applications over bulk at technologies down to gate lengths of between 50 and 100nm.

SOI vs BULK

Due to the dynamic threshold voltage effect, higher drive currents and reduced junction capacitance, SOI CMOS circuits have higher performance than CMOS on bulk silicon. SOI junction capacitance can be scaled more easily than bulk as supply voltage reduces. The reduced junction capacitance of SOI CMOS translates into superior SRAM performance, which permits faster microprocessors. Reduced soft error rate (SER) has been observed in SOI memory circuits, which is an advantage in SRAM applications. To maintain the same transistor

off state leakage current, SOI MOSFETs are typically designed with higher threshold voltages than bulk. Higher threshold voltage reduces available current drive diminishing the performance leverage especially at low supply voltages. Noise and latchup are minimized through reduced substrate coupling. Silicon resistors have improved linearity with respect to absolute voltage in many cases, since they do not form reverse biased diodes to substrate (as resistor voltage increases the reverse biased diode depletion region increases in bulk material, resulting in higher resistances for the same resistor layout). Inductor Q can be enhanced through the use of very high resistivity substrates.

Interconnect

Interconnect can be a substantial percentage of the capacitance loading in microprocessors. Power related to interconnect may account for over 40% of the total chip power. The capacitance from interconnect to substrate is lower in SOI than bulk, and interconnect length can be reduced by optimal path layout. At chip level additional gains over the circuit level advantages are limited to improvements achieved from interconnect. Memory circuitry therefore has little additional advantage at chip level, but for logic, significant reduction in interconnect can be obtained. Use of high resistivity substrates, not available to many bulk processes also improves performance, especially in high frequency applications.

When designing for low power, microprocessor performance is limited by system constraints. In computers these constraints include energy conservation regulations and cooling limitations. Despite power limitations, notebook microprocessors must still approach desktop standards. Microprocessor performance therefore must be maximized for given power constraints. The development of low power technologies like SOI and scaling of device features sizes is important in reaching low power goals.

Stacked SOI

SOI layers can be stacked (3D SOI), allowing for an increase in gate density (figure 2) [2 -4]. Enhanced packing potential and reduced interconnect from stacked SOI layers have resulted in 3D SOI being a source of intense study. Multiple layers of SOI using a layer transfer process which can be achieved in a variety of ways.

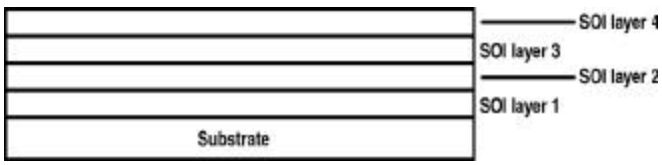

Figure 2: Stacked SOI cross section

Applications include advanced process integration, optical filters, micro-machining and sensors integrated with logic or DSP modules. The additional problems with this approach are even more severe thermal dissipation difficulties, matching between layers, the potential for electromagnetic or capacitive coupling between layers, and the higher probability of bond pad limited designs.

Soft Error Rate (SER) Effects

One benefit recognized early in the development of SOI has been reduction in memory soft-error rate resulting from cosmic rays and background radiation. SER is a greater concern in small area memory cells, where there is less charge to disrupt. With the sizes of all types of memory cells reducing at a rate close to that of process feature size reductions, any advantage that can be gained from reduced SER is significant. In addition, soft error immunity (radiation hardness) of SOI devices is important for high data rate network servers and global data transfer links. Alpha particles from radioactive elements in packaging are known to induce soft errors and impose design constraints in six-transistor planar SRAM cells. Due to the presence of buried oxide, it is more difficult for the alpha particles to get injected into the channel. The reduced cell size and storage node capacitance improves cell performance due to reduced parasitics.

In bulk CMOS, $\propto$-generated charges are collected mainly by the funneling effect, when particles collide with the drain diffusion layer. This is not significant in SOI MOSFET's due to presence of buried oxide. Charge collection can only occur in SOI MOSFET's when an $\propto$-particle interacts with the channel region. The amount of $\propto$-generated charges in SOI MOSFET is less than bulk. The total charge collected at the cell storage node is significantly higher than $\propto$-generated charges due to the parasitic bipolar effect. Alpha induced bipolar current flows over extended time periods.

References

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