

# Analysis and Design of Low-Phase-Noise Ring Oscillators

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## ABSTRACT

This paper presents a framework for CMOS ring oscillator phase noise analysis for given power consumption specifications. This model considers both linear and nonlinear operations. It indicates that fast rail-to-rail switching has to be achieved for low phase noise and that the up-conversion of low-frequency noise from the current bias/control circuit can be significant. Our phase noise model is validated via simulation and measurement results. We also present a coupled-ring oscillator whose phase noise is  $-114dBc/Hz$  at a  $600kHz$  offset from the  $960MHz$  carrier frequency.

## 1. INTRODUCTION

Voltage-controlled oscillators (VCO) are important building blocks in phase-locked loops (PLLs). The random fluctuations in the output phase of the oscillator, in terms of jitter or phase noise, are extremely undesirable in most applications. The design of CMOS VCOs with low phase noise is an active research topic [1, 2, 3]. Due to their ease of implementation and large tuning range, CMOS ring oscillators are attractive candidates for system-on-a-chip designs. However, their phase noise performance is usually worse than those with high-Q resonant elements.

There is direct trade-off between the power consumption and the oscillator phase noise performance. It is desirable to minimize the phase noise for a given power consumption budget. In this paper we first present a modified linear phase noise model for ring oscillators. Modifications include the non-linear operation caused by voltage clipping. Next we extend this model to include the up-conversion of the low-frequency noise from the bias/tail devices. Finally, we validate our model via simulations and measurement results.

## 2. PHASE NOISE ANALYSIS

In this section, we will derive the relation between the phase noise and the internal signal swing from a simplified model.

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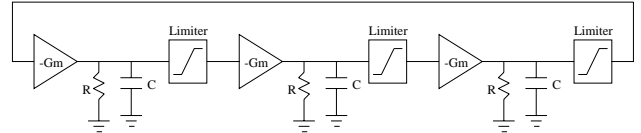


Figure 1: Modified linear model for a 3-stage ring VCO

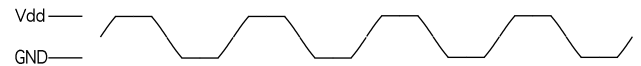


Figure 2: Sinusoidal waveform clipped by power supplies

We show that, for a given power consumption specification, in order to achieve phase noise comparable to LC-tank oscillators, sharp rail-to-rail voltage swings are needed, i.e., devices have to be switched on and off completely.

Figure 1 shows a simplified model for a 3-stage ring oscillator. The system is linear as long as the internal voltages are not clipped by the limiters. For this condition the single-sideband (SSB) phase noise can be shown to be represented by eqn.(1) [2], where  $k$  is the Boltzmann's constant and  $T$  is the absolute temperature. The excess noise factor  $F$  accounts for the total noise from the resistor  $R$  and the active device ( $-G_m$ ) [4].  $V_{pp}$  represents the peak-to-peak signal voltage. Here, we have only considered thermal noise.

$$L\{\Delta\omega\} = \frac{64FkTR}{9V_{pp}^2} \left( \frac{\omega_0}{\Delta\omega} \right)^2 \quad (1)$$

In reality, the waveform is bounded by the power supplies for large amplitudes. Let us assume that the sinusoidal waveform is symmetrically clipped as shown in Figure 2.

Its Impulse Sensitivity Function (ISF or  $\Gamma$ ) [3] can be approximated by

$$\Gamma(\omega t) \approx \frac{dv(\omega t)/d(\omega t)}{|dv(\omega t)/d(\omega t)|_{max}^2} = \begin{cases} \frac{2}{V_{pp}} \cos(\omega t) & (for \frac{V_{pp}}{2} \sin(\omega t) < \frac{V_{dd}}{2}) \\ 0 & (for \frac{V_{pp}}{2} \sin(\omega t) \geq \frac{V_{dd}}{2}) \end{cases}$$

Hence eqn.(1) has to be modified for  $V_{pp} > V_{dd}$  as shown in

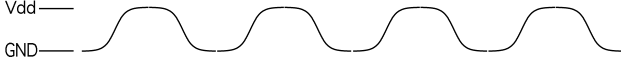


Figure 3: Waveform with soft slipping

eqn.(2).

$$L\{\Delta\omega\} = \frac{128FkTR}{9\pi V_{pp}^2} \left[ \arcsin\left(\frac{V_{dd}}{V_{pp}}\right) + \frac{V_{dd}}{V_{pp}} \sqrt{1 - \frac{V_{dd}^2}{V_{pp}^2}} \right] \left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$$\approx \frac{256FkTRV_{dd}}{9\pi V_{pp}^3} \left(\frac{\omega_0}{\Delta\omega}\right)^2 \quad (\text{for } V_{pp} \gg V_{dd}) \quad (2)$$

We use  $V_{pp}$  in eqn.(2) to represent the peak-to-peak voltage of the sinusoidal waveform as if there was no clipping. Eqns.(1) and (2) indicate that the phase noise is proportional to  $1/V_{pp}^2$  for linear operation and is proportional to  $1/V_{pp}^3$  when clipped by the power supplies. The additional noise reduction results from the fact that  $\Gamma(\omega t)$  is 0 when the voltage is clipped. Hence the period when the oscillator is susceptible to noise is reduced as the transitions take less time.

In reality, the clipping is rarely as hard as shown in Figure 2. We model this ‘‘soft clipping’’, shown in Figure 3 by

$$v(\omega t) = \frac{V_{dd}}{2} \tanh\left[\frac{V_{pp}}{V_{dd}} \sin(\omega t)\right]$$

The *ISF* is now given by eqn. (3) and the phase noise is then given by eqn.(4)

$$\Gamma(\omega t) = \frac{2 \cos(\omega t)}{V_{pp} \cosh^2\left[\frac{V_{pp}}{V_{dd}} \sin(\omega t)\right]} \quad (3)$$

$$L(\Delta\omega) = \begin{cases} \frac{64FkTR}{9V_{pp}^2} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (\text{for } V_{pp} \ll \frac{8V_{dd}}{3\pi}) \\ \frac{512FkTRV_{dd}}{27\pi V_{pp}^3} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (\text{for } V_{pp} \gg \frac{8V_{dd}}{3\pi}) \end{cases} \quad (4)$$

In Figure 4 we show the SSB phase noise at  $600kHz$  offset from a  $900MHz$  carrier frequency as a function of different signal voltage swings predicted by both hard clipping and soft clipping models. Here we assume that  $F = 4$ ,  $R = 1k\Omega$  and  $V_{dd} = 3.3V$ .

Both results indicate that the phase noise consists of two regions with regard to  $V_{pp}$ : a  $1/V_{pp}^2$  region without clipping and  $1/V_{pp}^3$  with clipping. The two equations provide slightly different break-even points between the two regions. The break-even point for the hard clipped model is  $V_{pp} = V_{dd}$ . While the break-even point for the soft clipped model is  $V_{pp} = 8V_{dd}/(3\pi) \approx 0.85V_{dd}$ . The phase noise values predicted by the two models are the same for small values of  $V_{pp}$  and only differ by 1.76dB for large values of  $V_{pp}$ .

Both models provide similar predictions for the phase noise. Hence, we expect the exact shape of the waveform not to significantly impact the phase noise performance. The models

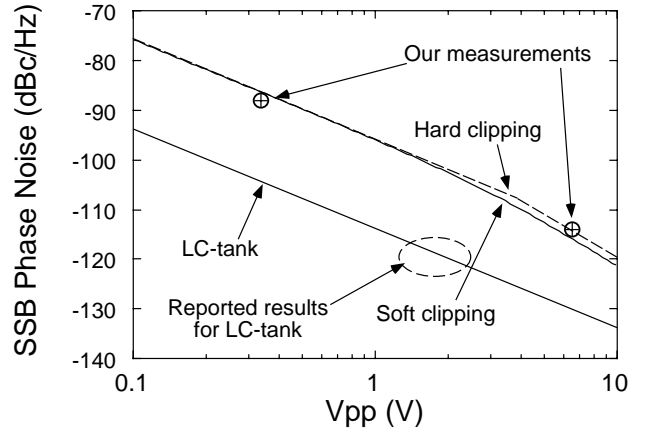


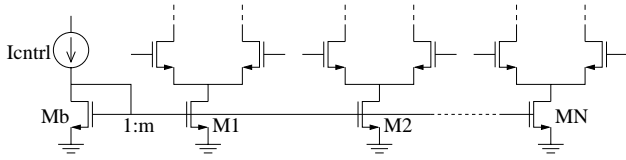
Figure 4: SSB phase noise vs.  $V_{pp}$

also suggest the additional reduction in phase noise when the voltage swing tends to exceed the power supply ( $V_{pp} > V_{dd}$ ).

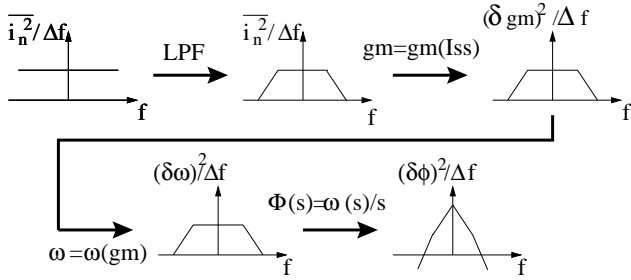
If active devices are used as loads instead of passive resistors, eqn.(4) has to be modified slightly. The resistor thermal noise  $4kT/R$  has to be replaced by  $4\gamma kTg_{ds0}$  for the active devices. The same derivation still holds. Eqn.(4) can now be rewritten as shown in eqn.(5), where  $I_{pp}$  is the peak-to-peak current. Maximizing  $V_{pp}$  is equivalent to maximizing the switching current. Eqn.(5) suggests that for a given power supply current, improving the current switching efficiency can reduce the phase noise. For a fully differential ring oscillator with tail current supply, an ideal case would be that all the tail current is used for switching, i.e., a current switching efficiency of 100. In other circuit topologies, the maximal current for charging and discharging the load capacitors sets a lower bound on the phase noise for a given power.

$$L(\Delta\omega) = \begin{cases} \frac{64F\gamma kTg_{ds0}}{9I_{pp}^2} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (\text{for } V_{pp} \ll \frac{8V_{dd}}{3\pi}) \\ \frac{512F\gamma kTg_{ds0}V_{dd}}{27\pi I_{pp}^2 V_{pp}} \left(\frac{\omega_0}{\Delta\omega}\right)^2 & (\text{for } V_{pp} \gg \frac{8V_{dd}}{3\pi}) \end{cases} \quad (5)$$

The trade-off between power consumption and phase noise can also be seen from eqn.(5). A simple way of scaling power consumption is to scale the device sizes. If all the device sizes are scaled by a factor of  $\alpha$ , the internal currents will be scaled by  $\alpha$ , and all the node voltages will remain unchanged. As a result, the power consumption is scaled by  $\alpha$ . According to eqn.(5), when  $g_{ds0}$  becomes  $\alpha g_{ds0}$  and  $I_{pp}$  becomes  $\alpha I_{pp}$ , the phase noise is scaled by  $1/\alpha$ . Therefore, the phase noise is inversely proportional to the oscillator power consumption. In other words, the phase noise can be reduced by  $3dB$  by doubling the power consumption. Another intuitive explanation to the trade-off between phase noise and power consumption is that when the device sizes are doubled, the signal doubles in amplitude and the noise only doubles in power. This results in a  $3dB$  improvement in SNR. The remaining question to be answered is how to minimize the phase noise for a given power consumption.



**Figure 5: Bias structure for an N-stage ring oscillator**



**Figure 6: Up-conversion mechanism for low frequency noise in the tail and bias**

A survey of published literature suggests that the phase noise of LC-tank oscillators is close to  $-120\text{dBc}/\text{Hz}$  when the results are scaled to a  $600\text{kHz}$  offset from a  $900\text{MHz}$  center frequency [5, 6, 7]. They are located within the dashed ellipse in Figure 4. The phase noise curve for LC-tank oscillators is also plotted in this figure for  $F = 4, R = 1\text{k}\Omega$  and  $Q = 6$ . Our calculation suggests that the phase noise for ring oscillators is likely to be significantly higher than that of LC-tank oscillators unless there is rail-to-rail switching, and efficient switching is the only possible approach. Figure 4 also shows the measurement results for our ring oscillators that match our analysis. Details are provided in a later section.

### 3. NOISE UP-CONVERSION

In a fully differential ring oscillator low-frequency noise from the bias and the tail devices is up-converted to the vicinity of the carrier frequency by frequency modulation. This is not modeled by our previous analysis or any previously published work. In this section, we analyze this noise up-conversion mechanism and later validate it via simulations.

An N-stage ring oscillator is generally biased as shown in Figure 5. Noise in the tail current causes the  $g_m$  of the delay cell to change, hence varying the instantaneous oscillation frequency. We will first consider thermal noise, and then extend our analysis to include flicker noise.

This up-conversion mechanism is illustrated in Figure 6. First, the noise is band-limited by the poles at the drains of  $M_b, M_1, M_2, \dots, M_N$ . This low-pass filtered noise then modulates the  $g_m$  of the delay cells, and results in frequency variation. Finally, since  $\phi(t) = \int_{-\infty}^t \omega(\tau) d\tau$  in the time domain, they satisfy  $\Phi(s) = \Omega(s)/s$  in s-domain. The phase noise has a  $1/f^2$  shape at low offset frequencies and drops off at a faster rate for higher offset frequencies. However,

since the low-pass bandwidth is usually in the same order as or even larger than the oscillation frequency, the faster phase noise roll-off is rarely observed and it is of little interest. Additionally, we are usually more concerned with the up-conversion of the low-frequency noise. This is more of an issue when flicker noise is present and causes the phase noise to rise at a more rapid rate at low offset frequencies.

We treat the noise from the bias transistor  $M_b$  separately from the noise contributed by transistors  $M_{1..N}$  in Figure 5, because the noise from  $M_b$  is correlated for all stages while the noise from  $M_{1..N}$  is not. In the following derivation, we assume that the current mirrors have a ratio of  $1 : m$  as shown in Figure 5.

In general, the oscillation frequency  $\omega_0$  is proportional to  $g_m/C_L$ , where  $C_L$  is the load capacitance for the delay cell. As an example,  $\omega_0 = (\sqrt{3}/2)(g_m/C_L)$  for a 3-stage ring oscillator. Even though  $C_L$  includes a voltage-dependent part, its variation is usually much smaller than the variation of  $g_m$  in the presence of noise. We can therefore derive the relation in eqn.(6) using this assumption.

$$\left| \frac{\delta\omega}{\omega_0} \right| = \left| \frac{\delta g_m}{g_m} \right| \quad (6)$$

When operated in the long channel regime, the  $g_m$  of each delay cell is given by  $g_m = \sqrt{(k'WI_{ss})/L}$ , where  $I_{ss}$  is the tail current. This is valid for all the reasonable gate overdrive voltages [8]. Considering eqn.(6), it can be shown that eqn.(7) is valid.

$$\left| \frac{\delta\omega}{\omega_0} \right| = \left| \frac{\delta g_m}{g_m} \right| = \frac{1}{2} \left| \frac{\delta I_{ss}}{I_{ss}} \right| \quad (7)$$

The thermal noise density from  $M_b$  is  $\overline{i_n^2}/\Delta f = 4kT\gamma g_{ds0,b}$ , where  $g_{ds0,b}$  is the  $g_{ds0}$  for  $M_b$ . The noise power is amplified by  $m^2$  times by each tail device. We can also replace  $mg_{ds0,b}$  with  $g_{ds0}$  for the tail devices. Hence the normalized variation in frequency is given by eqn.(8).

$$\frac{(\delta\omega)^2/\Delta f}{\omega_0^2} = \frac{(\delta g_m)^2/\Delta f}{g_m^2} = \frac{mkT\gamma g_{ds0}}{I_{ss}^2} \quad (8)$$

Finally we can write the resulting phase noise as shown in eqn.(9).

$$\begin{aligned} \frac{(\delta\phi)^2}{\Delta f} &= \frac{1}{\Delta\omega^2} \cdot \frac{(\delta\omega)^2}{\Delta f} \\ &= \frac{\omega_0^2}{\Delta\omega^2} \cdot \frac{(\delta\omega)^2/\Delta f}{\omega_0^2} \\ &= \frac{mkT\gamma g_{ds0}}{I_{ss}^2} \left( \frac{\omega_0}{\Delta\omega} \right)^2 \end{aligned} \quad (9)$$

The noise from  $M_1$  to  $M_N$  are treated in a similar manner to the noise from  $M_b$  except that the noise is uncorrelated for each tail device. Eqn.(7) has to be modified as shown in eqn.(10) where  $g_{m,i}$  and  $I_{ss,i}$  are the  $g_m$  and  $I_{ss}$  for the  $i$ th delay cell.

$$\left| \frac{\delta\omega}{\omega_0} \right| = \frac{1}{N} \left| \frac{\delta g_{m,i}}{g_{m,i}} \right| = \frac{1}{2N} \left| \frac{\delta I_{ss,i}}{I_{ss,i}} \right| \quad (10)$$

Considering that there are  $N$  delay stages, the resulting phase noise expression is given by eqn.(11).

$$\frac{(\delta\phi)^2}{\Delta f} = \frac{kT\gamma g_{ds0}}{NI_{ss}^2} \left(\frac{\omega_0}{\Delta\omega}\right)^2 \quad (11)$$

The SSB phase noise  $L(\Delta\omega)$  is  $1/4$  of  $(\delta\phi)^2/\Delta f$ , since the phase noise is split equally on both sides of the carrier. Therefore, the total noise contributed by the bias transistor  $M_b$  (eqn.(9)) and the  $N$  tail devices (eqn.(11)) is given by eqn.(12).

$$L(\Delta\omega) = \frac{1}{4} \frac{(\delta\phi)^2}{\Delta f} = \frac{(\frac{1}{N} + m)kT\gamma g_{ds0}}{4I_{ss}^2} \left(\frac{\omega_0}{\Delta\omega}\right)^2 \quad (12)$$

The up-conversion of flicker noise can be treated in a similar fashion. If the flicker noise is modeled as [9]

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{K_f \cdot I_{ds}^{A_f}}{C_{ox} L_{eff}^2 f}$$

where  $K_f$  and  $A_f$  are flicker noise parameters. Then eqn.(12) can be modified for flicker noise as shown in eqn.(13).

$$L(\Delta\omega) = \frac{\pi(\frac{1}{N} + m)K_f \cdot \omega_0^2}{8C_{ox} L_{eff}^2 I_{ss}^{2-A_f} \Delta\omega^3} \quad (13)$$

Since  $m$  is usually much larger than  $1/N$ , the up-conversion of the noise from  $M_b$  is likely to be more severe than that from the tail devices. In practice, the flicker noise from  $M_b$  could be a major noise source at low offset frequencies. This is confirmed by our simulation and measurement results in the following sections.

#### 4. SIMULATION RESULTS

In this section, we simulate the phase noise for a ring oscillator and show that the low frequency noise in the current bias/control can affect the phase noise significantly. We also verify the noise up-conversion process analyzed in the previous section.

We consider the circuit in Figure 7 as an example.  $M_1 - M_5$  is a delay cell of a 3-stage ring oscillator and the current bias and frequency control are supplied through  $M_6$  (Figure5). We apply the analysis methodology proposed in [3] by injecting a current pulse into the nodes 1, 2 and 3 throughout a complete clock cycle and observe the phase shift after it settles into steady state again. The effective  $ISFs(\Gamma_{effs})$  which are modulated by the thermal and flicker noise are calculated for each individual device.

As mentioned in [3] for thermal noise the RMS values for the  $\Gamma_{effs}$  is important and for flicker noise the mean values of the  $\Gamma_{effs}$  is important. Table 1 lists the RMS values for  $\Gamma_{eff,thermal}$ s and mean values for  $\Gamma_{eff,flicker}$ s for all the transistors in the delay cell. It can be seen that the thermal noise contribution of all the devices are similar in magnitude, though the contribution of  $M_{2,3}$  is slightly larger than the others. However, for flicker noise the contributions of  $M_1$

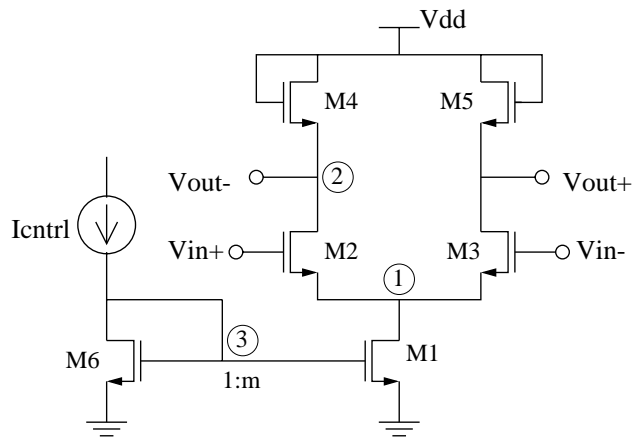


Figure 7: Differential delay cell and bias transistor

RMS/Mean for $\Gamma$	$M_1$	$M_{2,3}$	$M_{4,5}$	$M_6$
Thermal ( $deg/sec^{1/2}$ )	25	89	55	42
Flicker ( $deg/sec$ )	-2128	35	-168	7231

Table 1:  $\Gamma_{RMS,eff,thermal}$  and  $\overline{\Gamma_{eff,flicker}}$

and  $M_6$  dominate, suggesting that the majority of the low frequency phase noise is contributed by the bias devices.

We have only included a single device  $M_6$  in the bias. In reality, more devices are often used for the bias. For example, a voltage-to-current converter is usually needed between the loop filter and the VCO in a PLL. Any low frequency noise generated in  $I_{cntrl}$  is equivalent to an increase in the noise from  $M_6$  and could potentially dominate the low-frequency phase noise.

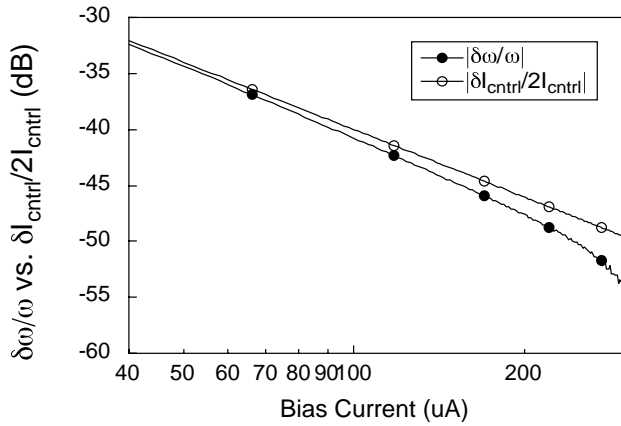
We verify our noise up-conversion analysis by using the circuit in Figure 7. We vary the bias current, and observe the variation in frequency in the steady state. Assuming  $I_{ss}$  is proportional to  $I_{cntrl}$  and  $\partial\omega/\partial I_{ss}$  is the same for DC and any low frequency noise in  $I_{ss}$ , we verify eqn.(7) in the previous section. Figure 8 provides the comparison between  $|\delta\omega/\omega|$  and  $|\delta I_{cntrl}/2I_{cntrl}|$ .

In Figure 8, both  $|\delta\omega/\omega|$  and  $|\delta I_{cntrl}/2I_{cntrl}|$  are drawn as functions of the bias current. In the simulation,  $\delta I_{cntrl}$  is given a fixed value so that  $I_{cntrl}$  is swept linearly. Therefore, the curve of  $|\delta I_{cntrl}/2I_{cntrl}|$  drops at a slope of 20dB/decade. The two curves match extremely well for low bias currents. The error increases with larger bias current because of short channel effects and current mirror mismatch due to the channel length modulation.

To take into account of short channel effects, the drain-to-source current can be modeled as shown in eqn.(14) [10].

$$I_D = \frac{\beta}{2}(1 - \epsilon_1)(V_{gs} - V_T)^{2-\epsilon_2} \quad (14)$$

where  $\epsilon_1$  and  $\epsilon_2$  are empirical numbers. They approach 0



**Figure 8: Simulation of frequency variation vs. bias current variation**

for long channel devices and take on larger values for short channel devices. By following a similar derivation as above, it can be shown that

$$\left| \frac{\delta\omega}{\omega_0} \right| = \frac{1 - \epsilon_2}{2 - \epsilon_2} \left| \frac{\delta I_{ss}}{I_{ss}} \right|$$

The factor  $(1 - \epsilon_2)/(2 - \epsilon_2)$  becomes smaller for short channel devices. This explains why the curve  $|\delta\omega/\omega_0|$  drops more rapidly for large bias currents. As a result, both eqns. (12) and (13) have to be multiplied by  $4 \left( \frac{1 - \epsilon_2}{2 - \epsilon_2} \right)^2$  to account for short channel effects.

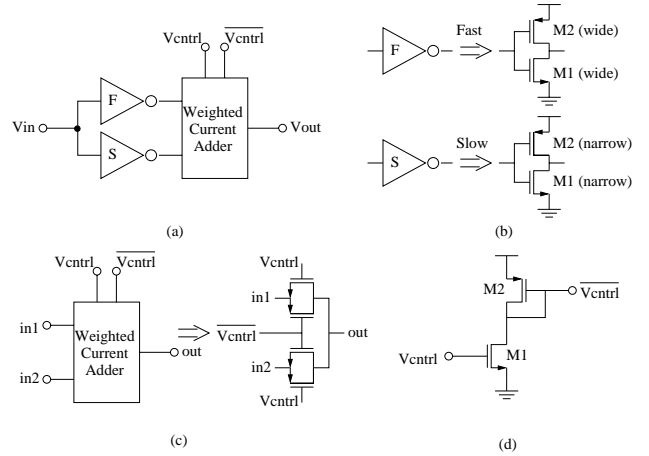
When  $I_{ctrl}$  increases, the mismatch between the drain voltages of  $M_b$  and  $M_1$  increases. This causes  $I_{ss}$  not to increase as much as  $I_{ctrl}$ . As a result, the oscillation frequency becomes less sensitive to  $I_{ctrl}$ , and the curve of  $\delta\omega/\omega_0$  falls further below the curve of  $\delta I_{ctrl}/I_{ctrl}$  in Figure 8 for the increased bias currents.

Despite the short channel effects and current mirror mismatch, our simulations confirm our model for noise up-conversion. Our conclusions are further strengthened by our measurement results in the next section.

## 5. EXPERIMENTAL RESULTS

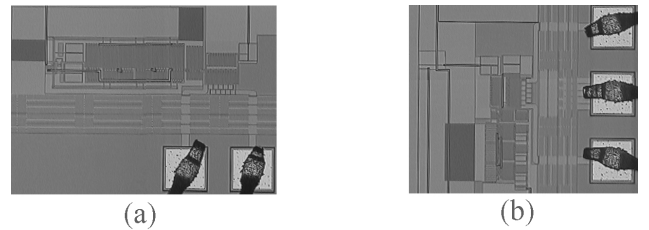
In addition to the fully differential oscillator shown in Figure 7, we also designed the coupled-ring oscillator shown in Figure 9. Weighted current adders are used to determine how much current is drawn from the fast and slow inverters to charge and discharge the load capacitors. Therefore, the oscillator frequency is continuously tuned between the frequencies set by the fast and slow inverters. We achieve complete rail-to-rail switching by using digital inverters. Additionally, this eliminates the current mirror bias structure. For both these reasons we expect less phase noise from this circuit than from the circuit in Figure 7.

Both oscillator designs were fabricated via MOSIS in a  $0.5\mu\text{m}$  CMOS technology. Micro photographs for both designs are shown in Figs. 10 (a) and (b). Their outputs are measured with a spectrum analyzer and resulting phase



**Figure 9: coupled-ring oscillator (a) delay cell (b) strong and weak inverters (c) weighted current adder (d) complementary control generator**

noise is computed by taking the noise power spectral density normalized by the carrier power.



**Figure 10: Die photo for (a) the ring oscillator from Figure 7 (b) the coupled-ring oscillator from Figure 9**

Figure 11 shows two experimental results for the differential oscillator from Figure 7 with a  $1.38\text{GHz}$  center frequency. In the first experiment, a  $100\mu\text{F}$  by-pass capacitor is connected between the bias point and ground so that most of the noise from  $M_6$  is filtered out and does not cause phase noise. In the second experiment, a  $11.7\text{nF}$  capacitor is used instead. Due to the higher low-pass corner frequency, some of the low frequency noise from  $M_6$  is up-converted to phase noise by frequency modulation. With a large by-pass capacitor, the phase noise curve falls well into the  $1/f^2$  region. With a small by-pass capacitor, the phase noise curve starts to rise at low offset frequencies and enters the  $1/f^3$  region. This implies that the flicker noise from the bias transistor can dominate at low frequencies which confirms our previous theoretical analysis. In practice, the bias point is an internal node and no large off-chip capacitor is available to by-pass the flicker noise from  $M_6$ . Therefore, for an integrated VCO design, the current mirror bias structure should be avoided if possible.

The SSB phase noise for the coupled-ring oscillator was also measured and compared with the fully differential ring oscillator in Figure 7. The results are shown in Figure 12. The

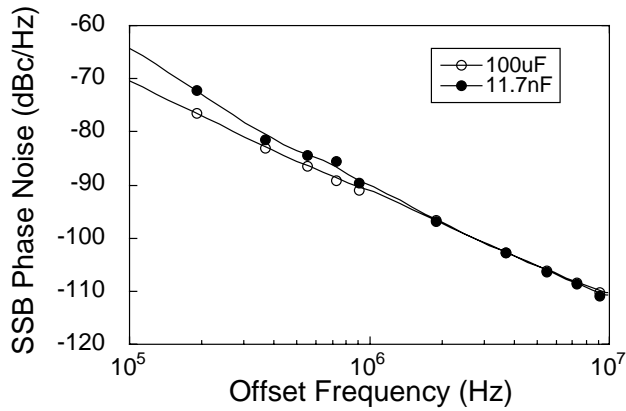


Figure 11: Phase noise with different by-pass capacitors

center frequency for the coupled-ring oscillator is  $960\text{MHz}$ . For a fair comparison, the phase noise of the fully differential ring oscillator is also scaled to  $960\text{MHz}$ . The measured SSB phase noise at a  $600\text{kHz}$  offset frequency is  $-114\text{dBc/Hz}$  for the coupled-ring oscillator.

As we are unable to measure the actual voltage swings without loading the oscillator, we use simulation results for  $V_{pp}$  as a guide. Our simulation indicates an unclipped  $V_{pp} = 6.48\text{V}$ . Its phase noise is  $26\text{dB}$  lower than that measured for the fully differential design in Figure 7. The majority of this difference is due to the difference in their internal voltage swings. According to our simulation the voltage swing for the differential oscillator is  $336\text{mV}$ , which accounts for about  $28\text{dB/Hz}$  difference in the SSB phase noise. Both results are marked in Figure 4 with circled plus signs. They match our theoretical predictions very well for fairly typical values for  $F$  and  $R$  ( $F = 4$ ,  $R = 1\text{k}\Omega$ ).

The phase noise for the coupled ring oscillator rises faster at offset frequencies that are less than  $300\text{kHz}$ . Our simulation suggests that this is mostly due to the flicker noise in the fast inverters. We would expect the phase noise due to both the flicker noise and the thermal noise to decrease with faster transitions in smaller geometry processes.

## 6. CONCLUSIONS

In this paper we have analyzed ring oscillator phase noise for both linear and non-linear conditions. We show that in order to achieve good phase noise performance, comparable with LC-tank oscillators, a rail-to-rail voltage swing is needed and the oscillator has to operate in the hard-switching mode. Under the constraint of a fixed power budget, the only way to achieve this goal is to improve current switching efficiency. We also model the low frequency noise up-conversion mechanism via the current bias circuits. Our simulation shows that the up-conversion of the noise from the devices in the bias/control circuit is significant and can potentially dominate the phase noise. As a result, the bias/control circuit has to be designed carefully. We have also presented experimental results to confirm our theoretical analysis. The

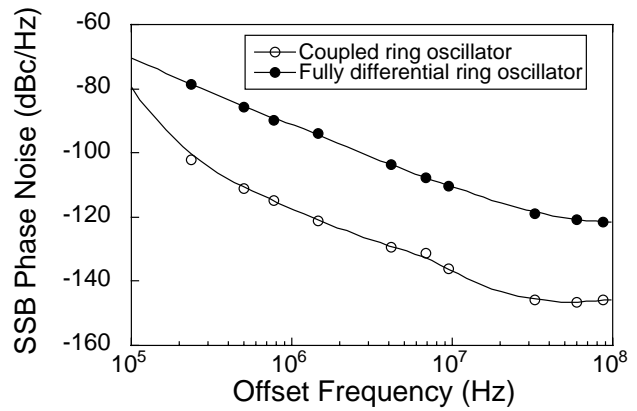


Figure 12: SSB phase noise comparison between the coupled-ring oscillator and the differential ring oscillator in Figure 7

measured SSB phase noise for a coupled-ring oscillator was  $-114\text{dBc/Hz}$  at  $600\text{kHz}$  offset from the center frequency of  $960\text{MHz}$ .

## 7. REFERENCES

- [1] Todd C. Weigandt, Beomsup Kim and Paul R. Gray, "Analysis of Timing Jitter in CMOS Ring Oscillators", in *Proc. IEEE Int. Symp. Circuits and Systems*, volume 4, pp. 27–30, London, UK, June 1994.
- [2] Behzad Razavi, "A Study of Phase Noise in CMOS Oscillators", *IEEE Journal of Solid-State Circuits*, vol. 31, n. 3, pp. 331–343, March 1996.
- [3] Ali Hajimiri and Thomas H. Lee, "A General Theory of Phase Noise in Electrical Oscillators", *IEEE Journal of Solid-State Circuits*, vol. 33, n. 2, pp. 179–194, February 1998.
- [4] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum", in *Proc. of IEEE*, pp. 329–330, February 1966.
- [5] Jan Craninckx and Michel S. J. Steyaert, "A 1.8-GHz CMOS Low-Phase-Noise Voltage-Controlled Oscillator with Prescaler", *IEEE Journal of Solid-State Circuits*, vol. 30, n. 12, pp. 1474–1482, December 1995.
- [6] Jan Craninckx and Michiel S. J. Steyaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors", *IEEE Journal of Solid-State Circuits*, vol. 32, n. 5, pp. 736–744, May 1997.
- [7] Peter Kinget, "A Fully Integrated 2.7V 0.35 $\mu\text{m}$  CMOS VCO for 5GHz Wireless Applications", in *IEEE ISSCC Digest of Technical Papers*, pp. 226–227, San Francisco, February 1998.
- [8] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, ch. 3, Cambridge University Press, 1998.
- [9] Meta-Software, *HSPICE User's Manual: Software for IC Design*, version 96.1 Edition, February 1996.
- [10] Daniel P. Foty, *MOSFET Modeling With SPICE: Principles and Practice*, Prentice Hall, 1996.