Panel
System-Level Design: Designers' Wish List vs. Reality

Abstract

System level design has brought together a number of formidable challenges, such as methodology, software and hardware design and design automation, to name a few. More than ever, the successfull design of a system requires all these challenges to be addressed - by both the designers and the design automation tools.

Designers, better and anyone else, know what the problems are. Design automation companies claim to know how to solve them and have the products to prove it. Is this really true? Are the design automation tools really solving the hard problems or skimming over the real challenges. This panel addresses exactly that by confronting the views of distinguished designers and tools developers.

The panelists belong to two teams. The designer team will present the main problems in doing system design including verification, IP use, integration and synthesis among others, and try to show that many of the real problems are not being addressed by current tools. The tools team will explain how the tools are indeed tackling the real problems and how the designers can make the best use out of them.

The attendees can expect a very interesting, informative and technical debate. At the end, the audience will be the judge and a veredict will be passed on what the real problems are, which ones can be solved with existing tools, and what needs to be done in the future to address the system design challenges.

Panelists:

Michael Franz, Toshiba USA, CA

Graham Hellestrand, VaST Systems Technology, CA

Arkady Horak, Motorola, TX

Joachim Kunkel, Synopsys Inc., CA

William Lee, IBM Corporation, NC

Grant Martin, Cadence Design Systems, CA

Kees Vissers, Philips Research Laboratories, Eindhoven, The Netherlands

Organizers and Moderators:

Daniel Gajski, University of California, Irvine, CA

Reinaldo Bergamaschi, IBM T. J. Watson Research Center, NY