A High Speed and Low Power Phase-Frequency Detector and Charge - pump

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Abstract – In this paper, we introduce a high-speed and low power Phase-Frequency Detector (PFD) that is designed using modified TSPC (True Single-Phase Clock) positive edge triggered D flip-flop. This PFD has a simpler structure with using only 19 transistors. The operation range of this PFD is over 1.2Ghz without additional prescaler circuits. Furthermore, the PFD has a dead zone less than 0.01ns in the phase characteristics and has low phase sensitivity errors. The phase and frequency error detection range is not limited as in the case of the pt-type and nc-type PFDs [3]. Also, the PFD is independent from the duty cycle of input signals. A new charge-pump circuit is presented that is designed using a charge-amplifier. A stand – by current enhances the speed of charge – pump and removes the charge – sharing which causes a phase noise in the charge – pump PLL. Also, the effects of clock feed – through are reduced by separating the output stage from UP and down signal. The simulation results base on a third – order PLL are presented to verify the lock – in process with the proposed PFD and Charge – pump circuits. The PFD and charge – pump circuits are designed using 0.8 ㎛ CMOS technology with 5V supply voltage.

I. INTRODUCTION

The input phase errors are detected by Phase - Detector (PD) or Phase – Frequency Detector (PFD). These errors, phase or frequency errors, are converted into current or voltage to control the output frequency of Voltage Controlled Oscillator (VCO) by charge pump in a charge – pump PLL. PD detects a phase error between the reference signal and the output signal of PLL. And the error detection range can be extended with PFD. A conventional CMOS PFD [1] is shown in Fig.1. This PFD has large dead zone in phase characteristics at the steady state which generates a large jitter in locked state in PLL. Also, a large amount of power consumption cannot be avoided in high frequency operations because internal nodes of PFD are not completely pull up or pull down. The additional prescaler circuits can be added to lower frequency of the input signals. However, as the division ratio increases, the steady state phase error will increase. A pt-type [2] and a nc-type PFDs [3] are shown in Fig.2 A pt-type PFD [Fig2.b] has very high speed, but dead zone exists. A nc-type PFD [Fig2.a] has no dead-zone, but phase characteristics depend on a duty cycle of input signals.

The capture range of PLL is determined by the error detection range of PFD. A conventional CMOS PFD has no limit to the error detection range. Therefore, the capture range of PLL is only limited by the Voltage Controlled Oscillator (VCO) output frequency range [5]. However, the error detection ranges of pt-type and nc-type PFDs are limited within $-\pi \sim +\pi$. So the capture range of PLL with these PFDs is only limited by input reference signals.

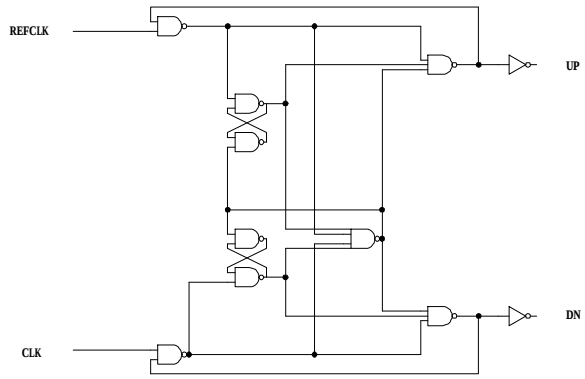

Fig.1. A conventional CMOS PFD [1].

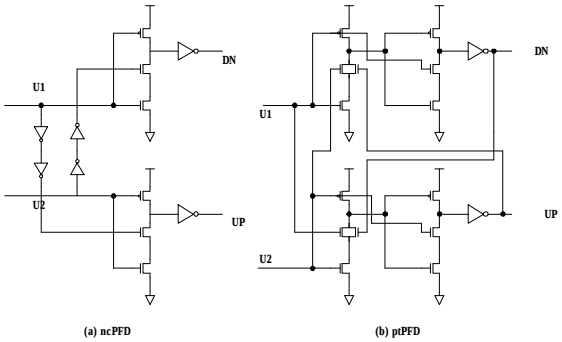

Fig.2. A high speed PFDs [2],[3].

The PFD and charge-pump circuits provide a transfer function of input phase error to the output charge per clock cycle [4]. Whenever UP and DOWN signals are switching, a conventional tri-state charge-pump [1] has problems such as charge sharing in high impedance- state, charge injection and clock feed through [5]. The clock feed through and

charge sharing introduce a step phase noise to a charge – pump PLL.

We propose a simple sequential type PFD circuit which uses modified TSPC positive edge triggered D flip-flop whose phase and frequency error detection range is not limited. Also, we present a new charge-pump circuit which is designed using a current - amplifier. The charge-pump reduces the effects of clock feed through and a charge sharing.

In section II and III, the proposed positive edge triggered D flip-flop and charge-pump circuit is described respectively. The phase and frequency characteristics of proposed PFD circuit are presented, and comparisons are made in section IV. In section V, a third - order PLL is designed to check the lock-in properties of proposed PFD and charge-pump circuits. In section VI, draw a conclusions.

II. Design of positive edge triggered D flip -flop

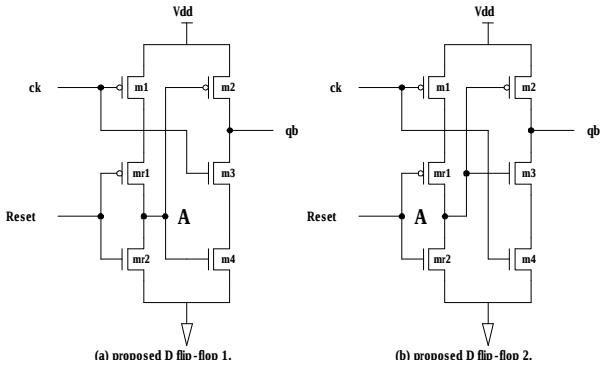

Fig.3. A circuit schematic of proposed D flip-flop

A circuit schematic of proposed D flip-flops is shown in Fig. 3. These flip – flops are modified the TSPC flip-flop [6] to satisfy the required function of D flip-flop for PFD. The operations of the proposed D flip – flop are very simple. When input clock and reset signals are low, the node A is connected to VDD through m1, mr1 and charges the node A to VDD. At the rising edge of the clock signal, output node is connected to ground through m3 and m4. Once the node A is charged to VDD, the output node is not affected by input clock signal. Because the charges at node A turn off the m3 and this prevents the output node from pulled up. Therefore, the output node is disconnected from input node. When the reset signal is applied, node A is disconnected from VDD by mr1 and connected to ground by mr2. As soon as the node A is discharged, the output node is pulled up through m2. The mr1 is added to prevent the short – circuit that happens whenever the reset signal is applied. If the clock signal is low in the condition of reset signal is high, a current path is made from VDD to ground without mr1. This increases the power consumption. Moreover, the reset time is increased because m1 charges the node A to VDD while the mr2 discharges node A to ground. Fast discharging node A means the fast reset operation. The operations of D flip – flop in Fig3.a and Fig.3.b are same but the connection is different. Dynamic power consumption can be reduced by lowering the internal switching and speed is increased by shortening the input to output path.

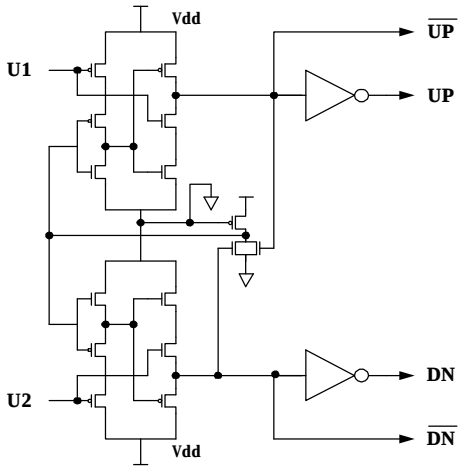

Fig.4. Full schematic of PFD

Full schematic of proposed PFD is shown in Fig.4. A conventional sequential type PFD structure is used. And for high-speed operation, a pseudo - NOR gate is used.

III. Design of charge - pump

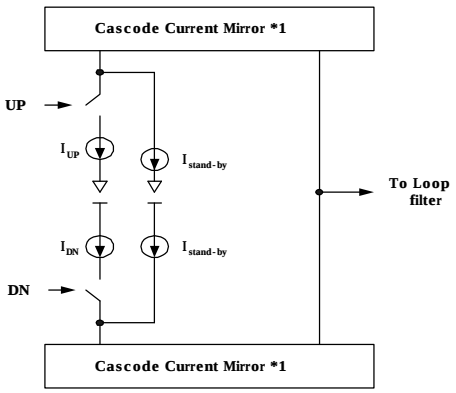

Fig.5. Block diagram of proposed charge-pump

A proposed charge-pump circuit is shown in Fig.5. The charge – pump consists of current amplifier with stand-by current and switched current source. The operation of charge – pump is similar to the conventional tri-state charge-pump. But the control switch is not connected directly to the output stage in order to reduce the effect of clock feed – through which causes the step phase - jump error whenever the UP/DN signals make transition. And stand - by current source added to the input of the charge – pump to enhance the speed of charge - pump. Also the stand – by current eliminates high – impedance state in the tri-state charge-pump which causes a charge sharing problems. The output current of charge - pump is same as conventional tri-state charge – pump. The stand-by current does not affect the output current only enhance the speed of charge - pump.

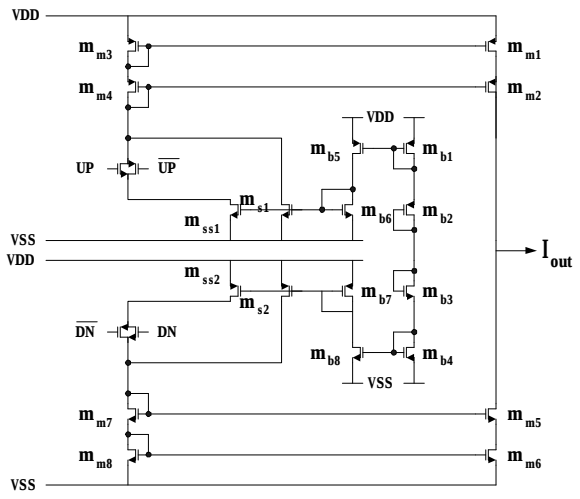

Fig.6. Circuit schematic of proposed Charge- pump

A detailed circuit schematic is shown in Fig.6. $m_{b1} \sim m_{b8}$ is a bias circuit for stand – by current(m_{s1},m_{s2}) and current sources(m_{ss1},m_{ss2}). Switch is implemented using transmission gate to reduce clock feed - through and the current mismatch caused by path delay mismatch can be reduced. Cascode current sources are used to increase the output impedance.

IV. PHASE CHARACTERISTICS

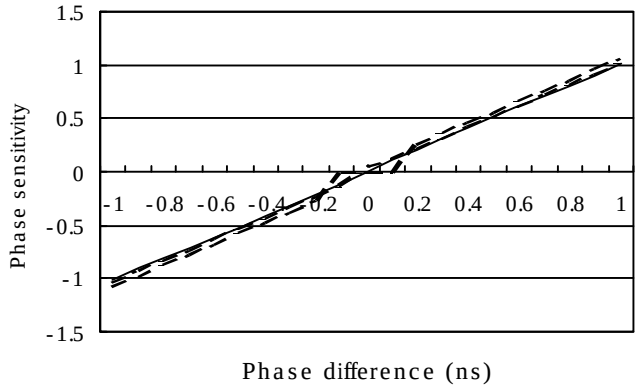

Fig.7. Phase characteristics of the pt-type PFD (dashed-line), and nc-type PFD (long dashed-line), and proposed PFD (solid line).

Fig.8. shows the phase characteristics of proposed PFD together with pt-type PFD and nc-type PFD. The pt-type PFD has 0.15ns dead zone and nc-type PFD has constant offset in phase characteristics. Moreover, nc-type PFD depends on the duty cycle of the input signals. The nc-block or flip-flop of nc-type and pt-type PFD are controlled by both input signals while the proposed PFD does not depend on other input signals. So the phase sensitivity error caused by input signal dependence is reduced. Phase sensitivity errors of pt-type PFD, nc-type PFD and proposed PFD are shown in Fig.8. Phase sensitivity errors are reduced less than 0.02ns with proposed PFD. The nc-type PFD has various phase offsets caused by the duty cycle of input signals. The pt-type PFD has similar phase characteristic to the proposed PFD. However, since the flip-flops are controlled by both input signals, the output signal is dependent on the state of input signals. This increases the phase sensitivity error.

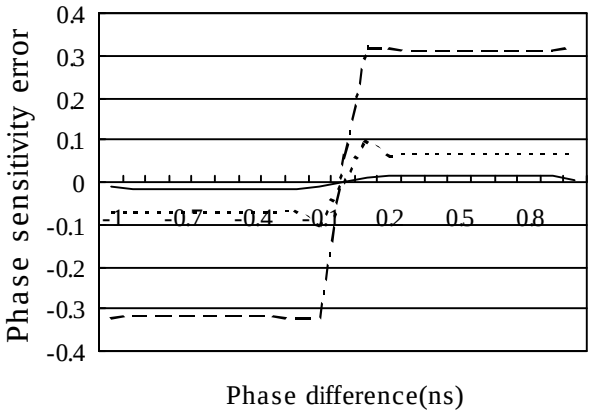

Fig.8. Phase sensitivity error of the pt-type PFD (dashed-line), and nc-type PFD (long dashed-line), and proposed PFD (solid line).

Setup and reset delay of proposed PFD as a function of supply voltage are shown in Fig.9. The setup delay of proposed PFD varies from 0.1ns up to 0.25ns as supply voltage decreases. But the reset delay varies from 0.45ns up to 1.45ns because of the delay of NOR gate increases significantly.

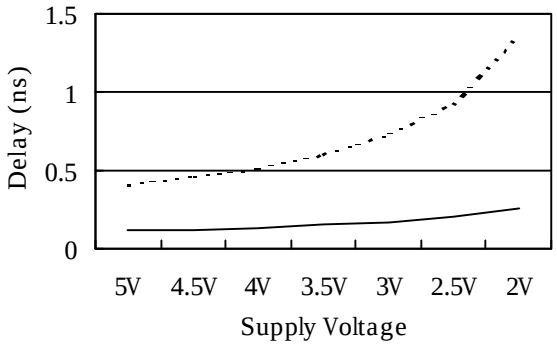

Fig.9. Setup delay(solid line) and Reset delay(dashed line) of proposed PFD as a function of supply voltage

V. VERIFICATION OF PFD AND CHARGE –PUMP WITH THIRD – ORDER CHARGE – PUMP PLL

In order to verify the lock – in properties of the proposed PFD and charge – pump, a complete third order charge – pump PLL was designed. The circuit schematic of VCO [6] and Loop – Filter is shown in Fig 10. The output frequency range of VCO measured from 650MHz up to 1.4Ghz. The gain of VCO is measured -592MHz/V. The key parameters of loop-filter are as follows. [R1=8K, R2=1K, C1=10pF, C2=2pF].

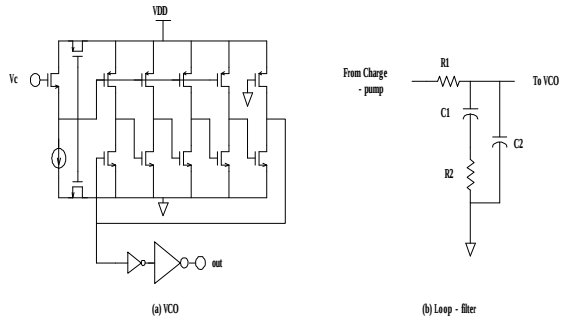

Fig.10. A circuit schematic of VCO [6] and Loop-filter

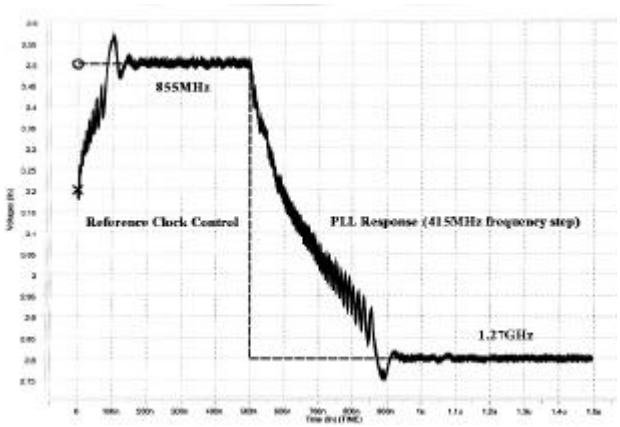

Fig.11. PLL step response for 415MHz frequency step

Fig.11. shows the step response of a third – order PLL. Step response of PLL is simulated using a same VCO that is used in PLL as a reference clock generator with phase noise. A dashed line represents the control voltage of reference VCO and the solid line shows the Loop – filter output. It takes 450ns for lock – in process about a 415Mhz frequency step is applied.

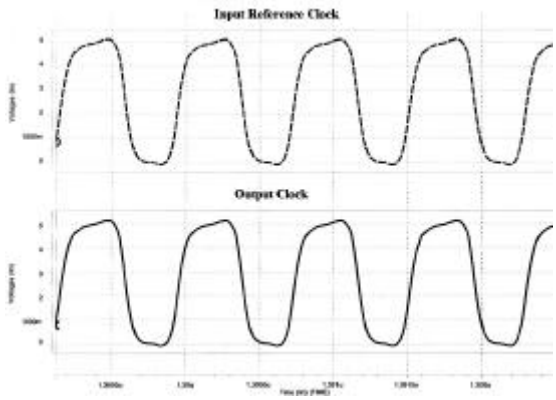

Fig.12. Input reference clock and output clock of PLL

Fig.12. represents the 1.27Ghz input reference and output clock signal of a third - order PLL. The steady state phase error (clock skew) measured 10.2ps.

VI. Conclusions

For high speed and low power CMOS PLL, we proposed a dynamic CMOS positive edge triggered D flip-flop for PFD and current amplifier charge – pump circuit. The proposed PFD has simpler structure and lower power dissipation. The dead zone of PFD is less than 0.01ns and error detection range is not limited. The proposed charge amplifier type charge – pump circuit reduces the effects of clock feed – through. Also, stand – by current removes the charge – sharing at high impedance state and the speed of the charge – pump circuit is increased. A simulation results based on a third - order PLL indicates that the proposed PFD operates over 1.2Ghz without additional prescaler circuits in 0.8-μm CMOS with 5Vsupply voltage. The steady state phase errors are measured less than 12ps and jitter is reduced to 15ps at 1.27Ghz input reference. The proposed dynamic CMOS PFD and charge amplifier type charge – pump circuits can be used in high frequency region over 1.2Ghz with precise and fast lock – in process.

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