Manufacturability of Low Power CMOS Technology Solutions

A. J. Strojwas[†], M. Quarantelli[†*], J. Borel[‡], C. Guardiani[**],
G. Nicollini[**], G. Crisenza[**], B. Franzini[**], J. Wiart[**]

[†]Dept. of Electrical and Computer Engineering,Carnegie Mellon University, 5000 Forbes Ave., Pittsburgh PA 15213, USA
[*]On leave from Università di Brescia, Dipartimento di Elettronica per l'Automazione, v. Branze 38, 25123 Brescia, Italy
[‡]SGS-Thomson Microelectronics, Central R&D, 850 rue J. Monnet, BP 16, 38926 Crolles cedex, France
[**]SGS-Thomson Microelectronics, Central R&D, v. C.Olivetti 2, 20041 Agrate Brianza, Italy

Abstract

This paper discusses manufacturabilty of state-of-the-art low power technologies. We report the results on two generations of bulk CMOS technologies, triple-well CMOS and Thin Film Silicon on Insulator (TFSOI) technologies. We present technology capabilities for several values of supply voltage and address the issue of performance scaling with the supply voltage reduction. Then we focus on the statistical characterization of these technologies and discuss both interchip and intrachip variations. Finally, we present the digital and analog designer perspectives on the low power IC operation.

Introduction

Reduction of IC power consumption is typically synonymous with the reduction of the dynamic power dissipation, P_{charge}, in digital IC's. In such a case, low power design can be achieved by reducing the following parameters: supply voltage, load capacitances and circuit activity rate. The decrease in supply voltage is the most effective method since the dynamic power dissipation is proportional to the square of supply voltage. Reduction of load capacitances is limited if we assume that the interconnect capacitances dominate which is the case for the scaled down technologies. Power savings can be also achieved by a number of architectural solution aimed at decreasing the activity rate. These solutions include: reduction of clock frequency via parallelization; employment of low switching activity or non-glitching circuit blocks, and standby (sleep mode) power reduction circuitry [1].

In general, digital IC designers do not want to sacrifice circuit performance (i.e., speed) while reducing power consumption. Although the decrease in gate oxide thickness in scaled-down technologies helps in increasing the drive current, I_{on}, the gate oxide thickness is limited to 40-45 Å due to tunneling and reliability constraints [2]. I_{on} can be also increased via effective channel length reduction but this results in increased variability as will shown later. Lowering threshold voltage, V_{th}, can be an efficient method for reducing the delays in digital IC's. However, it leads to the increase in leakage currents, I_{off}, and thus the increase in the static power dissipation, P_{leak}, which is undesirable especially for the battery-operated equipment in the standby mode. If this leakage power constraint is critical, V_{th} must remain constant while scaling down V_{DD}. This will, however, introduce a severe penalty in speed. Hence, to achieve an optimal trade-off between IC performance (speed) and total power dissipation (the sum of P_{charge}, P_{leak} and the short circuit power dissipation component P_{sc}), a number of factors ranging from architectural/circuit solutions, choice of supply voltage, to the choice of technology and device parameters must be taken into account.

The possible technologies for low power IC's include: scaled-down twin-tub bulk CMOS, triple-well bulk CMOS and Thin Film Silicon-On-Insulator (TFSOI) technologies. The key parameters in the twin-tub CMOS technology are the substrate/channel doping and LDD resistance. With additional threshold adjust implant there is also a possibility of two devices per type with different threshold voltage val-

ISLPED 1996 Monterey CA USA
0-7803-3571-8/96/$5.00 © 1996

ues (high and low). This has been very successfully explored in the CMOS DSP chip for mobile communication applications [3]. The triple-well technology is ideally suited for the variable threshold voltage/multiple threshold voltage schemes essential to reduce power consumption in the standby/sleep mode of operation. Moreover, the substrate bias can be used to compensate for V_{th} fluctuations in the manufacturing process. This is accomplished with negligible overhead in speed and area, and with less than 5% increase in cost and turnaround time [4]. Finally, the TFSOI technology, due to inherently low junction capacitances and small body effect, can achieve 2x increase in performance for identical layout and design rules as bulk CMOS [5].

The choice of technology and device parameter optimization must be ultimately based on manufacturability. This is especially important for low voltage IC's where the process fluctuations are relatively more important (e.g., variations in V_{th} will cause significant variations in the worst case values of the I_{on} currents).

At present, 0.5µm bulk CMOS technology is the workhorse in volume production, while 0.35µm technology is in early production stages. Variability in these two technology generations is a manufacturability concern. This variability is caused by three main factors: critical dimension variations, channel doping fluctuations and oxide thickness nonuniformity. Their relative importance will increase further in the 0.25µm technology which is now in the development/pilot production phase. The above factors contribute to the IC performance variations and must be taken into account in IC design optimization.

For digital IC's, the interchip (within wafer) variations are of key importance although we have already observed gradients in parameter mismatches with large chips that cannot be neglected in IC performance evaluation/optimization. Analog IC designers are additionally concerned about local mismatch since many basic analog circuit blocks rely on extremely precise matching between device parameters.

In this paper, we will address these manufacturability issues. We will demonstrate the capabilities of several technologies (0.5µm and 0.35µm twin-tub CMOS, 0.6µm triple-well CMOS and 0.18µm TFSOI technologies). We will present the effects of scaling down supply voltage on device parameters and IC performance. We will also report the results of statistical characterization of these processes. We will pay special attention to the matching of the device parameters (both global and local). Finally we will present digital and analog designer perspectives on the effects of process fluctuations on the design of low-power analog IC's in the state-of-the-art CMOS technologies.

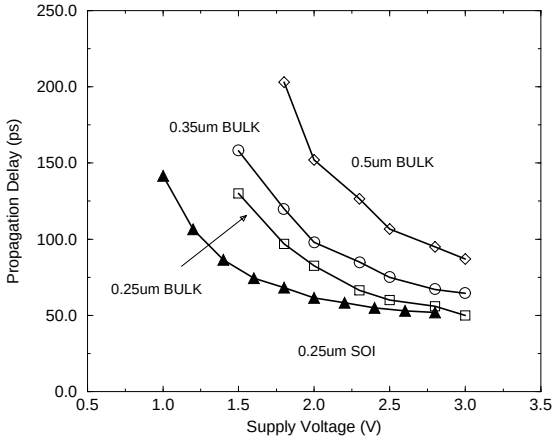

Fig. 1 Propagation delay vs. supply voltage

Technology Capabilities

Typical values of key device parameters (V_{th}, I_{on}, I_{off}) for minimum size devices in four different technologies are shown in Table 1.

The values for V_{th} have been extracted with the device in triode region (V_{ds} = 0.1 V) by extrapolating V_{gs} from the region of maximum slope of the I-V characteristic.

Technology	0.35µm bulk	0.5µm bulk	0.6µm triple-well	0.18µm TFSOI
L (µm)	0.35	0.5	0.6	0.18
V_{tn} (mV)	614	569	975	500
V_{tp} (mV)	555	649	958	500
$I_{on,n}$ (µA/µm)	550	330	280	250
$I_{on,p}$ (µA/µm)	250	150	180	126
$I_{off,n}$ (pA/µm))	1	1	N/A	10
$I_{off,p}$ (pA/µm)	1	1	N/A	2

Table 1: Typical device parameter values

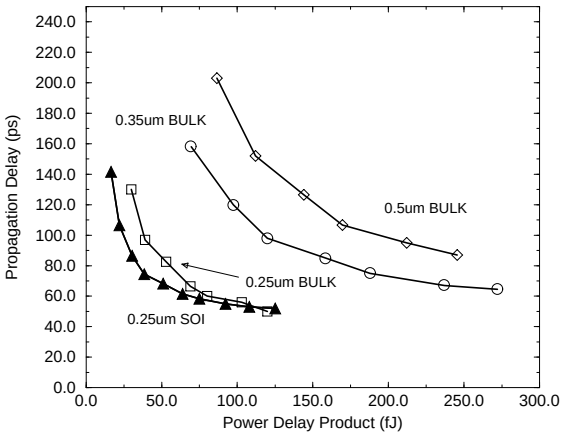

Fig. 2 Delay vs. powerdelay product

The I_{on} values are measured at 25 ^{o}C with V_{ds} and V_{gs} at the typical maximum supply voltages, i.e. 3.3V for the bulk CMOS processes, 3V for the triple-well and 1.5V for the TFSOI technology. Please note that all the reported I_{on} values are normalized to transistor width.

Although SOI is very attractive because of the lower threshold voltage and higher drive current for very low voltages, scaled down CMOS bulk processes appear to be still very efficient for values of the power supply above 2V [6]. Furthermore, their capability to supply higher drive current will increase with future generations as the gate oxide thickness is reduced.

Fig. 1 compares the propagation delay as a function of the power supply for an SOI technology and three CMOS bulk processes. This comparison has been made from ring oscillator data with the load dominated by the gates. For power supply greater than 2V, the delay is almost the same for the two families, but for supply voltage significantly lower than 2V, SOI delay is reduced by a factor of two [7].

This fact is also confirmed by Fig. 2 in which the relationship between gate delay vs. power-delay product is plotted from the ring oscillator data. For a given target delay, the power consumption of SOI is lower than that of CMOS by up to a factor of two. Nevertheless, as mentioned above, bulk technology will still dominate the high volume production in the near future.

The primary source of power consumption in digital blocks is usually due to capacitance charging/discharging:

$$P_{charge} = \frac{1}{2}(CV_{DD}^2) f_{ck} \alpha \qquad (1)$$

where f_{ck} is the clock frequency and α is the activity rate [8]. As shown in equation (1) the most straightforward way of minimizing the switching component of power is by reducing the supply voltage value.

Unfortunately, this also decreases the speed of the cells, as shown in Fig. 1 and Table 2 where the key performance parameters of these technologies from the low power design perspective are shown. Note that the normalized P_{charge} changes identically between 0.5µm and 0.35µm technology since the ratio of power dissipation for different supply voltages does not depend on load capacitance. If we are to compare the nominal values of power dissipation between 0.5µm and 0.35µm technologies, the ratio would be affected by the typical load capacitance ratio (e.g., if we assume a fan out of 3 and 100µm of interconnect as the typical loading we would obtain C_{load} of 156fF for 0.5µm technology and 135fF for 0.35µm technology). Hence, it is clear that the scaling of P_{charge} (or, more precisely, energy) is predominantly a function of V_{DD}^2 and not a function of minimum channel length. In addition to delay and power dissipation component values, we also present the inverse subthreshold slope which is defined as the V_{gs} required to increase the drain current by a factor of ten. The reported values are normalized with respect to the value computed at 5V for a fixed fan-out (which is assumed to be dominated by interconnect).

Table 2 shows that, for the same V_{th}, scaling the supply voltage leads to a very significant reduction in the power dissipation components but also to a penalty in terms of speed.

Technology	0.5µm bulk				0.35µm bulk			
Supply voltage	5 V	3.3 V	2.5 V	1.8 V	5 V	3.3 V	2.5 V	1.8 V
Delay	1	1.25	1.6	2.4	1	1.22	1.51	2.15
P_{sc}	1	0.34	0.168	0.08	1	0.46	0.168	0.078
P_{leak}	1	0.55	0.41	0.28	1	0.6	0.47	0.35
P_{charge}	1	0.44	0.25	0.1	1	0.44	0.25	0.1
Inverse Sub. slope	1	2.15	3.07	4.09	1	1.4	5.44	11.05

Table 2: Performance of bulk CMOS technologies vs. power supply (normalized values)

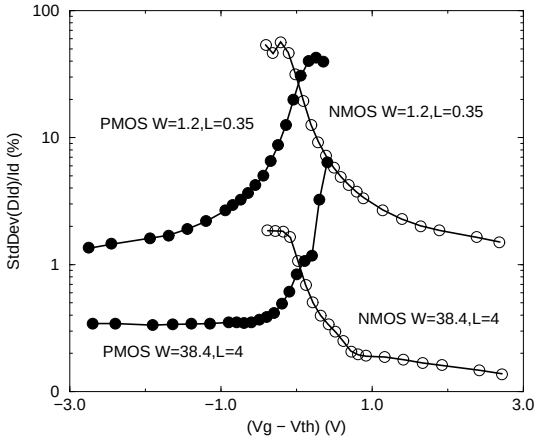

Fig. 3 Drain current mismatch as a function of (Vgs-V_{th})

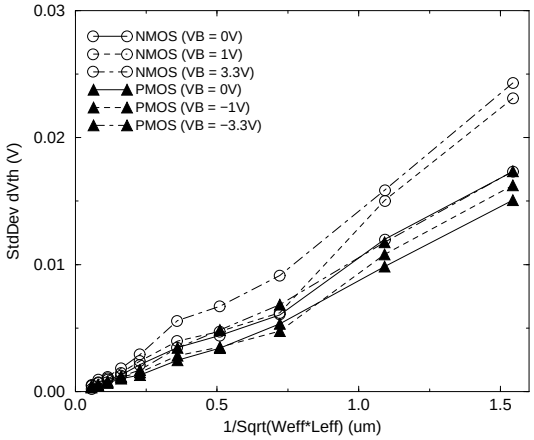

Fig. 4 Threshold voltage mismatch vs. 1/(effective gate area)

Statistical characterization

Technology scaling for performance improvement has to be traded off with process manufacturability, an operation which can be quantified as the amount of variability introduced during the fabrication process.

Table 3 shows the spreads, at wafer level, for some of the key parameters of the four technologies under consideration for the minimum size in each technology. The values are reported as a ratio of the standard deviation, σ, to the mean value, μ, for each parameter. It is clear that scaled down technologies carry a higher percentage of variability. At present, the advantages of high performance provided by TFSOI are reduced by the significant variability of device parameters.

Improvements in technology can be achieved only by identifying the process parameters which contribute substantially to the overall variability and the interactions between them. The increase in the parameter variability with the reduction of the minimum device size is consistent with the results from literature [9] where the critical dimension variations are reported to be the most important contributor to the overall variability along with other factors, such as channel doping and oxide thickness fluctuations.

To extract these components, sensitivity analysis followed by the analysis of variance (ANOVA) should be used.

Global variations (inter-die), which are significant across the whole wafer, and local mismatches (intra-die), which are relevant within the single die must be characterized and modeled.

As pointed out in the introduction, a precise characterization of global variations is critical to digital design, where both interconnect and gate variabilities are heavily affected by these fluctuations. The presence of process gradients across the wafer heavily affects inter-chip variations but can be accurately predicted because it is systematic in nature [10]. Furthermore, it has been reported [9] that inter-chip variations account for at least 2/3 of the total wafer variance. Similarly, the accuracy in the characterization of local mismatches can be drastically improved by extracting, from the total variance, the systematic part [11].

As will be shown later, local device mismatches are, in general, more critical in analog applications [12], and in low voltage/low power design, the concern for this kind of variability is even more critical. Lower power supply voltages imply a reduction in the value of (V_{gs} - V_{th}) which results in

σ/μ (%)	0.5μm bulk	0.6μm triple-well	0.35μm bulk	0.18μm TFSOI
V_{tn}	0.45	1.3	2.0	13.48
V_{tp}	0.526	0.96	2.1	22.48
$g_{max,n}$	1.5	0.3	N/A	N/A
$g_{max,p}$	0.71	2.3	N/A	N/A
$I_{on,n}$	0.551	2.0	2.9	N/A
$I_{on,p}$	1.031	3.0	N/A	N/A

Table 3: Device parameter comparison: wafer spreads

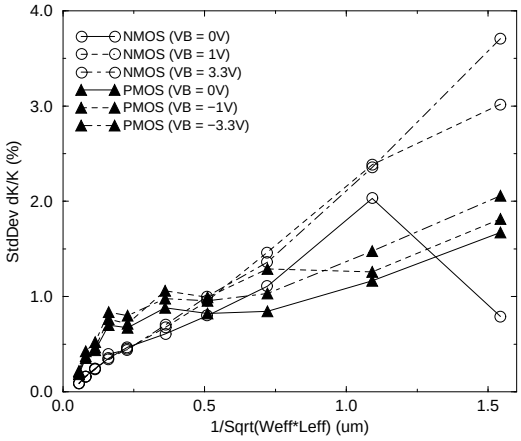

Fig. 5 Gain factor mismatch vs. 1/(effective gate area)

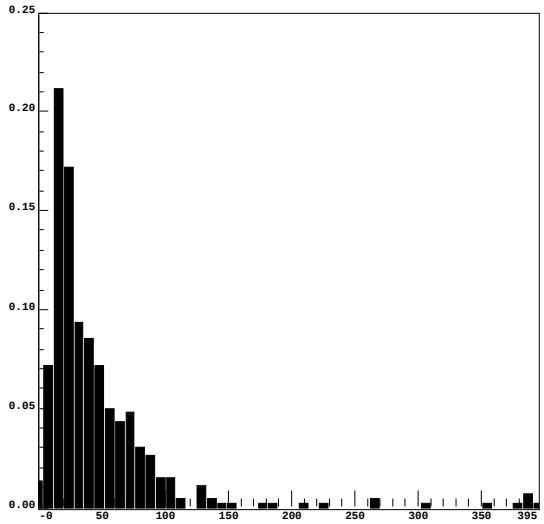

Fig. 6 Distribution of *K*

increased variability as suggested by the following expression for the drain current variance [13]

$$\frac{\sigma^2_{\Delta I_D}}{\overline{I_D}^2} = \frac{\sigma^2_{\beta}}{\overline{\beta}^2} + \frac{4\sigma^2}{(V_{gs} - \overline{V}_{th})^2} \qquad (2)$$

The data from Fig. 3, for a 0.35µm CMOS bulk process and extracted from a population of more than 400 dice, shows that, in case of minimum sized devices, the global current mismatch, given as the ratio $\sigma_{\Delta I_D}/I_D$, increases up to a factor of 35 when the input voltage is decreased from 3.3V down to 0.2V and as the device is driven from strong inversion down into deep subthreshold region. Clearly, the reduced swing of the input signal typical of low voltage applications, amplifies the effect of current mismatch.

This result is significant because it provides the warning to the designer that, although the mismatch in threshold voltage and gain factor can appear to be very good, the effect on the drain current mismatch can be still very strong. Fig. 4 shows the standard deviation of V_{th} versus the inverse of square root of effective channel area for NMOS and PMOS devices for three different values of the bulk bias. For this 0.35µm bulk technology, threshold voltage mismatch can be as good as 2.8% for NMOS and 2.5% for PMOS at minimum size (V_B = 0V) meanwhile, as shown in Fig. 5, gain factor mismatch is smaller, by a factor of two, for the same device size and bias condition. However, the difference in these two parameters is reduced as the back bias is increased.

The manufacturability is likely to become even worse with additional reduction of minimum size and device spacing. New sources of variability (negligible in previous technologies) will increase the local component of the total variance and the following effects will become dominant: over/under etching of small geometries, proximity effects [14], doping fluctuations along the channel [15], lateral diffusion of dopants between adjacent high-energy implanted wells [16]. They will have a dominant effect on local mismatch and should be considered in the standard characterization procedure.

Due to the phenomena described above, the systematic contribution to local mismatch increases significantly. It is necessary to design special purpose test structures to isolate these effects and extract the systematic component of local mismatch. A set of test structures should include structures to measure sheet resistance, linewidth (with and without dummy neighbors), doping and oxide thickness variations.

The digital designer's perspective

Process variability has been long considered an analog design problem only. However, as the minimum size of the CMOS device decreases to deep submicron, the effect of process variability has an increasing impact on the performance of digital IC's. Below we present the effect of process variations on power consumption of digital circuits.

In standard static CMOS, for minimum feature size below 0.5µm, most of the power is consumed by switching the load capacitance. The capacitance and resistance of interconnection lines, however, can be controlled quite accurately, (typically within ±5%). Moreover the switching component of the power consumption can be considered as the "useful" part of the total power dissipated by a logic circuit, as opposed to the short circuit and leakage components, since it is the energy necessary to perform the actual computation for which the circuit has been designed.

However, as we mentioned in the introduction, there exist other circuit solutions to explore low voltage/low power trade-offs such as, for example, multiple threshold or quadrail circuits [17]. In these cases the combination of short circuit and leakage power may be more significant, therefore we present below a brief discussion of the sensitivity of

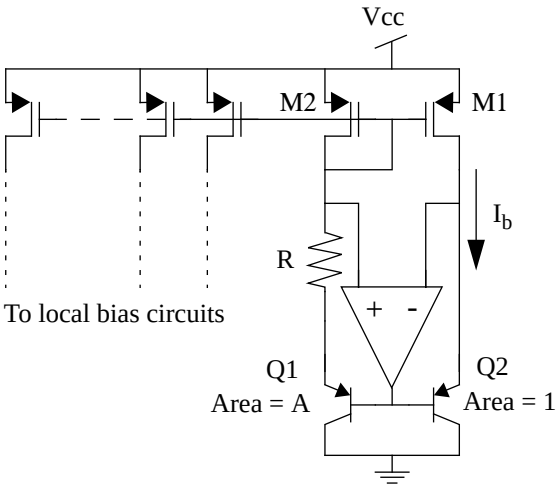

Fig. 7 PTAT bias circuit

these power components to process variations.

The impact of process variations on the short circuit component of the power consumption, P_{sc}, can be quite significant. In fact, this component is affected directly, through the shift of the logic threshold of the pull-up with respect to the pull-down stack of a CMOS cell, and indirectly, through the increase of the transition time of the switching events. The direct impact of the process variability on the short circuit component is usually quite moderate (e.g. $\Delta P_{sc} < 10\%$), whereas the indirect component can be as large as ±30% with respect to typical. We have characterized the effect of this indirect mechanism on the blocks of a standard cell library in a 0.5µm CMOS technology. In order to do so, we have initially characterized the parameters of a linear equation that relates P_{sc} to the output transition time:

$$P_{sc} = K\left(\frac{\tau_{rf} - \mu(\tau_{rf})}{\mu(\tau_{rf})}\right) + P_0 \qquad (3)$$

where τ_{rf} is the actual value and $\mu(\tau_{rf})$ the mean value of either the rise or fall time.

In equation (3), P_0 represents the short circuit component of the power dissipation for a typical process, and the first term accounts for the additional power dissipated because of variations in the output transition time. The amount of extra power is then weighted by a factor K.

Then, for each cell in the library, we have extracted the worst case (at ±3σ) output transition time from a Monte-Carlo simulation. The distribution of K across the different cells in the library is shown in Fig. 6. It can be seen that, even if generally the value of this coefficient is approximately 50, it may assume values as large as several hundreds for a simple inverter. Thus the total variation in the short circuit power component for 3σ variation of the output transition time can increase up to 30%.

Although the direct impact of process variations on the leakage component of power consumption is typically low, the process variability affects the subthreshold slope. However, leakage is still a problem for the battery operated IC's and it may be also quite significant in the solutions with greatly reduced threshold voltage.

From the digital designer viewpoint, the process variability limits the possible reduction of V_{th} necessary to maintain a sufficient worst-case noise margin.

Recently digital designers have started to employ analog style differential architectures (e.g., CVSL [18]) to low power design to minimize noise and cross-talk. These low voltage swing technologies are extremely sensitive to the local mismatch which increases the importance of intra-die variations.

The analog designer's perspective

Most CMOS analog IC's need accurate control of the transistor bias currents. In fact, excessive variations of these currents due to manufacturing tend to sacrifice power dissipation at the high extreme of bias current, and speed at the lower extreme, while dependence of bias currents on supply voltage result in poor power supply rejection. Accurate biasing can be achieved by a central (master) bias circuit which generates a multiplicity of currents and distributes them around the chip. These currents are used by local (slave) bias circuits which in turn produce the required bias voltages or currents for the nearby analog circuits. Another advantage of this choice is that a complete chip power-down can be simply achieved by turning off the central bias circuit.

The "Proportional To Absolute Temperature" (PTAT), and the "Proportional To Square Root of Absolute Temperature" (PTSRAT) are central bias circuits most commonly used.

These absolute temperature coefficients for reference currents are chosen by designers to compensate for similar but opposite coefficients of the MOS device parameters, keeping the performance of the complete circuit almost independent from the operating temperature. Therefore, the reference current, I_b, dependence from process parameters is unwelcome, especially in the case of low power IC's, because it forces analog designers to choose a typical value for the central bias current much higher than the desired minimum to assure a good yield during volume production of the chip

Very simplified schematics of PTAT and PTSRAT circuits in a N-well CMOS technology are shown in Figs. 7 and 8, respectively, where I_b is the reference current generated by central bias, k is Boltzmann's constant, T is the absolute temperature, µ and C_{ox} are MOS channel mobility and oxide specific capacitance, W/L is the MOS width to length factor, R is a poly or diffused resistor, A is the emitter area ratio between two vertical "parasitic" BJT's which are always present in a CMOS process, B is the ratio between

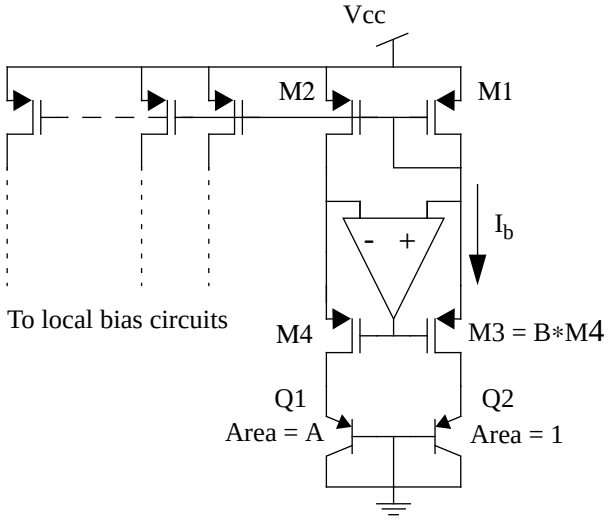

Fig. 8 PTSRAT bias circuit

the widths of M3 and M4, and V_{os} is the amplifier offset voltage in Fig.7 or the threshold mismatch between M3 and M4 in Fig.8.
For the PTAT bias:

$$I_b = \frac{1}{R} \cdot \left(\frac{kT}{q} \ln A + V_{os} \right). \qquad (4)$$

Thus, if the resistor temperature coefficient is negligible, the bias current is linearly related to absolute temperature. Considering the tolerance on poly resistor ($\pm 3\sigma = \pm 15\%$) and practical V_{os} values ($\pm 3\sigma = \pm 10$mV) as independent random variables, the $\pm 3\sigma$ bounds for bias current are -21% and +24%.
For the PTSRAT bias:

$$I_b = \frac{\mu C_{ox} (W/L)_4}{2\left(1 - B^{-0.5}\right)^2} \cdot \left(\frac{kT}{q} \ln A + V_{os} \right)^2. \qquad (5)$$

Since the channel mobility has an approximate $T^{-1.5}$ temperature dependence, the bias current is proportional to the square root of absolute temperature.
Again, assuming the tolerance on MOS channel mobility and oxide thickness ($\pm 3\sigma = \pm 12\%$) and practical threshold mismatch (e.g., for relatively large devices $\pm 3\sigma = \pm 8$mV) as unrelated processes, the $\pm 3\sigma$ bounds for bias current are -28% and +31%.

Conclusions

In this paper we have examined the manufacturability of four types of technology suitable for low voltage/low power applications. We have argued that the proper trade-off to be considered while lowering the supply voltage has to involve speed of the gates and the total power dissipation.
We have demonstrated that the manufacturability is becoming a crucial factor in achieving this trade off due to both global and local variations. Proper statistical characterization of process must be based on special purpose test structures to identify main sources of device parameter variations.
Finally, we have shown that is not sufficient to examine variability in device parameter only, since variations (both global and local) may be significantly amplified at the level of device currents or IC block performances.
In summary, a new comprehensive approach to assess the manufacturability of next generation low power circuits must be developed before the circuit designers (especially analog) can take full advantage of scaled down technology capabilities. It is especially important to zoom in on the second order effects associated with local mismatches.

Acknowledgments

The authors would like to thank David Guillou and Mukund Sivaraman for the continuous support and valuable discussions, Paola Zabberoni and Olivier Roux dit Buisson for their contributions to the experimental part of this work. We also appreciate the help of Jean-Luc Pelloie from LETI in providing us with experimental data for TFSOI devices.

References

[1] T. Andoh et *al.*, “Design Methodology for Low-Voltage MOSFET’s”, *Proc. IEDM*, 1994, pp. 79-82.
[2] R.H. Yan et *al.*, “Reducing Operating Voltage from 3, 2 to 1V and Below - challenges and guidelines for possible solutions”, *Proc. IEDM*, 1995, pp. 55-58.
[3] Mutoh et *al.*, “A 1V Multi-Threshold Voltage CMOS DSP with an Efficient Power Managment Technique for Mobile Phone Application”, *1996 ISSCC Digest*, pp. 168-169.
[4] T. Kuroda et *al.*, “A 0.9V 150MHz 10mV 4mm^2 2-D Discrete Cosine Transform Core Processor with Variable-Threshold-Voltage Scheme”, *1996 ISSCC Digest*, pp. 166-167.
[5] W.M. Huang et *al.*, “TFSOI CMOS Technology for Sub-1V Microcontroller Circuits”, *Proc. IEDM*, 1995, pp. 59-62.
[6] Z. Chen et *al.*, “CMOS Technology Scaling for Low Voltage Low Power Applications”, *IEEE Symp. on Low Power El.*, 1994, pp. 63-66.
[7] Jean-Luc Pelloie, LETI, Private Communication.
[8] A.P. Chandrakasan, R.W. Brodersen, “Low Power Digital CMOS Design”, Kluwer Academic Publishers, 1995.
[9] Z. Chen et *al.*, “Optimization of Quarter Micron MOSFETs for Low Voltage/Low Power Applications”, *Proc. IEDM*, 1995, pp. 63-66.
[10] J. Kibarian, “Statistical Diagnosis of IC Process Faults”, Ph.D. Thesis, Dec 1980.
[11] E. Felt et *al.*, “Measurement and Modeling of MOS

Transistor Current Mismatch in Analog IC's", *Proc. ACM*, 1994, pp. 272-277.
[12] P. Kinget et *al*., "Impact of Transistor Mismatch on the Speed-Accuracy-Power Trade-off Analog CMOS Circuits", *IEEE Custom Integrated Circuit Conf*., 1996, pp. 333-336.
[13] K.R. Lakshmikumar et *al*., "Characterization and Modeling of Matching in MOS Transistor for Precision Analog Design", *IEEE Journal of Solid State Circuits*, vol SC-21, Dec 1986, pp. 1057-1066.
[14] M. Eisele et *al*., "Intra-Die Device Parameter Variations and Their Impact on Digital CMOS Gates at Low Supply Voltages", *Proc. IEDM*, 1995, pp. 67-70.
[15] T. Mizuno et *al*. "Experimental Study of Threshold Voltage Fluctuation Due to Statistical Variation of Channel Dopant Number in MOSFET's", *IEEE Trans. Electron Devices*, vol. 41, no. 11, Nov 1994, pp. 2216-2221.
[16] H. Takatsuta et *al*. "Influence of Tilted High-Energy Ion-Implantation upon Scaled CMOS Structure", *Proc. ICMTS*, vol. 8, Mar 1995, pp. 274-251.
[17] R.K. Krishnamutrhy et *al*., "Static Power Driven Voltage Scaling and Delay Driven Buffer Sizing in Mixed Swing Quadrail for sub-1V I/O Swings", *Proc. ISLPED*, 1996.
[18] L.G. Heller et *al*., "Cascade Voltage Switch Logic: a Differential CMOS Logic Family", *Proc. ISSCC*, Feb 1984, pp. 16-17.