Evolvable Hardware
and its industrial applications

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Contents of this talk

• Basic Concept of Evolvable Hardware

• Digital Hardware Evolution
  – Gate-level Evolvable Hardware
    • EMG prosthetic hand
    • Clock-timing adjustment (Post-fablication adjustment)
    • Data compression for print image data
  – Function-level Evolvable Hardware
    • Autonomously reconfigurable neural network chip

• Analogue Hardware Evolution
  • Analogue EHW chip for cellular phones

• Mechanical Hardware Evolution
  – Evolvable Femto-second Laser System
  – Evolvable Interferometer
  – Evolutionary fiber alignment
Evolvable Hardware =

Evolutionary Computation +

Reconfigurable Hardware
**Evolvable Hardware (EHW)**

<table>
<thead>
<tr>
<th>Conventional Hardware</th>
<th>Evolvable Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification fixed</td>
<td>Spec. changes dynamically</td>
</tr>
<tr>
<td>Architecture fixed</td>
<td>Architecture changeable  =&gt; Hardware circuit is autonomously synthesized.</td>
</tr>
</tbody>
</table>
PLA (Programmable Logic Array)

Input

Output

Chromosome

\[ Y_0 = \overline{X_0 + X_0 \overline{1} X_1 X_2 X_3} \]

\[ Y_1 = X_0 \overline{1} X_1 X_2 X_3 + X_0 X_3 \]

0100000010 1001011010 1001100101 1000000101
GA (Genetic Algorithm)

Bio-inspired robust search and adaptation

- **Selection**
  - select high-fitness chromosomes
- **Crossover**
  - exchange of chromosomes
- **Mutation**
  - change of chromosomes
Basic idea of Evolvable Hardware

- EHW = Genetic Algorithms + Programmable Logic
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Digital Hardware Evolution

• Chromosome determines:
  – types of hardware components
  – interconnections among hardware components

• Gate-level hardware evolution
  – Hardware components are primitive gates such as AND-gate and OR-gate.

• Function-level hardware evolution
  – Hardware components are higher hardware functions such as adders and multipliers.
EHW chip

Prosthetic Hand

EHW chip
Problems in conventional EHW

Needs a PC to execute GA

Fitness evaluation and GA by software

→ Large Size

→ Slow Speed

PC

GA software

Programmable Logic Device
Gate Level EHW Chip

- Integration of GA hardware and a PLA on a single LSI chip.

- Compact & Fast
Myoelectric-controlled prosthetic-hand

• Myoelectric signals
  – Generated from muscular activation.
  – Detected on the surface of the skin by using surface electrode.

• Myoelectric-controlled prosthetic-hand
  – Controlled by myoelectric signals generated from remnant muscles.
Myoelectric signals are detected on the surface of the skin by using surface electrode (sensor).
An example of myoelectric signal patterns
Problems in myoelectric-controllers

• Problem
  – Individuality
    • Characteristics of myoelectric signals differ among individual persons.
    • Difficult to make specification of pattern classification circuit in advance.

• Our solution (1998--)
  – Evolvable hardware
    • An evolvable hardware chip.
    • Programmable hardware + Genetic algorithm
EHW chip architecture

- GA dedicated hardware
- Reconfigurable Hardware (PLA)
- Memory (training data, chromosome)
- Control logic
- Interface
EHW chip (version 1)
Gate-Level EHW chip

- Package: 144pins QFP, 20x20mm, Cell base LSI.
- Circuit size: about 80,000 gates.
- Clock frequency: 33MHz.
• Steady state GA and uniform crossover are used.
• There are new options for GA. (GRGA, on-line learning etc.)
• Execution time: 95 us / (chromosome evaluation)
  - 40 times faster than software on a PC (1.2GHz).
There are two PLAs for parallel evaluation of two circuits.
I/O: 12bit input / 4bit output, or 8bit input / 8bit output.
Product term line number: 32 in one PLA.
Performance evaluation

<table>
<thead>
<tr>
<th>Function</th>
<th>EHW chip (us)</th>
<th>Program (us)</th>
<th>(Program)/(EHW chip)</th>
</tr>
</thead>
<tbody>
<tr>
<td>One evaluation</td>
<td>94.8</td>
<td>3670</td>
<td>38.7</td>
</tr>
<tr>
<td>Crossover &amp; mutation</td>
<td>12.6</td>
<td>78.9</td>
<td>6.3</td>
</tr>
<tr>
<td>Fitness calculation</td>
<td>68.2</td>
<td>3560</td>
<td>52.2</td>
</tr>
<tr>
<td>Comparison of fitness values</td>
<td>0.03</td>
<td>0.15</td>
<td>5.0</td>
</tr>
<tr>
<td>PLA execution</td>
<td>0.03</td>
<td>13.42</td>
<td>447.3</td>
</tr>
</tbody>
</table>

- Comparison of the execution time with a GA program on a PC (AMD Athlon CPU 1.2GHz).
  => EHW chip: 38.7 times faster than the program.
    - PLA execution: 447 times faster than the program.
The hand controller with the EHW chip

myoelectric signal

Hand open
Hand close
Wrist flexion
Wrist extension

The EHW chip controller
Multi-functional myoelectric controlled artificial hand.

**Mechanical specifications**

<table>
<thead>
<tr>
<th>Functions</th>
<th>Hand open-close</th>
<th>Wrist flex-extend</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>almost same as adult human hands</td>
<td></td>
</tr>
<tr>
<td>Weight</td>
<td>about 400g</td>
<td></td>
</tr>
<tr>
<td>Motor</td>
<td>DC motor X 2</td>
<td></td>
</tr>
<tr>
<td>Battery</td>
<td>rechargeable: 12V</td>
<td></td>
</tr>
</tbody>
</table>
Multi-functional myoelectric controlled artificial hand.

User's merit of multi-functional hand.

- Natural and easy approach to the object.

Without wrist flexion. (Conventional hand)  
With wrist flexion.
Clinical evaluation.
Clock Timing Adjustment
Background

Beyond 90nm, operational yield rate will be degraded due to process variation.

=> the limit of design capability
=> strong need for post-fabrication LSI adjustment.

Trend beyond 90 nm:
from inter-chip variation to intra-chip variation

The same logical design no more guarantees the same performance.
Our approach: Post-fabrication LSI adjustment

Circuit design including adjustment circuits
+
Fast adjustment software

Fast adjustment software:

Genetic Algorithm (GA) in Artificial Intelligence

GA can determine quickly optimal values of many circuit parameters that affects LSI performance and operational yield rate.
Genetic algorithm

Genetic Algorithm (GA): A quick and robust search algorithm

step 1. Encode multiple circuit parameters into single chromosome.
step 2. Define an evaluation function $F$ that decides fitness of chromosomes
   $\Rightarrow$ decision whether a chromosome has good circuit parameters or not.
step 3. Prepare multiple chromosomes, then generate better chromosomes with genetic
   operations (e.g. cross-over, mutation) until good circuit parameters are found.
Outline

• Post-fabrication adjustment for Digital LSI
  – Background & advantages
  – Developed LSIs
  – Results (Three Advantages)
    1. Speed-up of Clock Frequency
    2. Reduction of Power Dissipation
    3. Reduction of Design Time
Background & Advantages

- Beyond 90nm, clock skew cannot be avoided only by design due to process variation
- Post-Fabrication clock timing adjustment with Genetic Algorithm
- Two 1GHz LSIs and a design experiment demonstrate three advantages:
  1. Speed-up of Clock Frequency (+25% max)
  2. Reduction of Power Dissipation (-54% max)
  3. Reduction of Design Time (-21% max)
Post-Fabrication Clock Timing Adjustment

1. Design
2. Fabrication
3. Adjustment
4. Shipping

- LSI Design
- Programmable Delay Circuits
- GA-based Adjustment Software
- LSI Tester

• Low operating yield
• Considerable power dissipation
• Design clock speed

• Higher operating yield
• Less power dissipation
• Faster clock speed than designed
Hierarchical Application of Clock Timing Adjustment

Clock Domain or Circuit Block

Clock Tree

Circuit Sub-Block or Flip-Flop

Clock adjustment required

Clock adjustment not required

Clock Driver

Clock not required

Clock adjustment for INTER-DOMAIN skew

Clock adjustment for INTRA-DOMAIN skew

Programmable Delay Circuit
Clock Skew

(a) Time t=0

Input Data

\[ \begin{align*}
\text{Register 1} & : 5 \\
\text{Circuit A} & : +1 \\
\text{Register 2} & : \begin{cases} +1 \text{ if clock skew occurs} \\
\text{unknown} \text{ otherwise} \end{cases} \\
\text{Circuit B} & : +1 \\
\text{Register 3} & : \end{align*} \]

Clock Signal

(b) Time t=T

When clock signal arrives earlier than specifications because of "clock skew", Register 2 will hold a wrong value.

Clock Signal
Clock Timing Adjustment for Solving the issues of "Clock Skew"

(a) Time $t=0$

Input Data

5 → 5 → +1 → +1 → Register 1 → Circuit A → Register 2 → Circuit B → Register 3

Clock Signal

(b) Time $t=T$

Register 1 → +1 → Circuit A → 6 → +1 → Register 2 → Circuit B → Register 3

Clock Signal

Programmable Delay Circuit
Insertion of Programmable Delay Circuits

Genetic Algorithms can find optimal delay values for a lot of delay circuits.

Delay Values must be globally optimized!
**Programmable Delay Circuit**

- **Delay Generator**
  - Clock In
  - Clock Out
  - \( V_{adj} \) (Controlling Voltage)

- **Register**

- **DAC**

---

**Controlling Voltage \( (V_{adj}) \) vs Delay and Delay Steps**

- Delay [ns] vs Delay Step [ns]
- Delay Steps
- 30ps

- "Delay Steps" are calculated as differences between adjacent delay plots.

- **DAC (Digital-Analog Converter)**
  - Die Photograph

- **Die Photograph**

- **0.18um, CMOS process**
- **18Tr: Delay Generator + DAC**
- **Some Delay Steps are less than 30ps**

---
Test Chip No.2: Multiplier and Memory Test Pattern Generator

0.13um, CMOS process, Design for 1GHz(typ),
Using the "Programmable Delay Circuits"
Three Advantages of GA-based adjustment

1. Speed-up of Clock Frequency (+25%)

2. Reduction of Power Dissipation (-54%)

3. Reduction of Design Time (-21%)
Advantage No.1: Clock Frequency Speed-up

LSI: Designed at 1000ps (=1GHz) period

Data Input -> Register 800ps -> Circuit 1000ps -> Circuit 600ps -> Register -> Data Output

Clock Input 1000ps (=1.0GHz) period

LSI: Clock period is enhanced to 800ps (=1.25GHz)

Data Input -> Register 800ps -> Circuit 1000ps -> Circuit 600ps -> Register 0

Clock Input 800ps (=1.25GHz) period

25% Enhancement of Clock Frequency (1000/800=1.25)

200ps delay inserted
Experiment Result:
Clock Frequency Speed-up

Each X point represents a unique chip

Operational clock frequency BEFORE adjustment

Operational clock frequency AFTER adjustment

Memory Test Pattern Generators

Multipliers

GA Details:
• Population: 50
• Termination: 20th Generation
• Selection: Tournament Selection
• Crossover: One-Point Crossover
• Crossover Rate: 1.0
• Mutation: Gaussian Mutation ($\sigma=1.0$)
• Mutation Rate: 1.0

25% increase over all the chips
Advantage No.2: Power Supply Voltage Reduction

LSI which operates at standard power supply voltage 1.2V

Data Input

Register

Circuit

Register

Circuit

Register

Circuit

Register

Circuit

Register

Circuit

Data Output

Clock Input

Lowering power supply voltage, from 1.2V to 0.8V

LSI which operates at lower power supply voltage 0.8V

Data Input

Register

Circuit

Register

Circuit

Register

Circuit

Register

Circuit

Register

Circuit

Data Output

Clock Input

Programmable Delay Circuit

Circuits which violate timing constraints
## Experiment Result:

**Power Supply Voltage Reduction**

Operational yield at each voltage and clock frequency, **BEFORE** adjustment

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>0.8V</th>
<th>0.9V</th>
<th>1.0V</th>
<th>1.1V</th>
<th>1.2V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.58GHz</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
</tr>
<tr>
<td>1.4GHz</td>
<td>0%</td>
<td>0%</td>
<td>20%</td>
<td>30%</td>
<td>40%</td>
</tr>
<tr>
<td>1.25GHz</td>
<td>0%</td>
<td>40%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
</tr>
<tr>
<td>1.0GHz</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
</tr>
</tbody>
</table>

Operational yield at each voltage and clock frequency, **AFTER** adjustment

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<th>Voltage (V)</th>
<th>0.8V</th>
<th>0.9V</th>
<th>1.0V</th>
<th>1.1V</th>
<th>1.2V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.58GHz</td>
<td>0%</td>
<td>0%</td>
<td>10%</td>
<td>20%</td>
<td>10%</td>
</tr>
<tr>
<td>1.4GHz</td>
<td>30%</td>
<td>60%</td>
<td>80%</td>
<td>100%</td>
<td>90%</td>
</tr>
<tr>
<td>1.25GHz</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
</tr>
<tr>
<td>1.0GHz</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
</tr>
</tbody>
</table>

**Clock Adjustment**

Voltage: 1.2V

0.8V & 1.25GHz

**Measured with the Memory-test-pattern Generators.**
Experiment Result:
Power Dissipation Reduction

Possible power reduction: 4/9

Sakurai's Formula for CMOS power dissipation [4]:

\[ P = \alpha \cdot f \cdot Vdd^2 + \beta \cdot Vdd \]

where

- \( Vdd \): Power supply voltage
- \( \alpha, \beta \): Almost constant
- \( f \): Clock frequency

Reduction of 2/3 in Vdd: 1.2V → 0.8V

Results: -75%!
Advantage No.3: Design Time Reduction

Target Design: DDR-SDRAM controller circuit

<table>
<thead>
<tr>
<th>Design Stage</th>
<th>Traditional *1</th>
<th>GA-based *1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function Design</td>
<td>12.0</td>
<td>1.5</td>
</tr>
<tr>
<td>Logic Design</td>
<td>30.0</td>
<td>30.0</td>
</tr>
<tr>
<td>Floor Planning</td>
<td>7.0</td>
<td>2.0</td>
</tr>
<tr>
<td>Verification (1)</td>
<td>5.0</td>
<td>5.0</td>
</tr>
<tr>
<td>Layout Design</td>
<td>7.0</td>
<td>1.5</td>
</tr>
<tr>
<td>Verification (2)</td>
<td>6.0</td>
<td>4.0</td>
</tr>
<tr>
<td>Library Design</td>
<td>42.0</td>
<td>42.0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>109.0</strong></td>
<td><strong>86.0</strong></td>
</tr>
</tbody>
</table>

*1 day·person

-21%
Overhead of the post-fabrication GA adjustment:

1. Area Overhead  4%

2. Time for Clock Timing Adjustment

<table>
<thead>
<tr>
<th>Operations</th>
<th>Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generation of Delay Setting and Test Data for Function Test</td>
<td>0.55</td>
</tr>
<tr>
<td>Write Data to Chip</td>
<td>0.02</td>
</tr>
<tr>
<td>Execution of Test</td>
<td>0.01</td>
</tr>
<tr>
<td>Read Results of Test from Chip</td>
<td>0.03</td>
</tr>
<tr>
<td>Calculation of Fitness</td>
<td>0.33</td>
</tr>
<tr>
<td><strong>Total Time</strong></td>
<td><strong>0.94</strong></td>
</tr>
</tbody>
</table>
Lossless compression method
for very high-resolution image data
Overview

- **Lossless** compression method bi-level image with high-resolution.

- Amendment to JBIG2 standard.
  
  (ISO/IEC JTC1/SC29/WG1 France meeting, 2003)
  
  – JBIG2 = **Joint Bi-level Image experts Group**, 2
    
    • International standard for bi-level image coding
    
    • ISO/IEC 14492 | ITU-T T.88

- Activity toward incorporating JBIG2-AMD2 datastream into TIFF/IT
  
  – TIFF/IT = **Tag Image File Format for Image Technology**
    
    • International standard of graphic data format for data exchange
    
    • ISO 12639
Digitalization of Workflow in Graphic-Arts Industry

**Conventional approach**

- Author
  - Edit
  - Composition
  - RIP
- Film
- Plate-making
- Plate
- Press
- Bookbinding

**Now and Future**

- Author
  - Edit
  - Composition
  - RIP
- CTP
- Plate
- Press
- Bookbinding
- DI Press
- eBook

**Huge costs for transport and storage**

**Deterioration in quality**

**Needs for skillful craftsman**

**Solution:**
- Data compression by AIST method
High-resolution Image for Graphic-Arts

Color Image

RIP
Raster Image Processor

Press

Graphic-Arts Image
- Bi-level
- Very-high resolution

High quality printed material
Lossless Compression of JBIG2

Less outputs for correct prediction

Accurate prediction leads efficient compression

Arithmetic Coder

Compressed data

Reference Pixels (16 bits) + Pixel to be coded (1bit)

Floating reference pixels

Reference Pixels

Pixel to be coded

256 pixels

128 lines
Principle of JBIG2-AMD2

Prediction Coding
Accuraxy of pixel prediction affects compression efficiency.

Halftone image with very high-resolution
Conventional methods achieve low prediction-hit rate.
⇒ Poor compression efficiency

JBIG2-AMD2
Extended template with many floating reference pixels
⇒ Improved compression efficiency
Strange structure: Shading is represented by size of dots, and Dots' size is represented by density of pixels.

=> Conventional lossless compression method cannot compress well
Limitation of JBIG2

Discovery by AIST:

• Too few floating reference pixels
  – Proposal to ISO: Enhancement of JBIG2
  – Extended template: Increased number of floating reference pixels from 4 to 12

• Large costs for template optimization
  – GA can quickly find the good template configuration for higher compression ratio
AIST method

Genetic Algorithm optimizes the template for the target image data to achieve the higher compression ratio.

Image Data

Codec of JBIG2-AMD2

Template Optimizer
Genetic Algorithm + Statistical approach

Template

Compressed Data

Compression ratio
Experimental Results

More floating reference pixels leads 30% better comp. efficiency.

- Limitation of JBIG2: Increased floating reference pixels
- Configuration of floating reference pixels
  => Artificial intelligence (AI) techniques
Performance 1 --Compression Ratio--

<table>
<thead>
<tr>
<th>Image</th>
<th>MMR(G4)</th>
<th>ZIP</th>
<th>JBIG2</th>
<th>JBIG2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>base</td>
<td>AMD2</td>
</tr>
<tr>
<td></td>
<td>Res.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCID#</td>
<td>Angle</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>1200</td>
<td>15</td>
<td>2.36</td>
<td>2.37</td>
<td>8.20</td>
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<tr>
<td></td>
<td>2400</td>
<td>3.59</td>
<td>2.74</td>
<td>10.80</td>
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<tr>
<td></td>
<td>3600</td>
<td>5.26</td>
<td>3.11</td>
<td>14.95</td>
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<tr>
<td>N5</td>
<td>1200</td>
<td>2.71</td>
<td>3.56</td>
<td>8.12</td>
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<td></td>
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<td>4.21</td>
<td>4.37</td>
<td>10.30</td>
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<td></td>
<td>3600</td>
<td>5.58</td>
<td>5.73</td>
<td>15.24</td>
</tr>
<tr>
<td>75</td>
<td>1200</td>
<td>2.14</td>
<td>2.44</td>
<td>9.04</td>
</tr>
<tr>
<td></td>
<td>2400</td>
<td>3.28</td>
<td>2.75</td>
<td>11.54</td>
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<tr>
<td></td>
<td>3600</td>
<td>4.14</td>
<td>2.92</td>
<td>15.47</td>
</tr>
<tr>
<td>N6</td>
<td>1200</td>
<td>2.53</td>
<td>4.64</td>
<td>10.59</td>
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<tr>
<td></td>
<td>2400</td>
<td>3.93</td>
<td>5.22</td>
<td>11.98</td>
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<td></td>
<td>3600</td>
<td>5.03</td>
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<td>75</td>
<td>1200</td>
<td>1.78</td>
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<td>2.66</td>
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<td>7.38</td>
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<tr>
<td></td>
<td>3600</td>
<td>3.32</td>
<td>2.77</td>
<td>10.88</td>
</tr>
<tr>
<td>N8</td>
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<td>3.49</td>
<td>7.19</td>
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<td>75</td>
<td>3.26</td>
<td>4.10</td>
<td>8.56</td>
</tr>
<tr>
<td></td>
<td>3600</td>
<td>4.06</td>
<td>5.44</td>
<td>13.19</td>
</tr>
</tbody>
</table>

- Compression Ratio = [Original size] / [Compressed size]
- Test data are created by RIPing images in SCID.
Performance 2 (European newspaper)

- 1270 dpi
- 17416 x 27958 pixels
- Approx. 58MB x (CMYK)

<table>
<thead>
<tr>
<th>Method</th>
<th>CR</th>
</tr>
</thead>
<tbody>
<tr>
<td>G4 Fax</td>
<td>27.67</td>
</tr>
<tr>
<td>JBIG1</td>
<td>41.54</td>
</tr>
<tr>
<td>This method</td>
<td>60.85</td>
</tr>
</tbody>
</table>

CR (Compression Ratio) = [Original size] / [Compressed size]
Performance 3 (Book page)

- 2400 dpi
- 17167 x 22100 pixels
- Approx. 45MB x 4 (CMYK)

<table>
<thead>
<tr>
<th>Method</th>
<th>CR</th>
</tr>
</thead>
<tbody>
<tr>
<td>LHA</td>
<td>28.3</td>
</tr>
<tr>
<td>TIFF (LZW)</td>
<td>17.9</td>
</tr>
<tr>
<td>This method</td>
<td>120.6</td>
</tr>
</tbody>
</table>

CR (Compression Ratio) =
[Original size] / [Compressed size]
Performance 4 (Leaflet)

- 2400 dpi
- 20400 x 28034 pixels
- Approx. 68MB x 4 (CMYK)

<table>
<thead>
<tr>
<th>Method</th>
<th>CR</th>
</tr>
</thead>
<tbody>
<tr>
<td>LHA</td>
<td>5.74</td>
</tr>
<tr>
<td>TIFF (LZW)</td>
<td>4.69</td>
</tr>
<tr>
<td>This method</td>
<td>16.86</td>
</tr>
</tbody>
</table>

CR (Compression Ratio) = [Original size] / [Compressed size]
Future Plans

• Standardization activity
  – TIFF/IT: Tag Image File Format for Image Technology (ISO 12639)
  – NWI proposal at ISO TC130/WG2 meeting
    • NWI = New Work Item

• R&D of graphic-arts technology at AIST venture company
  – Evolvable Systems Research Institute, Inc.
Application

- 1bitTIFF Workflow
- Graphic-arts machinery
  - Digital copier, Printer, CTP setter, DI press, ...
- Embedment in RIP, Printer-driver, and so on.
- Storage and Management of image data after RIP
- Data transfer
Advanced Graphic-arts system

Increase the competitiveness in the graphic-arts industry in next generation by using AIST method

- CTP (Computer To Plate) settter
- DI (Direct Imaging) Press
- DDCP (Direct Digital Color Proofing)

Target

- World market: 46.3 billion dollar (2008)
- Growth at 18%/year
  (Prediction of Hidelberg)
CTP (Computer To Plate) Setter

The machine to create *plate*, used in offset press, directly from digital data without analogue film.

AIST method drastically reduces the costs for data-transfer by efficiently compressing huge graphic-arts image

Leading manufacturer:
Creo, Heidelberg, Fuji Photo Film, Dainippon Screen MFG, Toyo Ink MFG, Toray Industries
DI (Direct Imaging) Press

The press machine with the functionality of laser imaging of thermal plate.

AIST method drastically reduces the costs for data-transfer by efficiently compressing huge graphic-arts image

**Leading manufacturer:**
Hidelberg, Adast, Karat Digital Press, MAN Roland, KOMORI, Dainippon Screen MFG, SAKURAI Graphic Systems, RYOBI Imagix
Digital workflow and AIST method

Advantages of digital printing

- Short-run, Low-cost
- Fine precision printing
- Eradication of out-of-print and -existence

The Problem

Enormous size of the image with high-resolution
=> Large costs for transfer and storage

Advantages of AIST method

- Efficient Compression
- Improvement in Compatibility between systems
Target in Graphic-Arts Industry

Large benefit: Total system
Small benefit: Elements in total system

Total system = Workflow
(Author - Edit - Proof - Output - Bookbinding - Delivery)

Advanced Workflow for Digital Publishing

FilingPro* (Image data filing software)
DDCP (Direct Digital Color Proof)
- CTP - DI (Digital Press Machinery)
On-demand Publishing

*Evolvable Systems Research Institute Inc.
FilingPro (Image Data Filing Software)

[This lossless compression method] + [Database system]
Contents of this talk

• Basic Concept of Evolvable Hardware

• Digital Hardware Evolution
  – Gate-level Evolvable Hardware
    • EMG prosthetic hand
    • Clock-timing adjustment
    • Data compression for print image data
  – Function-level Evolvable Hardware
    • Autonomously reconfigurable neural network chip

• Analogue Hardware Evolution
  – Analogue EHW chip for cellular phones

• Mechanical Hardware Evolution
  – Evolvable Femto-second Laser System
  – Evolvable Interferometer
  – Evolutionary fiber alignment
Function Level Hardware Evolution: Evolvable Neural Net Chip

• On-line digital EHW
• Purpose
  – fast and autonomous synthesis of non-linear functions
  – time-varying applications like pattern recognition, time-series prediction, etc.
  – Development of dedicated LSI
Problems of Neural Network

• Need of On-line Learning for time-varying applications
• Hardware support for fast NN execution
• Performance of NN
  – heavily depends on the number of hidden layers, hidden nodes, and functions of hidden nodes.

Weak theoretical background,
Limit of hardware support

• Weak performance of On-line learning
RBF vs. Sigmoid function

• Radial Basis Function (RBF) Network
  – fast learning speed
  – large number of hidden nodes

• Sigmoid Neural Network
  – slow learning speed
  – less number of hidden nodes

Combination of RBF and Sigmoid in single neural network (Hybrid Neural Network : HNN)
GRD chip: basic concept

Chromosome

(S,c1,d1,w1) (G,a2,b2,w2)

Genetic Operations

(G,a1,b1,w1) (G,a2,b2,w2)

Evolution

⋯ (S,ci,di,wi)⋯ (G,a15,b15,w15)

Network

GRDchip

RISC

DSP

Reconfiguration
Genetic Reconfiguration of DSPs Chip (GRD chip)

- Autonomously reconfigurable Neural Network chip
- 100Mhz 32bit RISC core + 33Mhz 16bit DSP x 15
  - RISC : GA, reconfiguration, I/O
  - DSP : execution of NN, Steepest Descent Method
  - scalable connection of the chips
DSP organization
Genetic Learning

• optimal number of hidden nodes, optimal combinations of RBF and sigmoid
  – can not be decided theoretically in advance.
  – Dynamic decision depending on problems and hardware resource.

• Dynamic decision with GA
Performance of GRD chip

• Operational since last June
• second version in progress
• 10 times faster than Pentium II (400MHz)
• 200 times faster than SUN Ultra2
  (with 9 GRD chips)
  – Execution speed per chip
    319MCPS (Mega Connection Per Second)
Adaptive Equalization

- On-line learning is needed to adapt to the changing environment.
- Fast speed and compact implementation by hardware.
Problems with traditional adaptive equalizer

\[ a_t \xrightarrow{\text{transmission signal}} y_t, y_{t-1}, y_{t-m+1} \xrightarrow{\text{received signal}} y_t, y_{t-1}, y_{t-m+1} \xrightarrow{\text{Linear Filter}} \sum \xrightarrow{\text{output}} \hat{a}_{t-d} \]

Severe performance degradation when non-linearity is strong.
Adaptive Equalizer with GRD

- Fast speed
- On-line adapt
- Nonlinear equalization

Advantage
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Analogue EHW chip for cellular phones

- Off-line analogue EHW
- Intermediate Frequency Filter
  - Analogue Band-pass Filter
  - Must be compact and fast: LSI required
  - Large market
- Variations in analogue components performance are adjusted by GA.
- **Installed in cellular phones since Dec. 2001.**
Variations in Analogue Components Values

- Analogue components values can be made as the same as the design specifications.
- Yield rates are degraded in high end applications.
  - e.g. Even 1% shift from the center frequency is not allowed in cellular phones.
Off-line analogue EHW chip

• The performance of the analogue EHW chip can be adjusted by downloading adequate bit string (i.e. chromosomes).

• GA reconfigures each chip when it's shipped out.

• Why? To let each chip to fill out the design specification.
Advantages of analogue EHW

- Improvement of yield rate (100%)
- Reduction of die space (60% less)
  - cheaper process can be utilized.
  - Reduction of power consumption (40% less)
- Less effort in the design phase

Applicable to large variety of analogue circuits.
Analogue EHW chip for IF filter

Analogue EHW Chip

IF Filter

(IF Filter)

Architecture Bits

(\text{Gm} : \text{Transconductance Amplifier})

CPU (GA)

evaluation

download

Chromosomes

Register

(0\,1\,0\,0\,1\,1\,0\,1\,0\ldots\,0\,1)
Variation in Gm element

- Gm value \((I_{OUT}/V_{IN})\) alters 20% (max).
- No chip satisfies the specification without adjustments.

GA adjusts bias currents:
90% of chips can fill out the specification.
Analogue EHW chip for cellular phones

- Bias Current Controller
- Filter 1
- Filter 2
- Filter 3
Result (1)

Yield rate : 100 %

Before

After

Gain

Specification

Frequency response

Frequency (kHz)
Result (2)

• Comparison with other methods
  – hill climbing : 65%
  – GA : 100%

GA escapes from local minimum.
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Evolvable Femtosecond Laser System

Laser alignment can be optimized autonomously by genetic algorithms to obtain the maximum output.

Advantages:
1. Autonomous Adjustment
2. Portable Size
3. Ultrashort pulse (∼10^{-15}sec)

Especially Suitable for:
1. Laser Processing for Diamonds and Shape-memory-alloy
2. Medical Treatment (e.g. macula, depilation)
Interferometer System

- Interferometer is main system of environmental spectroscopic analysis instruments
  - such as Fourier-transform Infrared Spectroscopy (FTIR)

- These instruments are very large, and performance is greatly influenced by environmental conditions.
  - Because the internal interferometer have many optical components to necessary precise positioning alignment.
Evolvable Interferometer

- The on-site use of spectrum-analysis instruments has been virtually impossible.

  Automatic Alignment System by GAs

- The automatic adjustment method eliminates this problem making it possible to use interferometers outdoors.

  The FTIR is used outdoor for environmental analysis on-site.
Result of Experiment
Fiber Alignment System

- Fiber alignment is necessary when two optical fibers are connected.

- The connection requires much greater precision in the order of sub-micron-meters.
Evolvable Fiber Alignment System

• Conventional fiber alignment system is
  – only capable of fibers with three degree of freedom (x,y,z)
  – non-useful to five or more degree of freedom (x,y,z, θ, φ,⋯)

• The alignment of optical fibers with five degrees of freedom can be completed within a few minutes.

Automatic Alignment System by GAs
Developed Fiber Alignment System
Conclusion

• Industrial Applications for EHW
  – Time-variant behaviour (Adaptive)
  – Real-time performance
  – Fault-tolerant
  – Analogue systems

• Promising application domains
  – analogue devices
  – optical systems