SYMBOLIC PARASITIC EXTRACTOR FOR CIRCUIT SIMULATION (SPECS)

J. D. Bastian * M. Ellement** P. J. Fowler*
C. E. Huang** L. P. McNamee**

*Rockwell International Corporation, Defense Electronics Operations
Microelectronics Research & Development, 3370 Miraloma Avenue
Anaheim, California 92803

** Computer Science Department
University of California at Los Angeles

ABSTRACT

This paper describes the design, development and implementation of the program SPECS. The purpose of SPECS is to automatically extract from a Rockwell microelectronic symbolic matrix description a netlist for circuit simulation. This program differs from others in that it uses a symbol layout matrix as an input, calculates both interelectrode and intrinsic capacitance, calculates conductor resistance, produces a schematic representation of the network and has a selective TRACE, i.e., traces only the circuit or network of interest.

INTRODUCTION

As integrated circuit technology has evolved, the constant trend has been toward smaller and smaller devices in order to decrease the total chip size required for some particular function and to increase the operating frequency. While the smaller feature size has yielded faster devices, it has not resulted in correspondingly faster circuits. This is a consequence of the greater role played by layout-generated parasitics. Because the vertical dimensions are not scaled in the same proportion as the horizontal ones, there is an increase in the interelectrode capacitance [1]. This is a serious problem for VLSI devices since a deteriation in speed performance and increased cross- talk will result. For current SOS, GaAs and SOI technology, coupling capacitance dominates. However, for bulk, because of the proximity of the ground plane, inherent capacitance dominates.

Current computer-aided design (CAD) tools have helped to solve some of the problems associated with the increasing complexity by performing design rule checks (minimum size and spacing rules) and extracting a network from the layout for input to logic simulators (e.g., MOSSIM, TEGAS) and to circuit simulators (e.g. SLIC, SPLICE). However, most of the extraction techniques consider only crossover capacitance and ignore the interconnect resistance and the coupling between parallel interconnects [2-9]. One technique presented by Yoshida, et al [10], does extract some parasitic capacitance and resistance from polygon layouts but in general is restrictive.

In order to include the effects of all the parasitics, a new program, SPECS, was developed. The program was jointly developed by Rockwell International's Microelectronics Research and Development Center and the University of California, Los Angeles, on a MICRO*** project. The intent of SPECS is to provide a detailed representation of the circuit network for an accurate circuit analysis. The circuit of interest may have been identified through a path analysis approach [11] or have been known to be critical due to its function.

PROGRAM OVERVIEW

The modules that comprise SPECS are depicted in the flow diagram of Figure 1. The initial input to the program consists of a Rockwell microelectronic symbolic dataset which contains a circuit of interest. A symbolic representation on a course grid is used at Rockwell for layout of VLSI devices. A symbol, such as *, is used to denote a specific width and length at a particular mask level. Some symbols such as contacts can be on multiple mask levels. Like symbols which are next to each other, i.e. no grid separation, are contiguous even if their dimensions would indicate a gap. Special symbols are used for n-channel and p-channel FETS.

On the symbolic layout, the designer specifies the coordinate locations for the DC supplies as well as the output node of interest. These inputs bound the problem. An automatic TRACE [12] algorithm originates from the specified output node and extracts rectangles of like symbols as it moves toward VDD and ground. It then returns to any branch point or gate node and traces again toward VDD and ground until the entire circuit is traced out. Presently, TRACE will track a circuit from the output node through the entire dataset. Future efforts will permit designer control of the extent of the trace by allowing him to specify how far back (number of stages) he wishes to go. At each gate node the designer will specify by means of prompts in the SIMULATOR FORMAT MODULE, the stimuli for transient simulation purposes.

***MICRO, Microelectronics Innovation and Computer Research Opportunities is a program instituted by the State of California, promoting research in microelectronics and computer science. Teams are formed between University of California personnel and their industrial sponsors. Funding for university personnel is provided half by the State of California and half by industry.

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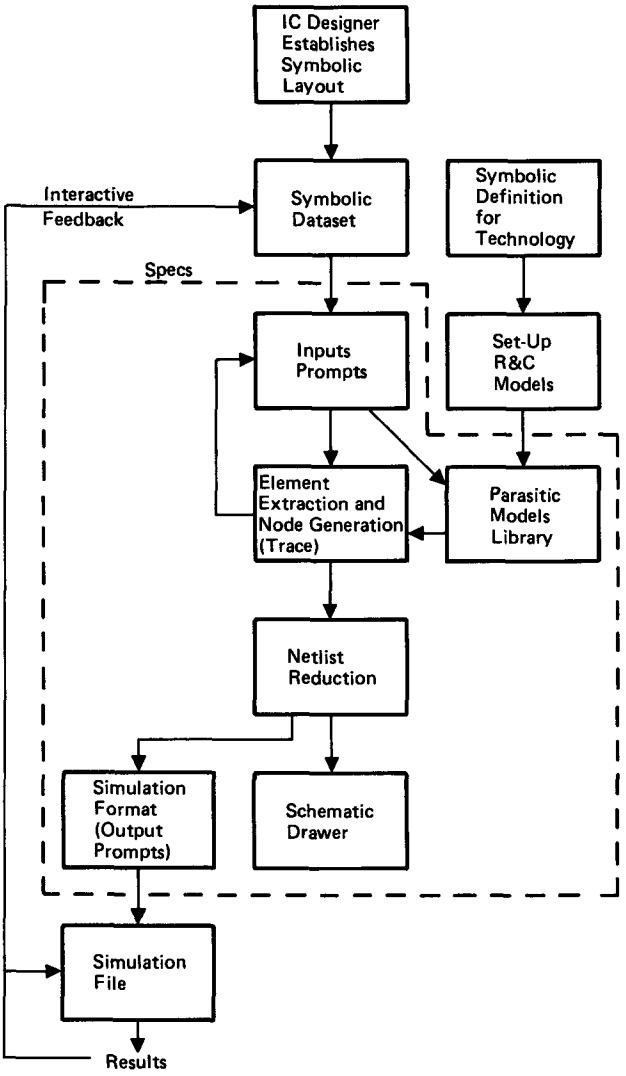


Figure 1. SPECS Flow Diagram

The PARASITIC MODEL LIBRARY is used to convert the trace extracted rectangular symbol sets into resistor and capacitor values for the specific technology. This dictionary is only created once for each technology. A NETLIST REDUCTION routine is used to combine and eliminate elements in accordance with technology determined criteria. The resultant reduced netlist then feeds the SCHEMATIC DRAWER and SIMULATOR FORMAT MODULE. The SCHEMATIC DRAWER allows viewing the extracted circuit in a configuration similar to the symbolic layout, while the SIMULATOR FORMAT MODULE structures the netlist for the appropriate simulator. The initial simulator utilized was the Rockwell inhouse transient circuit analysis program, TRAN. The format, however, could be easily reformatted for the SPICE program. After the circuit file is created, it is submitted for the actual TRAN simulation. Finally, the results of the simulation are returned to the designer for review of the performance results. If required, the designer may change the TRAN input file or symbolic layout description to evaluate various design options, e.g. a wider gate, shorter interconnect, or changes to the basic layout configuration. Also by reviewing the changes to the netlist, the designer can determine the effects of layout changes on both capacitance and resistance values.

The host system for the SPECS program is a VAX-11/780 computer with a tape drive and disk drive. The software is written in U.C. Berkeley PASCAL, with emphasis on using only ANSI-standard constructs, running under the UNIX operating system. The TRAN simulations are done on an IBM 3033.

All SPECS files in the data base are stored using the UNIX file system which consists of directories composed of both files and additional sub-directories. The program is highly modularized so that numerous students could work on programming activities simultaneously without interference.

INPUT PROMPT MODULE

An INPUT PROMPT MODULE was developed in order to prompt the designer for special information that was not included in the symbolic matrix file. The questions asked are as follows:

TECHNOLOGY TYPE ?
SYMBOL REDEFINE ?
GRID SIZE ?
OUTPUT NODE?
SUPPLY VALUES AND LOCATIONS ?

PARASITIC MODEL LIBRARY

In the process of extracting electrical elements, the TRACE algorithm obtains rectangular sets of identified symbols. The rectangular sets have either no interelectrode effects or have interelectrode effects entirely along one side. This means that a single conductor, even when it is in the shape of a rectangle, may consist of numerous rectangles linked together. The PARASITIC MODEL LIBRARY contains the necessary models and tables to convert the rectangles into resistance and capacitance values. Depending on the technology, equations are entered in the PARASITIC MODEL LIBRARY for the intrinsic capacitance value of each symbol, the interelectrode capacitances between all combinations of symbols from one to four grids apart and the coupling capacitance values for conductor crossovers. No capacitance values were entered for diodes or FET devices since the TRAN device models will automatically include the appropriate value based on the individual device size.

The capacitance look-up table was produced with the aid of the FLUX simulator [13]. The FLUX program numerically solves Laplace's equations in two dimensions for the potential distribution and calculates the capacitance using Gauss's law. The parasitic capacitances considered are crossover, intrinsic and parallel, as depicted in Figure 2.

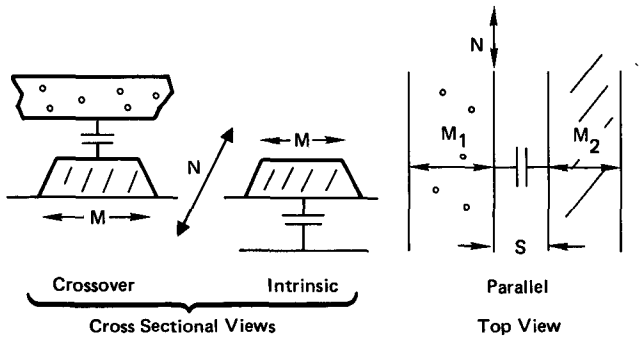


Figure 2. Parasitic Capacitance Conditions Considered

The intrinsic and crossover capacitances are a function of area and length. Their evaluation is performed using the equation:

$$C = C_o (M * N) + C_1 (P)$$

where C_o is the parallel plate capacitance of one square symbolic plot to the ground plane in the case of the intrinsic, or the capacitance of one symbolic plot to another in the case of crossover capacitance. C_1 is the fringing capacitance per symbolic plot which is a result of the perimeter symbols. For the intrinsic, the perimeter (P) is N and for the crossovers, it is N + M where M is the width in symbolic plots and N is the length in symbolic plots. Note, C_o and C_1 have different values for different symbols based on area, thickness and distance from the ground plane. Therefore for each technology, a C_o and C_1 is stored for each symbol used.

The expression for the parallel interelectrode capacitances is of the form,

$$C = N * F_s * C_2$$

Where N is the length of the two conductors in symbolic plots, F_s is the separation factor (no units) and C_2 is the capacitance per symbolic plot. The value of F_s, C_o, C_1 and C_2 were determined by extensive use of the FLUX simulator. The separation factor is a function of how many symbolic plots (S) separate the two conductors, i.e. one, two, three or four plots; no consideration is presently made past four plots. The value of F_s is inverse proportional to the number of separation plots. The value of C_2 is a function of the minimum width (M) of the two conductors. As for F_s, a width of greater than four plots is not considered. All of the coupling capacitance calculations are based on a three body approach.

While there are slight differences in the mathematical expressions for the different types of parasitic capacitances, the most notable difference is in their extraction. The intrinsic and crossover types involve an accounting operation. The parallel type involves the determination of the minimal width and separation distance (orthogonal to the parallel direction). This means the parasitic capacitance resulting from the parallel type, occurs in segments as illustrated in Figure 3.

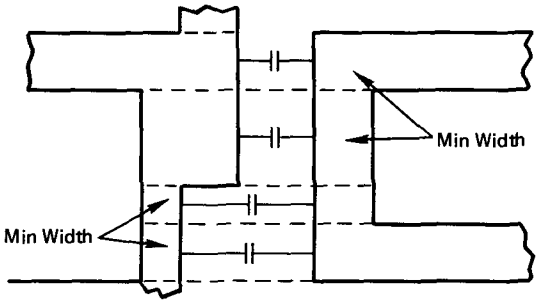


Figure 3. Illustration of Segmenting Parallel Interconnects

For determining the parasitic resistance, expressions for five different rectangle configurations are required. The different configurations are defined by the orientation of their input (a) and output (b) ports as depicted in Figure 4. The orientations considered were: Opposite, Diagonal, Center, Orthogonal and Same.

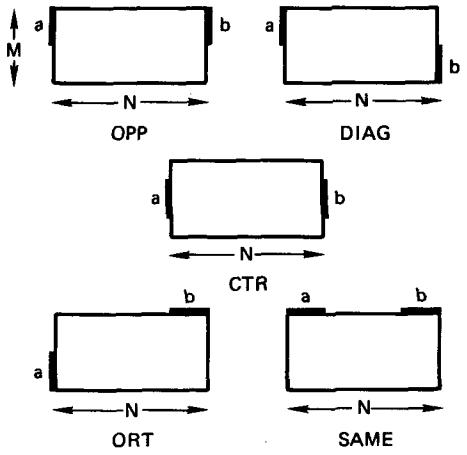


Figure 4. Five Building Block Rectangles

The variables associated with these rectangles are port size (a and b), port orientation (OPP, DIAG, CTR, ORT and SAME) and the rectangles' dimensions (M and N). For each of the five building blocks, an expression was developed which relates the variables to the resistance from port (a) to port (b). The approach consisted of representing each rectangle with a resistor mesh network, as shown in Figure 5. The resistor mesh network was then solved on a circuit simulator to determine the equivalent resistance value. The data at certain points were compared with results in reference [14] and with 2D modeling results, and found to correlate. The data from over 300 simulations was analyzed using a Hewlett-Packard Polynomial Regression routine. The resultant equations were of the form:

$$R = \{F(N/M) + B_0 + B_1 [a/M + b/M] + B_2 [(a/M)^2 + (b/M)^2] + B_3 [(a/M)^3 + (b/M)^3] + B_4 [(a/M)^4 + (b/M)^4]\} \rho$$

The function F (N/M), equals N/M for all rectangle types except SAME where it equals zero. The coefficients, B_i, are unique for each rectangle. To consider short rectangles and relatively large input ports, twelve sets of coefficients were used along with a series of dimensional checks.

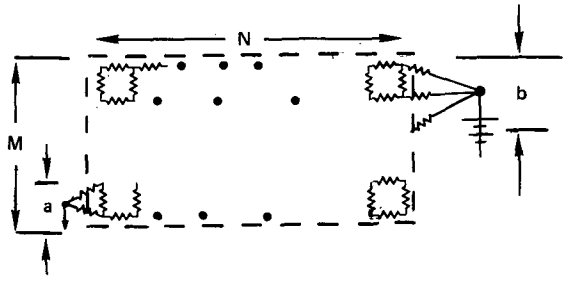


Figure 5. Mesh Representation of DIAG Rectangle

ELEMENT EXTRACTION AND NODE GENERATION

The ELEMENT EXTRACTION AND NODE GENERATION are accomplished by a complex signal flow trace algorithm which takes advantage of the discrete and informational attributes of the symbolic layout matrix. This routine is the largest, consisting of over 5000 lines of code. Starting at a contact

symbol (the output node must be specified at a contact), the trace proceeds along each of the symbols specified by the contact description. Since adjacent-like symbols indicate continuity, the trace maps the area of like symbols into a series of rectangles. It accomplishes this while perserving a sense of current flow direction and acquiring information about near neighbor interconnects (conductors that are separated by from one to four empty grid spaces). By interpreting the symbols, their geometric configuration with respect to current flow and their near neighbor relations, the parasitic resistances and interelectrode capacitances can be evaluated by the equations in the PARASITIC MODEL LIBRARY.

Circuit nodes are automatically entered when: (a) a change in trace path width occurs (e.g., a branch, a change in conductor width or a turn); (b) a new symbol, or (c) a near neighbor occurrence. Crossovers, FET's and diodes have unique symbols; therefore their extraction involves symbol recognition and determination of the signal flow direction. This is particularly important for determining what is the length and width for the FET gate. While the extracted elements are being stored in their respective stacks, with their node numbers and values, the coordinate locations of the extracted nodes and the general layout shape are also stored for subsequent processing by the SCHEMATIC DRAWER.

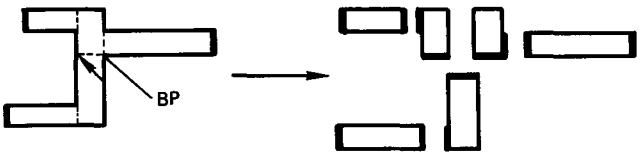


Figure 6. Illustration of Partitioning.

The trace algorithm which starts at a contact, advances until there is a change in width; at this point a rectangle with the two ports, the contact and the partition, is established, as shown in Figure 6. This two-port rectangle is referenced to the PARASITIC MODEL LIBRARY for capacitance and resistance evaluations. These values are stored along with the port locations and the TRACE continues. The next change in width produces another partition and another two-port rectangle. After evaluation, this value can be combined with the preceding one assuming their common port does not occur at a branch. This partition and splice operation continues until the configuration is completely traced.

When branching occurs, a rectangle of more than two ports is generated. (See rectangle with partition marked BP in Figure 6) This reduces to a two-port rectangle by treating the input port as a branch node and closing all except one of the output ports. The branch port is stored for a subsequent trace which is required to complete the configuration. The resultant two-port rectangle is evaluated. Partitioning and splicing continue from the selected output port until a contact or labeled supply/ground node is reached. If another branch is encountered, the same procedure is applied. When the trace returns to a branch port, an untraced output port is opened while all other output ports are closed. The branch port rectangle is then reevaluated with this new output port, and becomes part of the spliced rectangles of the branch being traced.

These operations are repeated until all branches have been traced, thus completing the configuration.

The validity of breaking a complex conductor into a series of rectangles and then summing the individual rectangular resistance values to obtain the overall resistance was substantiated by a series of empirical tests. This was accomplished by cutting electrically conductive foam into various shapes (Figure 7). Ohmic contact was made with aluminum foil and EKG gel. Curve tracer measurements were made on the intact structures and progeny. Measurements on the component rectangles were done with aluminum/EKG contacts along the cuts.

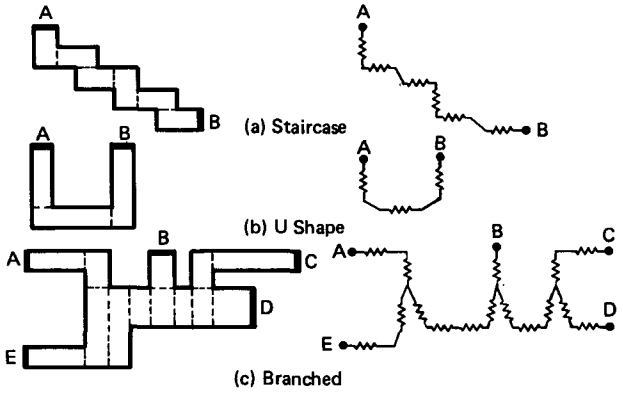


Figure 7. Experimental Structures Used for Partition and Splice Validation

The error for the staircase was three percent, for the U shape one percent and for the complex branched structure it was a maximum of fifteen percent. Even though the latter error may appear high, note that the overall percent error depends on the relative resistance of the branch rectangles to that of all of the other rectangles between the contacts, i.e., as the length of the branches increases, the percent error decreases. The error is a result of the placement of the branch node. Depending on the origin of the trace, the branch node may be located at any one of the ports, but not at the electrical "center of gravity". Consequently, the resistance for any pair of contacts of a multibranched structure is dependent upon the original trace path taken within the structure.

NETLIST REDUCTION

The partitioning which is done in the process of extraction automatically produces pseudo-distributed networks. However, efficient use of the circuit simulation precludes utilization of all of these elements and nodes as extracted. Rather it is preferrable to reduce the number of components and nodes in the netlist without compromising the simulation. This is accomplished initially by a straight forward summing of series resistance and parallel capacitance. The major reduction, however is obtained by an approximation technique using a technology dependent time constant τ, and a minimum resistance and capacitance, RMIN and CMIN. The time constant reflects the minimum transition time for a particular technology. An initial estimate of τ is 0.1 times the transition time of a single unit size inverter. Figure 8 illustrates how the reduction process continues based on this criteria.

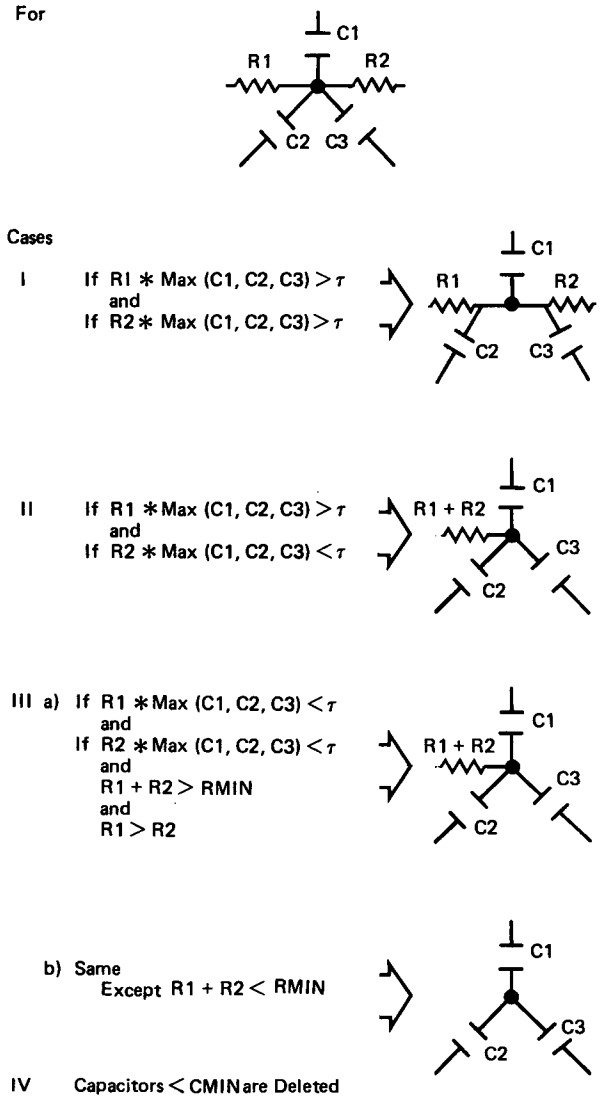


Figure 8. Netlist Reduction Technique

Interelectrode capacitances which go to floating nodes, i.e., nodes which are not in the circuit of interest, are multiplied by 2.0 to account for a potential "Miller" effect.

SCHEMATIC DRAWER

The SCHEMATIC DRAWER provides the designer a quick visual means of analyzing the extracted circuit. All extracted FET's, resistors and node numbers are displayed. In order to make the representation readable, the paraistic capacitances are not indicated. However, by examining the netlist, the designer can easily determine their location and value. The module consists of approximately 900 statements. During the extraction, the coordinates of conductor corners, the extracted components and the associated nodes are stored as linked lists. These are then used to construct a double-linked sparse matrix, creating rows and columns only when either a new X or new Y coordinate is encountered. Next, the minimum distance between columns is determined based on the longest node/device name which must be present. This minimum distance is always greater than 0, forcing items which were originally not colinear to stay not colinear; this helps preserve the original geometrical shape so that the designer should be able to recognize where components are located. This procedure is used to generate a one to one mapping of the old coordinates to new coordinates, which is used to place components and nodes in their correct location on the printer plot schematic. The output of the SCHEMATIC DRAWER is illustrated in Figure 9.

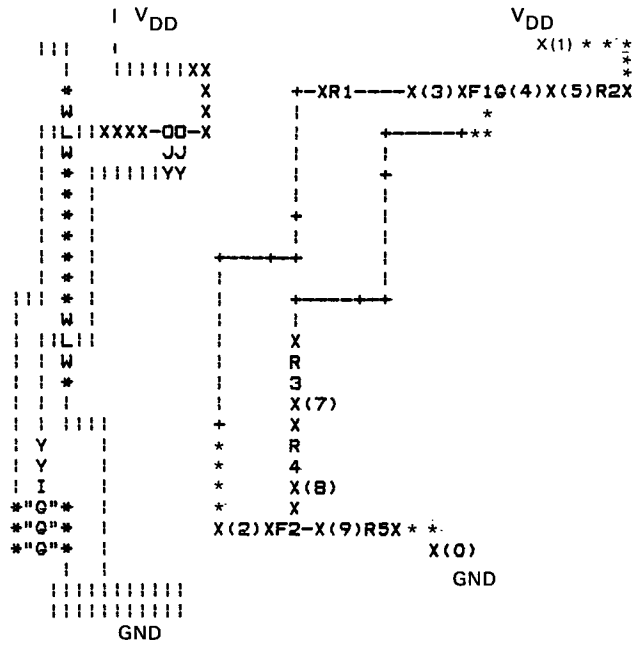


Figure 9. Illustration of Correspondence Between the Symbolic Layout and the Output of the SCHEMATIC DRAWER

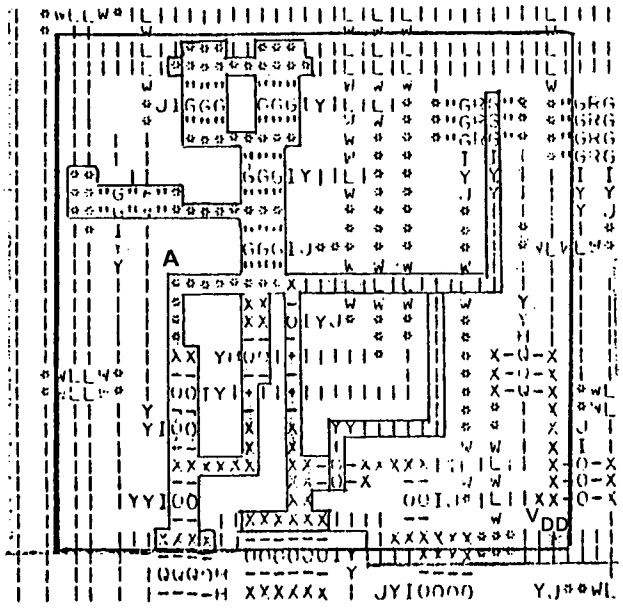
SIMULATION FORMAT MODULE

The SIMULATION FORMAT MODULE consists of approximately 2000 statements. The formator operates on the reduced netlist. It automatically inserts the control statements based on inputs from a series of prompts, and properly formats the components (e.g., a 1K resistor between nodes one and two becomes R1 (1,2) 1K. The designer is prompted to provide the FET parameter data name from the process data bank and the condition, i.e. typical, fast, slow, etc. He is also prompted for the voltage and current sources, simulation sampling time, simulation end time, temperature and variable to be plotted or printed by the simulator. The resultant file is then submitted for a TRAN simulation. This MODULE is to be expanded in the future, to aid in the display of TRAN outputs in an interactive mode which can be tied to both the schematic and the symbolic representation.

SAMPLE PROBLEM

The symbolic layout dataset, shown in Figure 10 was exercised on the SPECS program. The thick continuous line is used to highlight the area of interest and the outline is to show

the location of the circuit. Neither of these lines are part of the layout data base. This limited the overall trace to a reasonable area, with a focus on the subcircuit of interest. The reduced extracted netlist is shown in Figure 11. The CPU time required to generate the netlist was 63 seconds on the VAX-11/780. This consisted of 10 seconds for reading the symbolic matrix, 7 seconds for tracing the power lines, 32 seconds for extraction and 14 seconds for formatting the extracted elements. No specific attempt to optimize the CPU time was made for any of the modules.



I = METAL
* = n^+ CONTACT
" = n^+ CONDUCTOR (W, L)
G = n FET
X = p^+ CONTACT
O = pFET
- = p^+ CONDUCTOR

Figure 10. Symbolic Layout of Example Circuit. The Circuit to be Extracted is Within the Thick Continuous Line. The Output is Designated by the Large A and the Input by I.

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SPECX.DATA
TRAN 1
EXTRACTED CIRCUIT
SETN1=SOS4EN,4TYP
SETP2=SOS4EP,4TYP
F1,SN1(G3,D6,S2,B5)3X,1X
F2,SN1(G0,D0,S7,B10)2X,1X
F3,SN1(G14,D15,S6,B16)3X,1X
F4,SN1(G18,D0,S15,B20)3X,1X
F5,SN1(G0,D0,S15,B26)3X,1X
F6,SP2(G39,D45,S2,B46)1X,1X
F7,SP2(G36,D47,S2,B48)2X,1X
F8,SP2(G0,D50,S49,B51)2X,1X
F9,SP2(G23,D52,S49,B53)2X,1X
F10,SP2(G0,D54,S52,B55)2X,1X
R1(6,7)110
R2(0,12)100
R3(18,22)100
R4(22,23)200
R5(0,28)100
R6(28,30)190
R7(30,0)200
R8(14,33)100
R9(33,35)190
R10(35,36)200
R11(3,37)100
R12(37,38)190
R13(38,39)200
R14(2,42)200
R15(2,44)200
R16(45,1)1200
R17(47,49)560
R18(50,1)200
R19(54,2)200
C35(50,1)0.34F
C36(35,36)2.70F
E1(+1,-0)+5
E2(+3,-0)+5
E4(+36,-0)+5
E6(+18,-0)POINTS,0,0/0,1N/+5,2N/+5,20N
R20(36,35)200
C1(6,0)1.86F
C2(8,0)1.00F
C3(12,2)2.40F
C4(12,0)1.50F
C5(13,0)2.80F
C6(17,0)1.80F
C7(18,0)0.70F
C8(22,17)0.56F
C9(22,6)6.00F
C10(22,2)3.30F
C11(22,0)3.30F
C12(22,8)0.80F
C13(22,12)3.40F
C14(23,0)2.80F
C15(25,0)0.82F
C16(24,0)0.70F
C17(28,0)2.00F
C18(30,2)4.22F
C19(31,0)2.80F
C20(14,17)0.70F
C21(33,28)2.68F
C22(35,2)4.91F
C23(36,0)2.80F
C24(37,33)1.20F
C25(37,2)8.09F
C26(39,0)1.40F
C27(28,2)5.70F
C28(33,2)5.30F
C29(42,0)4.20F
C30(2,1)1.20F
C31(44,0)2.80F
C32(35,45)2.70F
C33(30,45)2.70F
C34(30,47)2.70F
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Figure 11. Netlist Representation of Circuit Extracted From Symbolic Layout (Figure 10)

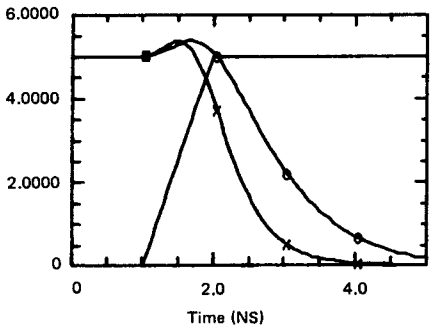

Figure 12. Simulation Results From Figure 11 Netlists. Input Waveform Idealized Output (X), Extracted Output (0)

Circuit simulations were performed with TRAN using the reduced extracted netlist and an idealized netlist (i.e. no parasites). Figure 12 is a plot of the two outputs to highlight the difference with and without parasitics. The outputs at A (re. Figure 10) are the result of a 5 volt step applied at the input I (re. Figure 10) with the other FET's in the circuit biased so that the signal could propagate to the output A. The transition time from 4 volt to 1 volt for the idealized circuit was .75N sec, while for the extracted circuit was 1.31N sec. This factor of 1.76 while significant, only reflects the impact of coupling on speed and not the possibly more significant affect of cross-talk on performance.

It should also be stressed that this was a simple example, extended conductor lines which would have introduced large parasitic resistors and capacitors were not present due to the limited window considered.

CONCLUSIONS

A circuit level extractor program SPECS was described which extracts interelectrode and intrinsic conductor capacitance, conductor resistance and the size/location of active devices from a symbolic layout description, and generates a simulation netlist (including node numbers and the necessary controls).

Key features such as the use of a selective TRACE algorithm which extracts only the circuit of interest, a scheme for reducing the extracted netlist and a terminal display of the resultant electrical schematic were illustrated. Also a new approach consisting of extracting rectangles of like symbols to calculate parasitic resistance and capacitance was developed and validated for resistance calculations of irregular shapes. Although SPECS was developed primarily for the Rockwell symbolic dataset, it could be extended to other layout data bases, such as sticks and CIF. The present limitation of considering interelectrode effects up to four symbols away could be expanded, if warranted by additional modeling or test data. The existing version of SPECS can only handle a 125 x 125 symbolic matrix becuase of limitations imposed by the PASCAL compiler on the VAX-11/780 computer. This limitation will be expanded to a 5000 x 5000 matrix for the next version of SPECS. In the future, the look-up values used for parasitic capacitance and resistance are to be correlated with test chip results.

The demonstration on a simple circuit showed the large effects which parasitics can play on device operation, and the criticality of extracting the parasitics. The extent and number of parasitics make a manual extraction time consuming and difficult.

ACKNOWLEDGEMENT

The authors would like to extend their thanks to Kenneth Swanson and Joseph Szelong at UCLA, and to William Dierking, Dave Kliment, Robert Gauthier, Bob Polkinghorn, Ken Gerst, Ben Franqui, Garry Heimbigner and Bill Pearce at Rockwell for their valuable contributions during the planning phase of SPECS and their continuing support throughout the development.

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