Panel: How Will the Fabless Model Survive?

Chair: Don Clark - Wall Street Journal
Speakers: Thomas Hartung - X-FAB Semiconductor Foundries AG
Mark Bohr – Intel Corporation
Ana Hunter - Samsung Semiconductor Inc
Brad Paulsen - TSMC NA
Felicia James - Cadence Design Systems
Nick Yu - Qualcomm

ABSTRACT
The fabless model was traditionally enabled through clean interfaces – both in technical and business terms – between foundries and fabless semiconductor companies. However, with advanced geometry and analog/mixed-signal process nodes, the technical challenges have been greatly magnified, so that successful semiconductor design requires intimate cooptimization of design and manufacturing, infringing upon those clean interfaces. The panel presents views to these challenges and specifically how companies are planning to address them.

Keywords: Business, DFM, Foundry, Fabless
The Good, the Bad, and the Ugly of Silicon Debug

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ABSTRACT
Silicon debug begins with the arrival of design prototypes and can continue well after a product has gone into production. It is perhaps the most exciting and challenging stage of the integrated circuit development process. This paper gives an overview of silicon debug, and describes tools and methods used during the debug process.

Keywords: Debug, design for test and debug, characterization, validation.

REFERENCES
A Reconfigurable Design-for-Debug Infrastructure for SoCs

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ABSTRACT
In this paper we present a Design-for-Debug (DFD) reconfigurable infrastructure for SoCs to support at-speed in-system functional debug. A distributed reconfigurable fabric inserted at RTL provides a debug platform that can be configured and operated post-silicon via the JTAG port. The platform can be repeatedly reused to configure many debug structures such as assertions checkers, transaction identifiers, triggers, and event counters.

Keywords: Silicon debug, at-speed debug, assertion-based debug, what-if experiments.

REFERENCES
[3] Collett ASIC/IC Verification Study, 2004 (data for 180nm and 130nm)
Visibility Enhancement for Silicon Debug

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ABSTRACT
Several emerging Design-for-Debug (DFD) methodologies are addressing silicon debug by making internal signal values and other data observable. Most of these methodologies require the instrumentation of on-chip logic for extracting the internal register data from in situ silicon. Unfortunately, lack of visibility of the combinational network values impedes the ability to functionally debug the silicon part. Visibility enhancement techniques enable the virtual observation of combinational nodes with minimal computational overhead. These techniques also cover the register selection analysis for DFD and multi-level design abstraction correlation for viewing values at the register transfer level (RTL). Experimental results show that visibility enhancement techniques can leverage a small amount of extracted data to provide a high amount of computed combinational signal data. Visibility enhancement provides the needed connection between data obtained from the DFD logic and HDL simulation-related debug systems.

Keywords: Functional verification, Silicon Debug, Silicon validation

REFERENCES
A CPPLL Hierarchical Optimization Methodology
Considering Jitter, Power and Locking Time

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Abstract
In this paper, a hierarchical optimization methodology for charge pump phase-locked loops (CPPLLs) is proposed. It has the following features: 1) A comprehensive and efficient behavioral modeling of the PLL enables fast simulations and includes the important PLL performances jitter, power and locking time, as well as stability constraints for the nonlinear locking process and the linear lock-in state; 2) Behavioral modeling of the PLL building blocks addresses as behavioral-level parameters: current and jitter of the charge pump (CP), gain, current and jitter of the voltage controlled oscillator (VCO), as well as R, C’s of the loop filter (LF). It enables a proper propagation of PLL specifications down to the circuit-level design parameters; 3) An accurate and efficient performance space exploration technique on circuit level provides the feasible regions of the behavioral-level parameters of the building block by multidimensional Pareto-optimal fronts. This enables a first-time-successful top-down optimization process. Experimental results show the efficacy and efficiency of the presented method. The methodology can be applied to other large-scale analog circuits.

Keywords: Hierarchical Optimization, Pareto-Optimal Fronts

References


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Hierarchical Bottom–up Analog Optimization Methodology Validated by a Delta–Sigma A/D Converter Design for the 802.11a/b/g Standard

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ABSTRACT
This paper describes key points and experimental validation in the development of a bottom–up hierarchical, multi–objective evolutionary design methodology for analog blocks. The methodology is applied to a continuous–time ΔΣ A/D converter for WLAN applications, to generate a set of Pareto–optimal design solutions. The generated performance tradeoff offers the designer access to a set of optimal design solutions, from which the designer can choose a satisfactory design point according to the performance specifications. The presented method takes advantage of the Pareto–optimal performance solutions of the hierarchical lower–level sub–blocks to generate the overall Pareto–optimal set at system level. The way the lower–level performance tradeoffs are combined and propagated to higher hierarchical levels, is one of the major key points in the bottom–up methodology. The experimental results validate the methodology for a 7–block hierarchical decomposition of a complex high–speed ΔΣ A/D modulator for a WLAN 802.11a/b/g standard.

Keywords: Hierarchical Synthesis

REFERENCES


Generation of Yield-Aware Pareto Surfaces for Hierarchical Circuit Design Space Exploration

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ABSTRACT
Pareto surfaces in the performance space determine the range of feasible performance values for a circuit topology in a given technology. We present a non-dominated sorting based global optimization algorithm to generate the nominal pareto front efficiently using a simulator-in-a-loop approach. The solutions on this pareto front combined with efficient Monte Carlo approximation ideas are then used to compute the yield-aware pareto fronts. We show experimental results for both the nominal and yield-aware pareto fronts for power and phase noise for a voltage controlled oscillator (VCO) circuit. The presented methodology computes yield-aware pareto fronts in approximately 5-6 times the time required for a single circuit synthesis run and is thus practically efficient. We also show applications of yield-aware paretos to find the optimal VCO circuit to meet the system level specifications of a phase locked loop.

Keywords: Yield, performance space, pareto surfaces, optimization

REFERENCES
A Real Time Budgeting Method for Module-Level-Pipelined Bus Based System using Bus Scenarios

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ABSTRACT
In designing bus based systems with parallel and pipelined architecture, it is important to derive a real time budget (a specified execution time limit) for each task of a bus based system while satisfying given end-to-end real-time constraints of the entire system such as throughput and latency constraints. In this paper, we define a bus scenario representing a set of possible execution sequences of tasks and bus transfers executed in a bus based system. Then we propose a method for deriving real time budgets of all the tasks running in parallel and pipelined fashion from the pair of a system configuration (such as bus topology) and a bus scenario. In deriving such real time budgets, we consider computational complexity of each task, the amount of bus transfers and bus arbitration policies (e.g. fixed priority or time divided round robin based arbitration). We show that the proposed method is effective for designing several bus based systems such as MPEG decoders.

Keywords: Bus based systems, Real-time systems, Pipelined processing, Multimedia processing, Cycle budgeting

REFERENCES


Exploiting Forwarding to Improve Data Bandwidth of Instruction-Set Extensions

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ABSTRACT
Application-specific instruction-set extensions (custom instructions) help embedded processors achieve higher performance. Most custom instructions offering significant performance benefit require multiple input operands. Unfortunately, RISC-style embedded processors are designed to support at most two input operands per instruction. This data bandwidth problem is due to the limited number of read ports in the register file per instruction as well as the fixed-length instruction encoding. We propose to overcome this restriction by exploiting the data forwarding feature present in processor pipelines. With minimal modifications to the pipeline and the instruction encoding along with cooperation from the compiler, we can supply up to two additional input operands per custom instruction. Experimental results indicate that our approach achieves 87–100% of the ideal performance limit for standard benchmark programs. Additionally, our scheme saves 25% energy on an average by avoiding unnecessary accesses to the register file.

Keywords: Instruction-set Extensions, Data Forwarding

REFERENCES
Multiprocessor System-on-Chip Data Reuse Analysis for Exploring Customized Memory Hierarchies

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ABSTRACT
The increasing use of Multiprocessor Systems-on-Chip (MPSoCs) for high performance demands of embedded applications results in high power dissipation. The memory subsystem is a large and critical contributor to both energy and performance, requiring system designers to perform exploration of low power memory organizations. In this paper we present a novel multiprocessor data reuse analysis technique that allows the system designer to explore a wide range of customized memory hierarchy organizations with different size and energy profiles. Our technique enables the system designer to explore feasible memory subsystem solutions that meet power and area constraints while maintaining the necessary performance level. Our experiments on the complex QSDPCM benchmark illustrate the exploration of a wide range of customized memory hierarchies for an MPSoC implementation.

Keywords: Scratch pad memory management, customized memory hierarchy, multiprocessor data reuse analysis.

REFERENCES
Prototyping a Fault-Tolerant Multiprocessor SoC with Run-time Fault Recovery

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ABSTRACT
Modern integrated circuits (ICs) are becoming increasingly complex. The complexity makes it difficult to design, manufacture and integrate these high-performance ICs. The advent of multiprocessor Systems-on-chips (SoCs) makes it even more challenging for programmers to utilize the full potential of the computation resources on the chips. In the mean time, the complexity of the chip design creates new reliability challenges. As a result, chip designers and users cannot fully exploit the tremendous silicon resources on the chip. This research proposes a prototype which is composed of a fault-tolerant multiprocessor SoC and a coupled single program, multiple data (SPMD) programming framework. We use a SystemC based modeling and simulation environment to design and analyze this prototype. Our analysis shows that this prototype as a reliable computing platform constructed from the potentially unreliable chip resources, thus protecting the previous investment of hardware and software designs. Moreover, the promising application-driven simulation results shed light on the potential of a scalable and reliable multiprocessing computing platform for a wide range of mission-critical applications.

Keywords: retargetable simulation, network-on-chip, multiprocessor system, fault-tolerance, system-on-chip, run-time verification

REFERENCES
Statistical Analysis of SRAM Cell Stability

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ABSTRACT
The impact of process variation on SRAM yield has become a serious concern in scaled technologies. In this paper, we propose a methodology to analyze the stability of an SRAM cell in the presence of random fluctuations in the device parameters. We provide a theoretical framework for characterizing the DC noise margin of a memory cell and develop models for estimating the cell failure probabilities during read and write operations. The proposed models are verified against extensive Monte-Carlo simulations and are shown to match well over the entire range of the distributions well beyond the 3-sigma extremes.

Keywords: SRAM, reliability, stability, noise margin, modeling

REFERENCES
Criticality Computation in Parameterized Statistical Timing

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ABSTRACT
Chips manufactured in 90 nm technology have shown large parametric variations, and a worsening trend is predicted. These parametric variations make circuit optimization difficult since different paths are frequency-limiting in different parts of the multi-dimensional process space. Therefore, it is desirable to have a new diagnostic metric for robust circuit optimization. This paper presents a novel algorithm to compute the criticality probability of every edge in the timing graph of a design with linear complexity in the circuit size. Using industrial benchmarks, we verify the correctness of our criticality computation via Monte Carlo simulation. We also show that for large industrial designs with 442,000 gates, our algorithm computes all edge criticalities in less than 160 seconds.

Keywords: Criticality probability, Statistical timing, Parametric variation

REFERENCES
Mixture Importance Sampling and Its Application to the Analysis of SRAM Designs in the Presence of Rare Failure Events

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ABSTRACT
In this paper, we propose a novel methodology for statistical SRAM design and analysis. It relies on an efficient form of importance sampling, mixture importance sampling. The method is comprehensive, computationally efficient and the results are in excellent agreement with those obtained via standard Monte Carlo techniques. All this comes at significant gains in speed and accuracy, with speedup of more than 100X compared to regular Monte Carlo. To the best of our knowledge, this is the first time such a methodology is applied to the analysis of SRAM designs.

Keywords: Statistical Performance Analysis, Yield Prediction, SRAM

REFERENCES
ABSTRACT
Although many physical limitations have been reached in modern micro-lithography, printed critical dimensions continue to shrink according to the International Technology Roadmap for Semiconductors (ITRS) [1]. To meet the demands imposed by this guideline, the traditional separation between design and manufacturing communities is being bridged. Many EDA tools package manufacturing data for delivery into established simulation engines for design verification. However, none of them provide practical implementations of design optimizations at an early stage in the design flow.

This paper presents an automated layout modification flow for metal layers with the goal of enhancing manufacturability. It can easily be deployed in a current custom design flow in a way that is visible to designers. The result of this scheme is improvements to process windows and yield, while minimizing circuit performance detractors. The flow is verified through analyses of both the impact on circuit performance and the benefit to manufacturability. It has been implemented in a state-of-the-art 65 nm chip design. Both silicon yield and electrical performance data are currently being collected and analyzed.

Keywords: DFM, OPC, layout, design flow

REFERENCES
Abstract:
Creating ICs in the nanometer age is a high-stakes race that few companies can afford to compete in – and even fewer can win. Hear how senior technologists from the world’s top technology companies are striving to improve their chances of success. Will leakage constraints force power-sensitive applications to stay with older technologies, or will there be a bifurcation to a new process technology? Will ballooning capital equipment expenses delay new capacity or price out design rules for mainstream applications? Will silicon-on-insulator and new device structures like FinFETs force rethinking of design, modeling and simulation methodologies? And which EDA technologies, delivered when, will be critical for victory? These senior technologists, from some of the biggest companies in the high tech industry, will discuss and debate how they think the overall industry will successfully transition to the nanometer age. Specific examples from the technologists’ broad exposure to industry trends and competitors will help illustrate their forecasts and predictions.

Keywords: Hardware
Use of C/C++ Models for Architecture Exploration and Verification of DSPs

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ABSTRACT
Architectural decisions for DSP modules are often analyzed using high level C models. Such high-level explorations allow early examination of the algorithms and the architectural trade-offs that must be made for a practical implementation. The same models can be reused during the verification of the RTL subsequently developed, provided that various "hooks" which are desirable during the verification process are considered while creating these high level models. In addition, consideration must be given to the qualitative content of these high level models to permit an optimal verification flow allowing for compromise between features of the model and the completeness of the verification. Thus, high quality design and verification are achieved by the use of valid models and the valid use of models. In this paper, we describe our approach and show examples from a typical image processing application.

Keywords: Verification, C/C++, Simulation, Formal, RTL.

References
Maintaining Consistency Between SystemC and RTL System Designs

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ABSTRACT
We describe how system design consistency can be maintained across multiple levels of design abstraction using a modular verification IP strategy. This strategy involves delivery of verification IP in an environment independent manner, utilizing a standard system verification architecture that leverages re-usable component verification drivers, transaction-based interfaces, and synchronization through a system-verification master. This enables a single test-bench to be applied for systems modeled both in SystemC, as well as at the RT level. The configuration of the verification testbench is kept consistent with the design by using system-design meta-data described using the specifications of The SPIRIT Consortium.

Keywords: Verification, VIP, Testbench, SystemC, TLM, Transactor, RTL, SPIRIT

REFERENCES
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SystemC Transaction Level Models And RTL Verification

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ABSTRACT
This paper describes how systems companies are adopting SystemC transaction level models for system on chip design and verification, and how these transaction level models are being reused for RTL verification. The paper discusses how the task of system verification is changing as systems become more complex and it discusses how companies are striving to eliminate fragmentation within their design and verification flows by leveraging SystemC transaction level models.

Keywords: SystemC, Transaction Level Model, TLM, RTL Verification, Hardware/Software Co-Design, Hardware/Software Co-Verification.

REFERENCES
Towards A C++-based Design Methodology Facilitating Sequential Equivalence Checking

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ABSTRACT
It has long been the practice to create models in C or C++ for architectural studies, software prototyping and RTL verification in the design of Systems-on-Chip (SoC). These models are written in C++ primarily because it is possible to achieve very high simulation speeds, but also because it is productive to code at high levels of abstraction. In this paper we present a modeling methodology that continues to exploit the inherent advantages of writing models in C++ while ensuring that they are usable for formal verification of RTL through the use of sequential equivalence checking technology. An industrial case study is presented to show the validity of the approach.

Keywords: Modeling Methodology, Sequential Equivalence Checking

References
ABSTRACT
Designing an energy efficient power gating structure is an important and challenging task in Multi-Threshold CMOS (MTCMOS) circuit design. In order to achieve a very low power design, the large amount of energy consumed during mode transition in MTCMOS circuits should be avoided. In this paper, we propose an appropriate charge recycling technique to reduce energy consumption during the mode transition of MTCMOS circuits. The proposed method can save up to 46% of the mode transition energy while, in most cases, maintaining, or even improving, the wake up time of the original circuit. It also reduces the peak negative voltage value and the settling time of the ground bounce.

Keywords: MTCMOS, charge recycling, low power design.

REFERENCES
ABSTRACT
In this paper, we propose a novel projection-based algorithm to estimate the full-chip leakage power with consideration of both inter-die and intra-die process variations. Unlike many traditional approaches that rely on log-Normal approximations, the proposed algorithm applies a novel projection method to extract a low-rank quadratic model of the logarithm of the full-chip leakage current and, therefore, is not limited to log-Normal distributions. By exploring the underlying sparse structure of the problem, an efficient algorithm is developed to extract the non-log-Normal leakage distribution with linear computational complexity in circuit size. In addition, an incremental analysis algorithm is proposed to quickly update the leakage distribution after changes to a circuit are made. Our numerical examples in a commercial 90nm CMOS process demonstrate that the proposed algorithm provides 4x error reduction compared with the previously proposed log-Normal approximations, while achieving orders of magnitude more efficiency than a Monte Carlo analysis with 104 samples.

Keywords: Statistical Analysis, Leakage Power

REFERENCES
The application of power gating circuits to semicustom design based on standard-cell elements is limited due to the requirement of customizing cells that are tailored for power gating or the requirement of customizing physical design methodologies for placement and power network. We propose a new power network architecture that enables use of conventional standard-cell elements. A few custom library elements are developed wherever needed, including output interface circuits and data retention storage elements. A novel method of current switch design is also described. The proposed methodology is applied to ISCAS benchmark circuits, and also to a commercial Viterbi decoder with 0.18μm CMOS technology.

Keywords: Power gating, low power, leakage current

References
Challenges in Sleep Transistor Design and Implementation in Low-Power Designs

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ABSTRACT
Optimum power gating sleep transistor design and implementation are critical to a successful low-power design. This paper describes important considerations for the sleep transistor design and implementation including header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency. It also investigated various power-on current rush control methods for the sleep transistor implementation.

Keywords: low-power design, power gating, sleep transistor, methodology.

REFERENCES
A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for Leakage Power Reduction

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ABSTRACT
Input vector control (IVC) technique is based on the observation that the leakage current in a CMOS logic gate depends on the gate input state, and a good input vector is able to minimize the leakage when the circuit is in the sleep mode. The gate replacement technique is a very effective method to further reduce the leakage current. In this paper, we propose a fast algorithm to find a low leakage input vector with simultaneous gate replacement. Results on MCNC91 benchmark circuits show that our algorithm produces 14% better leakage current reduction with several orders of magnitude speedup in runtime for large circuits compared to the previous state-of-the-art algorithm. In particular, the average runtime for the ten largest combinational circuits has been dramatically reduced from 1879 seconds to 0.34 seconds.

Keywords: Input vector control, leakage reduction, gate replacement

REFERENCES
Timing Driven Power Gating

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ABSTRACT
Power Gating is effective for reducing leakage power. Previously, a Distributed Sleep Transistor Network (DSTN) was proposed to reduce the sleep transistor area by connecting all the virtual ground lines together to minimize the Maximum Instantaneous Current (MIC) through sleep transistors. In this paper, we propose a new methodology for determining the size of sleep transistors for the DSTN structure. We present novel algorithms and theorems for efficiently estimating a tight upper bound of the voltage drop. We also present efficient heuristics for minimizing the sizes of sleep transistors. Our experimental results are very exciting.

Keywords: Leakage Current, Power Gating, IR Drop

REFERENCES
A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoring and Analysis: Architectural Design Space Exploration

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ABSTRACT
In this paper we focus on MPSoC architectures for human heart ECG real-time monitoring and analysis. This is a very relevant bio-medical application, with a huge potential market, hence it is an ideal target for an application-specific SoC implementation. We investigate a symmetric multi-processor architecture based on STMicroelectronics VLIW DSPs that process in real-time 12-lead ECG signals. This architecture improves upon state-of-the-art SoC designs for ECG analysis in its ability to analyze the full 12 leads in real-time, even with high sampling frequencies, and ability to detect heart malfunction. We explore the design space by considering a number of hardware and software architectural options.

Keywords: Multiprocessor System-on-Chip, embedded system design, electrocardiogram algorithms, real-time analysis, hardware space exploration

REFERENCES

An Automated, Reconfigurable, Low-Power RFID Tag

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ABSTRACT
This paper describes an ultra low power active RFID tag and its automated design flow. RFID primitives to be supported by the tag are enumerated with RFID macros and the behavior of each primitive is specified using ANSI-C within the template to automatically generate the tag controller. Two power saving components, a passive transceiver/burst switch and a smart buffer, are presented to save power and increase tag lifetime. Based on a test program, the processors required 183, 43, and 19 μJ per transaction for StrongARM, XScale, and EISC processors, respectively. Three hardware controllers using a Fusion FPGA, Coolrunner II CPLD, and ASIC required 13 nJ, 1.3 nJ, and 0.07 nJ per transaction.

REFERENCES
Design Space Exploration and Prototyping for On-chip Multimedia Applications

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ABSTRACT
Traditionally, design space exploration for Systems-on-Chip (SoCs) has focused on the computational aspects of the problem at hand. However, as the number of components on a single chip and their performance continue to increase, a shift from computation-bound to communication-bound design becomes mandatory. Towards this end, this paper presents a comprehensive evaluation of two communication architectures targeting multimedia applications. Specifically, we compare and contrast the Network-on-Chip (NoC) and Point-to-Point (P2P) communication architectures in terms of power, performance, and area. As the main contribution, we present complete P2P and NoC-based implementations of a real multimedia application (MPEG-2 encoder), and provide direct measurements using a FPGA prototype and actual video clips, rather than simulation and synthetic workload. From an experimental standpoint, we show that the NoC architecture scales very well in terms of area, performance, power and design effort, while the P2P architecture scales poorly on all accounts except performance.

Keywords: Networks-on-chip, Point-to-point, System-on-chip, MPEG-2 encoder, FPGA prototype

REFERENCES
Evaluation and Design Trade-Offs Between Circuit-Switched and Packet-Switched NOCs for Application-Specific SOCs

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ABSTRACT
NOC architectures have to deliver good latency-throughput performance in the face of very tight power and area budgets. However, the latency and the power consumption for transferring information down the transmitter stack, through the channel, and up the receiver stack might be unacceptably high. In this paper, we evaluate the designs of packet-switched and the proposed circuit-switched NOC in detail, and we advocate using circuit-switched NOC as it is more attractive for application-specific SOC designs because of communication localization. We implement and synthesize the designs of packet-switched and circuit-switched NOCs, and we take multimedia applications as our case studies. The experimental results show that the area, latency and the energy consumption of the packet-switched NOC are much larger than that of the circuit-switched NOC for application-specific designs.

Keywords: Low-Power, SOC, Application-specific designs, NOC

REFERENCES
Refined Statistical Static Timing Analysis Through Learning Spatial Delay Correlations

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ABSTRACT
Statistical static timing analysis (SSTA) has been a popular research topic in recent years. A fundamental issue with applying SSTA in practice today is the lack of reliable and efficient statistical timing models (STM). Among many types of parameters required to be carefully modeled in an STM, spatial delay correlations are recognized as having significant impact on SSTA results. In this work, we assume that exact modeling of spatial delay correlations is quite difficult, and propose an experimental methodology to resolve this issue. The modeling accuracy requirement is relaxed by allowing SSTA to impose upper bounds and lower bounds on the delay correlations. These bounds can then be refined through learning the actual delay correlations from path delay testing on silicon. We utilize SSTA as the platform for learning and propose a Bayesian approach for learning spatial delay correlations. The effectiveness of the proposed methodology is illustrated through experiments on benchmark circuits.

Keywords: Statistical timing, Bayesian learning, delay correlations

REFERENCES
ABSTRACT
We propose a scalable and efficient parameterized block-based statistical static timing analysis algorithm incorporating both Gaussian and non-Gaussian parameter distributions, capturing spatial correlations using a grid-based model. As a preprocessing step, we employ independent component analysis to transform the set of correlated non-Gaussian parameters to a basis set of parameters that are statistically independent, and principal components analysis to orthogonalize the Gaussian parameters. The procedure requires minimal input information: given the moments of the variational parameters, we use a Padé approximation-based moment matching scheme to generate the distributions of the random variables representing the signal arrival times, and preserve correlation information by propagating arrival times in a canonical form. For the ISCAS89 benchmark circuits, as compared to Monte Carlo simulations, we obtain average errors of 0.99% and 2.05%, respectively, in the mean and standard deviation of the circuit delay. For a circuit with $|G|$ gates and a layout with $g$ spatial correlation grids, the complexity of our approach is $O(g|G|)$.

Keywords: Non-Gaussian, Statistical Timing, Independent Component Analysis, Moment Matching

REFERENCES
Statistical Timing Based on Incomplete Probabilistic Descriptions of Parameter Uncertainty

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ABSTRACT
Existing approaches to timing analysis under uncertainty are based on restrictive assumptions. Statistical STA techniques assume that the full probabilistic distribution of parameter uncertainty is available; in reality, the complete probabilistic description often cannot be obtained. In this paper, a new paradigm for parameter uncertainty description is proposed as a way to consistently and rigorously handle partially available descriptions of parameter uncertainty. The paradigm is based on a theory of interval probabilistic models that permit handling uncertainty that is described in a distribution-free mode - just via the range, the mean, and the variance. This permits effectively handling multiple real-life challenges, including imprecise and limited information about the distributions of process parameters, parameters coming from different populations, and the sources of uncertainty that are too difficult to handle via full probabilistic measures (e.g. on-chip supply voltage variation). Specifically, analytical techniques for bounding the distributions of probabilistic interval variables are proposed. Besides, a provably correct strategy for fast Monte Carlo simulation based on probabilistic interval variables is introduced. A path-based timing algorithm implementing the novel modeling paradigm, as well as handling the traditional variability descriptions, has been developed. The results indicate the proposed algorithm can improve the upper bound of the 90\textsuperscript{th} percentile circuit delay, on average, by 5.3\% across the ISCAS’85 benchmark circuits, compared to the worst-case timing estimates that use only the interval information of the partially specified parameters.

REFERENCES


Probabilistic Interval-Valued Computation: 
Toward a Practical Surrogate for Statistics Inside CAD Tools

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Abstract
Interval methods offer a general, fine-grain strategy for modeling correlated range uncertainties in numerical algorithms. We present a new, improved interval algebra that extends the classical affine form to a more rigorous statistical foundation. Range uncertainties now take the form of confidence intervals. In place of pessimistic interval bounds, we minimize the probability of numerical “escape”; this can tighten interval bounds by 10X, while yielding 10-100X speedups over Monte Carlo. The formulation relies on three critical ideas: liberating the affine model from the assumption of symmetric intervals; a unifying optimization formulation; and a concrete probabilistic model. We refer to these as probabilistic intervals, for brevity. Our goal is to understand where we might use these as a surrogate for expensive, explicit statistical computations. Results from sparse matrices and graph delay algorithms demonstrate the utility of the approach, and the remaining challenges.

Keywords: Intervals, DFM, algorithms

References
Decision-Making for Complex SoCs in Consumer Electronic Products

Chair: Ron Wilson - EDN, San Mateo, CA
Speakers: Charlie Matar, Qualcomm CDMA Technologies, San Diego, CA
Riko Radojcic, Qualcomm CDMA Technologies, San Diego, CA
Rene Delgado, Freescale, Semiconductor, Inc., Austin, TX
Dawn Fitzgerald, Aurora Enterprises, Boston, MA
Mario Manninger, austriamicrosystems AG, Unterpremstaetten, Austria

Abstract
Consumer electronics chips are the technology drivers today. They require different types of optimizations and thus the need to adopt emerging solutions to meet such requirements. Optimizing for high volume production, low power, and shrinking sizes necessitate adequate trade-off analysis and technical/business decision making by management. The lead managers in this session will discuss today's emerging solutions and their economic impact.
Entering the Hot Zone — Can You Handle the Heat and Be Cool?

Chair
Daya Nadamudi, Gartner Dataquest, San Jose, CA

Panelists:
Andrew Yang - Apache Design Solutions, Mountain View, CA
Javier A. DeLaCruz - eSilicon, New Providence, NJ
Rajit Chandra - Gradient Design Automation, Santa Clara, CA
Sribalan Santhanam - P.A. Semi, Santa Clara, CA
Simon Burke - ATI Technologies, Santa Clara, CA
Uming Ko - Texas Instruments, Dallas, Texas

ABSTRACT
With the latest gaming systems such as X-box, Playstation 3, PSP, IPTV, and H264 requiring more bandwidth, packaged in smaller devices, and providing higher quality, in return they evacuate more heat and consume more power, thus making power consumption and thermal dissipation a major issue for chip designers in the nanometer era.

Thermal effects on the chip and package is the next wave. First, there was signal integrity. Then power integrity and now, there is a new first-order effect in the horizon for IC and system designers called thermal integrity. And the traditional design methodology of using uniform temperature across the chip is becoming woefully inadequate and provides insufficient data to the package and system designers, unable to meet the requirement and demands of the consumer. To better understand the impact of temperature variation on chip’s performance, both power distribution and package characteristics must be considered in the design and analysis flow. Likewise, a realistic view of the heat distribution across the chip is becoming essential for package and system designers. What makes the analysis of signal, power, and thermal integrity effects challenging is that they must all be considered concurrently across the entire chip, which requires novel approaches to mitigate the issue.

The panel will discuss how urgent is the impact of thermal integrity on system designs and is this a real concern or are we making it up? When and under what condition will it become urgent, and is it related to process nodes, low power applications, type of packaging used, etc.? Is there specific design techniques used for more specific multimedia processing? Can you separate the IC design from package and system designs with some assumptions or is co-design the only way? How accurate is the industry’s understanding of the physics of the chip (device), interconnect, and package? Is thermal integrity a first order or second order effect? Given the other variations from nominal, how important is this? The moderator will conclude with a summary of the panelist comments and be able to make a forward-looking statement about the future of power and heat and their impact on system design.

Keywords: Thermal effects, Low power, IC packaging
Reliability Challenges for 45nm and Beyond

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ABSTRACT

Scaling, for enhanced performance and cost reduction, has pushed existing CMOS materials much closer to their intrinsic reliability limits. This will require that designers will have to be very careful with: high current densities, voltage overshoots, localized hot spots on the chip, high duty-cycle applications, and high thermal-resistance packaging. In addition to the reliability issues, interconnect RC time-delay will worsen with scaling because Cu resistivity is expected to increase due to surface and grain boundary scattering in very narrow interconnects. Also, the low-k interconnect-dielectric introduction rate has been much slower than ITRS roadmap forecasts.

Keywords: CMOS, reliability, scaling, design, materials

References

Design Tools for Reliability Analysis

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ABSTRACT
Recent progress in EDA tools allows IC designs to be accurately verified with consequent improvements in yield and performance through reduced guard bands. This paper will present a tools perspective, including the primary effects such as HCI, NBTI and EM for which EDA tools are available, types of tools (dynamic simulation vs. static rule checking) and necessary reliability infrastructure and flows that have been working in practice. Finally, developing areas and future opportunities will be addressed.

Keywords: HCI, NBTI, EM, Reliability simulation, Design-in Reliability.

REFERENCES
ABSTRACT
Silicon design implementation has become increasingly complex with the deep submicron technologies such as 90nm and below. It is common to see multiple processor cores, several types of memories, I/Os, complex analog circuits and synthesized logic on the same chip. Sophisticated IP integration techniques are needed in order to realize today’s complex systems-on-chip (SoC). Also, with the explosive growth in the communications semiconductor market, ensuring product reliability to meet reliability goals and achieve good yield is of significant concern. This paper is intended to bring the inherent challenges in the reliability domain and some of the effective techniques currently used in the EDA world to meet these challenges. We also discuss the need for developing new methods to address the upcoming challenges in ultra-deep submicron design environment.

Keywords: Reliability, nanometer design challenges, EDA tools, Electro Migration, Self Heat

REFERENCES
[1] Enabling DIR (Design In Reliability) through CAD capabilities, ISQED 2000, SEMATECH DIR Team.
[2] Panel: When bad things happen to good chips: By Ray Hokinson - Compaq Computer Corp., Shrewsbury, MA; Sung-Mo Kang - Univ. of Illinois, Urbana, IL; Wonjae Kang - Intel Corp., Santa Clara, CA; Sani Nassif - IBM Corp., Austin, TX; David Overhauser - Simplex Solutions, Sunnyvale, CA; Tak Young - Monterey Design, Sunnyvale, CA
ABSTRACT
Voltage analysis is a major part of design-in reliability as voltage is the driver for electric degradation in dielectrics and MOS devices. Particularly, voltage has the largest influence on gate oxide reliability. An important trend designers should be aware of is the planned shift to new gate oxide failure criteria, which will tolerate progressive soft breakdowns in the gate oxide introducing additional gate leakage and noise. With increasing electric oxide fields negative bias instability of pFET devices became a severe problem, which cannot be solved by technology alone but requires also design solutions. Thus, simulation of MOSFETs being degraded by hot carrier stress and negative bias temperature stress becomes mandatory, as well as the control of device properties of circuit elements in a design. Design-in reliability in the metallization levels mainly is related to via placing and therefore, design tools should be able to trade off between increase in size, e.g. due to redundant vias, and benefit in reliability. Analysis of metal lines with maximum potential difference and minimal spacing also becomes mandatory in order to calculate the risk of time-dependent dielectric breakdown in the inter-metal dielectric, particularly for low-k dielectrics. From ESD point of view the following demands exist for future EDA solutions: 1) verification of net oriented ESD rules, 2) IR-drop analysis on layout to check ESD metallization rules, and 3) automatic placement of ESD or I/O cells depending on some formalized ESD guide lines that codify the ESD protection concept.

Key Words: Design-in reliability, gate oxide integrity, hot carrier stress, NBTI, electromigration, stress-induced voiding, TDDB of inter-metal dielectric, ESD

REFERENCES
[27] R. Thewes et al., European Solid-State Device Research Conf. (ESSDERC), pp. 73-80, 2001
ABSTRACT
Much research has been done lately concerning analysis and optimization techniques for on-chip power grid networks. However, all of these approaches assume a particular model or behavior of the power delivery. In this paper, we describe the first detailed full-die dynamic model of an industrial microprocessor design, including package and non-uniform decap distribution. This model is justified from the ground up using a full-wave model and then increasingly larger but less detailed models with only the irrelevant elements removed. Using these models we show that there is little impact of on-die inductance in such a design, and that the package is critical to understanding resonant properties of the grid. We also show that transient effects are sensitive to non-uniform de-cap distribution and that locality is a tight function of frequency and of the package-die resonance, producing newly explained localized resonant effects. Specifically, all of these points have impact on what kind of analysis and optimization are required from CAD.

Keywords: IR, Ldi/dt, decap, resonance, locality, power supply networks.

REFERENCES
Fast Analysis of Structured Power Grid by Triangularization Based Structure Preserving Model Order Reduction

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ABSTRACT
In this paper, a Triangularization Based Structure preserving (TBS) model order reduction is proposed to verify power integrity of on-chip structured power grid. The power grid is represented by interconnected basic blocks according to current density, and basic blocks are further clustered into compact blocks, each with a unique pole distribution. Then, the system is transformed into a triangular system, where compact blocks are in its diagonal and the system poles are determined only by the diagonal blocks. Finally, projection matrices are constructed and applied for compact blocks separately. The resulting macromodel has more matched poles and is more accurate than the one using flat projection. It is also sparse and enables a two-level analysis for simulation time reduction. Compared to existing approaches, TBS in experiments achieves up to 133X and 109X speedup in macromodel building and simulation respectively, and reduces waveform error by 33X.

Keywords: Model Order Reduction, PG grid simulation

REFERENCES
Stochastic Variational Analysis of Large Power Grids Considering Intra-die Correlations

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ABSTRACT
For statistical timing and power analysis that are very important problems in the sub-100nm technologies, stochastic analysis of power grids that characterizes the voltage fluctuations due to process variations is inevitable. In this paper, we propose an efficient algorithm for the variational analysis of large power grids in the presence of a significant number of Gaussian intra-die process variables that are correlated. We consider variations in the power grid’s electrical parameters as spatial stochastic processes and express them as linear expansions in an orthonormal series of random variables using the Karhunen-Loève (KLE) method. The voltage response is then represented as an orthonormal polynomial series and the coefficients are obtained optimally using the Galerkin method. We propose a novel method to separate the stochastic analysis for the random variables that effect only the inputs (e.g, drain currents) and for those that effect the system parameters as well (e.g., conductance, capacitance). We show that this parallelism can result in significant speed-ups in addition to the speed-ups inherent to Galerkin-based methods. Our analysis has been applied to several industrial power grids and the results show speed-ups of up to two orders of magnitude over Monte Carlo simulations for comparable accuracy.

Keywords: Power Grids, Process Variations, Correlations, Stochastic Analysis, Polynomial Chaos, Orthonormal Polynomials

REFERENCES
A Fast On-Chip Decoupling Capacitance Budgeting Algorithm Using Macromodeling and Linear Programming

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Freescale Semiconductor, Inc.

ABSTRACT
We propose a novel and efficient charge-based decoupling capacitance budgeting algorithm. Our method uses the macromodeling technique and effective radius of decoupling capacitance to reduce the size of the problem. We formulate the nonlinear optimization into a linear program (LP) by integrating the nodal equations across a time period of interest and through certain approximations. To reduce the error caused by linearization, we do multiple iterations of the linear program. Experimental results demonstrate that, with the proposed algorithm, even very large power networks (eg. 5 million nodes) can be optimized in a couple of hours with 1-2 transient analyses. Comparison of our algorithm with another heuristic method shows area efficiency and run time advantage of our method.

Keywords: Decoupling capacitance, budgeting, macromodeling, sequence of linear programming

REFERENCES
ABSTRACT
Dynamic BDD reordering is usually a computationally-demanding process, and may slow down BDD-based applications. We propose a novel algorithm for distributing this process over a number of computers, improving both reordering time and application time. Our algorithm is based on Rudell’s popular sifting algorithm, and takes advantage of a few empirical observations we make regarding Rudell’s algorithm. Experimental results show the efficiency and scalability of our approach, when applied within an industrial model checker.

Keywords: Model checking, BDD, reordering, distributed computing.

REFERENCES
**SAT Sweeping with Local Observability Don't-Cares**

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**Abstract**

SAT sweeping is a method for simplifying an AND/INVERTER graph (AIG) by systematically merging graph vertices from the inputs towards the outputs using a combination of structural hashing, simulation, and SAT queries. Due to its robustness and efficiency, SAT sweeping provides a solid algorithm for Boolean reasoning in functional verification and logic synthesis. In previous work, SAT sweeping merges two vertices only if they are functionally equivalent. In this paper we present a significant extension of the SAT-sweeping algorithm that exploits local observability don't-cares (ODCs) to increase the number of vertices merged. We use a novel technique to bound the use of ODCs and thus the computational effort to find them, while still finding a large fraction of them. Our reported results based on a set of industrial benchmark circuits demonstrate that ODC-based SAT sweeping results in significantly more graph simplification with great benefit for Boolean reasoning with a moderate increase in computational effort.

**Keywords:** And/inverter graphs, SAT sweeping, observability

**References**


Predicate Learning and Selective Theory Deduction for a Difference Logic Solver

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Abstract

Design and verification of systems at the Register-Transfer (RT) or behavioral level require the ability to reason at higher levels of abstraction. Difference logic consists of an arbitrary Boolean combination of propositional variables and difference predicates and therefore provides an appropriate abstraction. In this paper, we present several new optimization techniques for efficiently deciding difference logic formulas. We use the lazy approach by combining a DPLL Boolean SAT procedure with a dedicated graph-based theory solver, which adds transitivity constraints among difference predicates on a “need-to” basis. Our new optimization techniques include flexible theory constraint propagation, selective theory deduction, and dynamic predicate learning. We have implemented these techniques in our lazy solver. We demonstrate the effectiveness of the proposed techniques on public benchmarks through a set of controlled experiments.

Keywords: Difference logic, decision procedure, SMT solver, SAT

References


Fast Illegal State Identification for Improving SAT-Based Induction

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ABSTRACT
In this paper, we propose a novel framework to quickly extract illegal states of a sequential circuit and then use them as constraints during the SAT-based induction runs. First, we employ a low-cost combinational ATPG to identify unreachable partial-states among groups of related flip-flops. Second, we propose the concept of necessary-assignment looping to identify additional unachievable partial-states. Third, we extend the above unachievability theory to capture new non-trivial sequential logic dependencies among the circuit signals. Finally, we use a unified framework that utilizes all the above information and aims at maximizing the learning. All the learned illegal states are converted into constraint clauses and are replicated at all the unrolled transition relations to prune the searchspace. Experimental results show that, due to the added constraints, many safety properties can be proved at earlier depths and the induction run-times can be significantly reduced.

Keywords: Induction, SAT, ATPG, Learning

REFERENCES
A Multi-port Current Source Model for Multiple-Input Switching Effects in CMOS Library Cells

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ABSTRACT
The problem of multiple-input switching (MIS) has been mostly ignored by the timing CAD community. Not modeling MIS for timing can result in as much as 100% error in stage delay and slew calculation. The impact is especially severe on stages immediately after a bank of flops, where the inputs have a high probability of arriving simultaneously. Other problems such as modeling of interconnect loads, complex (nonlinear/non-monotonic) input waveforms, power-droop impact on cell delay, nonlinear input capacitances, delay variations due to cross-capacitance, etc. are also known sources of error. In this paper, we introduce the multi-port current source model (MCSM). MCSM can efficiently handle an arbitrary number of simultaneously switching inputs, including single-input switching (SIS). Moreover, MCSM is comprehensive in that other modeling problems associated with delay and noise computation are elegantly covered. We demonstrate the applicability of MCSM on a large 65 nm industrial test-case. For cells experiencing MIS, the model yields delay and slew-rate errors within ±5% for 88.3% and 93.0% of the cases, respectively. We also present data that show that MCSM is an effective receiver model which captures active loading effects without incurring significant additional error. MCSM makes combined cell-level timing, noise, and power analysis a possibility.

Keywords: multiple input switching, current source model, timing analysis, cell library characterization, cell model, MCSM

REFERENCES
Statistical Logic Cell Delay Analysis Using a Current-based Model

Hanif Fatemi, Shahin Nazarian, Massoud Pedram
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Abstract
A statistical model for the purpose of logic cell timing analysis in the presence of process variations is presented. A new current-based cell delay model is utilized, which can accurately compute the output waveform for input waveforms of arbitrary shapes subjected to noise. The cell parasitic capacitances are pre-characterized by lookup tables to improve the accuracy. To capture the effect of process parameter variations on the cell behavior, the output voltage waveform of logic cells is modeled by a stochastic Markovian process in which the voltage value probability distribution at each time instance is computed from that of the previous time instance. Next the probability distribution of \( \alpha \% V_{dd} \) crossing time, i.e., the hitting time of the output voltage stochastic process is computed. Experimental results demonstrate the high accuracy of our cell delay model compared to Monte-Carlo-based SPICE simulations.

Keywords: Statistical gate timing analysis, Crosstalk noise, Process variations

References
Multi-Shift Quadratic Alternating Direction Implicit Iteration for High-Speed Positive-Real Balanced Truncation

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**School of Electrical and Computer Engg, Purdue University, IN, USA

ABSTRACT
This paper presents a multi-shift generalization of the recently proposed quadratic alternating direction implicit (QADI) iteration. QADI and its Cholesky Factor (CF) variant, CFQADI, have been shown to be efficient ways of solving the large-scale algebraic Riccati equations (AREs) required in positive-real balanced truncation (PRBT). However, only their single-shift implementations have been considered so far. Using linear fractional transformation (LFT), we present elegant multi-shift extensions of both QADI and CFQADI, thereby enabling even faster and more accurate PRBT.

Keywords: Model order reduction, positive real, balanced truncation, ADI

REFERENCES
ABSTRACT

Passivity in a VLSI model is an important property to guarantee stable global simulation. Most VLSI models are naturally described as descriptor systems (DSs) or singular state spaces. Passivity tests for DSs, however, are much less developed compared to their nonsingular state space counterparts. For large-scale DSs, the existing test based on linear matrix inequality (LMI) is computationally prohibitive. Other system decoupling techniques involve complicated coding and sometimes ill-conditioned transformations. This paper proposes a simple DS passivity test based on the key insight that the sum of a passive system and its adjoint must be impulse-free. A sidetrack shows that the proper (non-impulsive) part of a passive DS can be easily decoupled along the test flow. Numerical examples confirm the effectiveness of the proposed DS passivity test over conventional approaches.

Keywords: Descriptor system, positive real, passivity test

REFERENCES


Model Order Reduction of Linear Networks With Massive Ports via Frequency-Dependent Port Packing

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ABSTRACT
Model order reduction has been a driving force for reducing analysis complexity of VLSI systems containing large linear networks. However, most existing reduction techniques are only applicable to networks with a small number of ports, failing to fulfill an even stronger need of reducing massively interconnected subsystems such as power grids and wide buses. In this paper, a port packing scheme is presented wherein the correlation between circuit ports is explored in a frequency-dependent manner. In the proposed McPack (Multiport Circuit Packing) algorithm, port packing is combined with a practical realization of the recently developed tangential interpolation scheme for model reduction. McPack performs feasible moment matching for networks with many ports in the sense of tangential interpolation. With guaranteed passivity, extensibility to multi-point expansion as well as comparable complexity, McPack systematically introduces frequency-domain port packing into the existing projection-based model order reduction framework. For several large networks with high port count, the presented algorithm is shown to be significantly more accurate than the standard block-moment matching algorithm as well as other recently developed alternative.

Keywords: Model order reduction, multi-port networks.

REFERENCES
Tradeoffs and Choices for Emerging SoCs in High-End Applications

Chair: Nic Mokhoff - EE Times, Manhasset, NY
Speakers: Ken Wagner, PMC-Sierra, Inc., British Columbia, Canada
         Rajesh Shah - Open-Silicon, North Milpitas, CA
         Rajesh Galivanche - Intel Corp., Santa Clara, CA
         Kee Sup Kim – Intel Corp., Folsom, CA

Abstract
Design and manufacturing flows and methodologies are directly impacted by the demand for emerging SoCs with increasing performance and parallelism. Moving to new semiconductor technology nodes can significantly affect the choices of suppliers. This session will provide an overview of changing needs and corresponding management decision criteria to make the right choices from a pool of alternate options for flows, methodologies and suppliers.
Overview of the MPSoC Design Challenge

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ABSTRACT
We review the design challenges faced by MPSoC designers at all levels. Starting at the application level, there is a need for programming models and communications APIs that allow applications to be easily re-configured for many different possible architectures without tedious rewriting, while at the same time ensuring efficient production code. Synchronisation and control of task scheduling may be provided by RTOS's or other scheduling methods, and the choice of programming and threading models, whether symmetric or asymmetric, has a heavy influence on how best to control task or thread execution. Debugging MP systems for the typical application developer becomes a much more complex job, when compared to traditional single-processor debug, or the debug of simple MP systems that are only very loosely coupled. The interaction between the system, applications and software views, and processor configuration and extension, adds a new dimension to the problem space. Zeroing in on the optimal solution for a particular MPSoC design demands a multi-disciplinary approach. After reviewing the design challenges, we end by focusing on the requirements for design tools that may ameliorate many of these issues, and illustrate some of the possible solutions, based on experiments.

Keywords: MPSoC, Multi-Processor System-on-Chip, System-Level Design,

REFERENCES
Programming models and HW-SW Interfaces Abstraction for Multi-Processor SoC

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ABSTRACT
For the design of classic computers the Parallel programming concept is used to abstract HW/SW interfaces during high level specification of application software. The software is then adapted to existing multiprocessor platforms using a low level software layer that implements the programming model. Unlike classic computers, the design of heterogeneous MPSoC includes also building the processors and other kind of hardware components required to execute the software. In this case, the programming model hides both hardware and software refinements. This paper deals with parallel programming models to abstract both hardware and software interfaces in the case of heterogeneous MPSoC design. Different abstraction levels will be needed. For the long term, the use of higher level programming models will open new vistas for optimization and architecture exploration like CPU/RTOS tradeoffs.

Keywords: Programming models, HW/SW interfaces, Heterogeneous MPSoC

REFERENCES
ABSTRACT
In this paper, we describe the challenges users face for software development on Systems on Chip (SoC) involving multiple cores. We will briefly review the trends and challenges for MPSoC design and will derive from them the resulting requirements. We will then discuss briefly the required exploration tools and close with an analysis of which type of providers will be able to provide appropriate solutions to the MPSoC challenge.

Keywords: Multicore, Simulation, Debugging, Software Development

REFERENCES
Design of a 125µW, Fully-Scalable MPEG-2 and H.264/AVC Video Decoder for Mobile Applications

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**MediaTek Inc., HsinChu, Taiwan, ROC

ABSTRACT
A design of MPEG-2 and H.264/AVC video decoder is demonstrated in a 0.18µm CMOS [1]. The key design issues involved in this advanced IC are discussed, including improving area and power efficiency. Power dissipation is greatly lowered through the architectural exploration. Measurement results show that MPEG-2 and H.264/AVC real-time decoding of QCIF@15fps are achieved at 1.15MHz with power dissipation of 108µW and 125µW respectively at 1V supply voltage.

Keywords: MPEG-2, H.264/AVC, Mobile, Low-power.

REFERENCES
A CMOS SoC for 56/18/16 CD/DVD-dual/RAM Applications

Jyh-Shin Pan, Hao-Cheng Chen, Bing-Yu Hsieh, Hong-Ching Chen, Roger Lee, Ching-Ho Chu, Yuan-Chin Liu, Chuan Liu, Lily Huang, Chang-Long Wu, Meng-Hsueh Lin, Chun-Yiu Lin, Shang-Nien Tsai, Jenn-Ning Yang, Chang-Po Ma, Yung Cheng, Shu-Hung Chou, Hsiu-Chen Peng, Peng-Chuan Huang, Benjamin Chiu, Alex Ho
MediaTek Inc., Hsin-Chu City, Taiwan, R.O.C.

ABSTRACT
A SoC, integrating RF/AFE and 1.5 Gb/s SATA PHY, is presented. It supports 471 Mb/s bit-rate at 18xS DVD. A partial parity mode reduces SDRAM bandwidth. A power control mode minimizes system clock rate. The SoC has 10M transistors, occupies 5.4 x 5.1 mm2 in 0.18 mm CMOS process, and consumes 772 mW during 16xS DVD read.

Keywords: DVD-RAM, Optical Storage, WSR, SATA, CMOS

REFERENCE
Hierarchical Power Distribution and Power Management Scheme for a Single Chip Mobile Processor


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***Hitachi, Ltd., Kokubunji, Tokyo, Japan
****NTT DoCoMo, Inc., Yokosuka, Kanagawa, Japan

ABSTRACT

A hierarchical power distribution methodology that enables more than dozen power domains in a chip and a power management scheme using 20 power domains are described. This method can achieve very low leakage current in the partial active mode of a single chip mobile processor. The single chip mobile processor embedded three CPU’s that is baseband processor, application processor, and multi-media processor. In the “waiting for calling” mode of the mobile handsets, application processor and multimedia processor part can be power-off. This chip can power off these power domains although the some of baseband parts are actively operating. Many new techniques for multiple power domains in the chip are described.

Keywords: VLSI, power domain, partial power off, mobile processor.

REFERENCES

Buffer Insertion in Large Circuits with Constructive Solution Search Techniques

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ABSTRACT
Most existing buffer insertion algorithms, such as van Ginneken's algorithm, consider only individual nets. As a result, these algorithms tend to over buffer when applied to combinational circuits, since it is difficult to decide how many buffers to insert in each net. Recently, Sze, et al. [1] proposed a path-based algorithm for buffer insertion in combinational circuits. However their algorithm is inefficient for large circuits when there are many critical paths. In this paper, we present a new buffer insertion algorithm for combinational circuits such that the timing requirements are met and the buffer cost is minimized. Our algorithm iteratively inserts buffers in the circuit to improve the circuit delay. The core of this algorithm is simple but effective technique that guides the search for a good buffering solution. Experimental results on ISCAS85 circuits show that our new algorithm on average uses 36% less buffers and runs 3 times faster than Sze's algorithm.

Keywords: Buffer Insertion, Cost optimization, Physical Design, Interconnect synthesis

REFERENCES
Low-Power Repeater Insertion With Both Delay and Slew Rate Constraints

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ABSTRACT
In this paper, a novel repeater insertion algorithm is presented to minimize the power dissipation of interconnect trees under given timing budgets and slew rate constraints. In contrast to traditional bottom-up dynamic programming approaches, the proposed algorithm combines a Lagrangian relaxation framework and a graph-based search method to derive possible solutions in a top-down fashion. As a result, it is capable of analyzing repeater slew rates efficiently. In addition, our scheme incorporates accurate circuit models and is therefore able to capture the precise delay and slew rate information, leading to high-quality interconnect designs. We have applied our scheme to interconnects of different topologies and various timing and slew rate constraints. Experimental results demonstrate the effectiveness of our approach in comparison with previous low-power repeater insertion schemes. Under tight timing constraints, our scheme can always derive repeater insertion solutions that meet both delay and slew rate requirements, whereas other schemes often fail. Under loose timing constraints, our algorithm achieves up to a 23% average power dissipation reduction for different interconnects specifications with shorter runtimes.

Keywords: Repeater Insertion, Interconnect, Slew Rate, Low Power

REFERENCES
Fast Algorithms For Slew Constrained Minimum Cost Buffering

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†IBM Austin Research Laboratory, Austin, Texas

ABSTRACT
As a prevalent constraint, sharp slew rate is often required in circuit design which causes a huge demand for buffering resources. This problem requires ultra-fast buffering techniques to handle large volume of nets, while also minimizing buffering cost. This problem is intensively studied in this paper. First, a highly efficient algorithm based on dynamic programming is proposed to optimally solve slew buffering with discrete buffer locations. Second, a new algorithm is developed to handle the difficult cases in which no assumption is made on buffer input slew. Third, an adaptive buffer selection approach is proposed to efficiently handle slew buffering with continuous buffer locations. Experiments on industrial netlists demonstrate that our algorithms are very effective and highly efficient: we achieve > 100 speed up and save up to 40% buffer area over the commonly-used van Ginneken style buffering.

Keywords: Buffer Insertion, Slew Constraint, Physical Design

REFERENCES
ABSTRACT
At-speed test of integrated circuits is becoming critical to detect subtle delay defects. Simulation-based functional test is difficult because low-cost testers are unable to supply multiple asynchronous clocks to the IC. Moreover, low-cost testers simply cannot operate at chip speed. Existing structural at-speed test methods are inadequate because they are unable to supply sufficiently-varied functional clock sequences to test complex sequential logic. Moreover, they require tight restrictions on the circuit design. In this paper, we present a new method for GHz-speed structural test of ASICs having no tight restrictions on the circuit design. In the present implementation, any complex at-speed functional clock waveform for 16 cycles can be applied. We also describe a method to test asynchronous clock domains simultaneously. Experimental results for two multi-million gate ASICs demonstrate high at-speed coverage.

Keywords: ASICs, asynchronous clock domains, at-speed, deskewer, structural test, test waveform generator

REFERENCES
Timing-Based Delay Test for Screening Small Delay Defects

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**Texas Instruments, Inc., Dallas, TX

Abstract
The delay fault test pattern set generated by timing unaware commercial ATPG tools mostly affects very short paths, thereby increasing the escape chance of smaller delay defects. These small delay defects might be activated on longer paths during functional operation and cause a timing failure. This paper presents an improved pattern generation technique for transition fault model, which provides a higher coverage of small delay defect that lie along the long paths, using a commercial no-timing ATPG tool. The proposed technique pre-processes the scan flip-flops based on their least slack path and the detectable delay defect size. A new delay defect size metric based on the affected path length and required increase in test frequency is developed. We then perform pattern generation and apply a novel pattern selection technique to screen test patterns affecting longer paths. Using this technique will provide the opportunity of using existing timing unaware ATPG tools as slack based ATPG. The resulting pattern set improves the defect screening capability of small delay defects.

Keywords: delay testing, test generation.

REFERENCES
ABSTRACT

In this paper we motivate the explicit validation of hold-time violations in silicon and propose a method for doing so. New holdtime failure model and test pattern generation methodologies are defined. We outline conditions under which these tests can be applied reliably. We present results of applying these test patterns on a microprocessor and discuss the implications of intermittent failures on the relevance of hazards during timing analysis.

Keywords: Hold time validation, Delay test, ATPG, Timing analysis

References

Practical Methods in Coverage-Oriented Verification of the Merom Microprocessor

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ABSTRACT
Functional coverage is a well known means of measuring verification progress. However, approaches to coverage, such as Coverage Driven and Coverage Oriented approaches, are often difficult or impractical to implement. This paper presents the coverage methodology used in the verification of Merom, Intel's first converged-core microprocessor. We describe practical methods and applied techniques which enabled a high return on a significantly reduced investment in coverage measurement and analysis. Given the tight schedule, this approach provided a clear metric for measuring verification progress and for effectively steering resources to improve the quality of the design under test.

General Terms and Keywords: Logic design. Logic verification. Coverage. Functional coverage.

REFERENCES
Verification of the Cell Broadband Engine™ Processor

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² Sony Computer Entertainment Inc., Tokyo, Japan,
³ Toshiba Corporation, Ohme, Japan

ABSTRACT
Successfully developing an implementation of entirely new chip architecture such as the Cell Broadband Engine™ (Cell BE) processor from scratch is a notable achievement. Consider further the design complexity (234 million transistors) and the project management complexity (5 participating companies, work in 5 different time zones), and the task seems quite challenging. This paper describes how the central verification team staffed by Sony Computer Entertainment Inc. (SCEI), Toshiba Corporation, and IBM, produced on first silicon a Cell BE microprocessor functional enough to boot an operating system and run applications.

Keywords: Processor reference model, Directed random verification, Hierarchical verification, Trace-based verification

REFERENCES
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Shielding Against Design Flaws with Field Repairable Control Logic

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ABSTRACT
Correctness is a paramount attribute of any microprocessor design; however, without novel technologies to tame the increasing complexity of design verification, the amount of bugs that escape into silicon will only grow in the future. In this paper, we propose a novel hardware patching mechanism that can detect design errors which escaped the verification process, and can correct them directly in the field. We accomplish this goal through a simple field-programmable state matcher, which can identify erroneous configurations in the processor’s control state and switch the processor into formally-verified degraded performance mode, once a “match” occurs. When the instructions exposing the design flaw are committed, the processor is switched back to normal mode. We show that our approach can detect and correct infrequently-occurring errors with almost no performance impact and has approximately 2% area overhead.

Keywords: Hardware patching, Processor verification.

REFERENCES
Scheduling-based Test-case Generation for Verification of Multimedia SoCs


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ABSTRACT

Multimedia SoCs are characterized by a main controller that directs the activity of several cores, each of which is in charge of a stage in the processing of a media stream. The verification of these SoCs is a significant challenge due to time-to-market constraints and system complexity. We present a novel approach to system-level, random test case generation for multimedia SoCs, and a tool, called SoCVer, that implements this approach. We use the SoC’s main controller point of view for controlling the flow of data in the SoC. Test case generation is done by allocating processing tasks to the various cores and determining which core processes which data item at what time. Solving these scheduling problems allows SoCVer to generate software for the SoC’s main controller; this software coordinates and synchronizes the operations of all the cores on the chip without the need for the real operational software. We demonstrate the use of SoCVer using a DVD player SoC.

Keywords: Functional Verification, System on a Chip, Test Generation

References

Rapid and Low-Cost Context-Switch through Embedded Processor Customization for Real-Time and Control Applications

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ABSTRACT
In this paper, we present a methodology for low-cost and rapid context switch for multithreaded embedded processors with realtime guarantees. Context-switch, which involves saving and restoring the thread state, has constituted not only a large performance overhead for many multithreaded embedded systems, but also an obstacle creating a significant delay in the response time for many time-critical control applications. The proposed technique exploits application information extracted during compile time to make sure that only a minimal amount of thread state is saved and subsequently restored on preemption. The register liveness within the application inner loops is analyzed and a few points, referred to as switch points, are identified where the program has minimal number of live registers. At run-time the preemption point is deferred to a switch point and the Real-Time Operating System (RTOS) kernel invokes a switch point specific code generated by the compiler to save and restore the thread state in a custom fashion. Through the utilization of these novel mechanisms, a drastic improvement on both performance and response time is achieved. The presented experimental results demonstrate the effectiveness of the proposed technique on a number of widely-used computational kernels and embedded applications.

REFERENCES
Efficient Detection and Exploitation of Infeasible Paths for Software Timing Analysis

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Department of Computer Science, National University of Singapore

ABSTRACT
Accurate estimation of the worst-case execution time (WCET) of a program is important for real-time embedded software. Static WCET estimation involves program path analysis and architectural modeling. Path analysis is complex due to the inherent difficulty in detecting and exploiting infeasible paths in a program’s control flow graph. In this paper, we propose an efficient method to exploit infeasible path information for WCET estimation without resorting to exhaustive path enumeration. We demonstrate the efficiency of our approach for some real-life control-intensive applications.

Keywords: WCET analysis, infeasible path detection

REFERENCES
Leakage-Aware Intraprogram Voltage Scaling for Embedded Processors

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ABSTRACT
With scaling of technology feature sizes, the share of leakage in total power consumption of digital systems continues to grow. Conventional dynamic voltage scaling (DVS) techniques fail to accurately address the impact of scaling on system power consumption and hence, are incapable of achieving energy efficient solutions. To overcome this problem, we utilize adaptive body biasing (ABB) to adjust transistors' threshold voltage at runtime. We develop a leakage-aware compilation methodology that targets embedded processors with both DVS and ABB capabilities. Our technique has the unique advantage of jointly optimizing active and leakage energy dissipation. Considering the delay and energy penalty of switching between operating modes of the processor and under deadline constraint, our compiler improves the energy consumption of the generated code by average of 13.07% and up to 30.26% at 90nm. While our technique's improvement in energy dissipation over conventional DVS is marginal (4.54%) at 130nm, the average improvement continues to grow to 7.8%, 15.94% and 29.56% for 90nm, 65nm and 45 technology nodes, respectively.

REFERENCES


Building A Common ESL Design and Verification Methodology – Is it Just a Dream?

Chair:    Gary Smith - Gartner-Dataquest, San Jose, CA
Speakers: Anoosh Hosseini - Cisco Systems, Milpitas, CA
        Ashish Parikh - Pixelworks, Inc., Campbell, CA
        H. Tony Chin - HD Lab, Inc., Shin-Yokohama, Japan
        P. Urard - ST Microelectronics, Cedex, France
        Emil Girczyc - Summit Design, Inc., Los Altos, CA
        Simon Bloch - Mentor Graphics Corp., San Jose, CA

Keywords: C/C++, Design, ESL, Methodology, Modeling Rapid Hardware Prototyping, RTL, SystemC, SystemVerilog, Verification

PANEL SUMMARY

In recent years, industry cooperation has established common language and methodology standards to support electronic system level (ESL) modeling, design and verification: SystemC, SystemC Verification (SCV) and SystemC Transaction Level Modeling (TLM). What is still conspicuously absent, is a common, standard methodology for ESL design and verification itself. As a result, leading ESL adopters have been forced to devise their own custom methodologies. Does everyone need to develop their own custom ‘vertical’ methodology using standard ‘horizontal’ languages, libraries, and data formats, or is it possible to devise a common, standard methodology – open to all – that would help to mainstream ESL design and verification?

This panel of ESL users and suppliers will take a close look at what is being done today and debate the issues around what more is needed to address increasing system complexity. What are the major attributes and requirements for a standard methodology? How would it deliver the diverse requirements of algorithm development, system architecture exploration and optimization, integration and re-use of intellectual property (IP) from diverse sources, processor and coprocessor development, software development, RTL design, and testbench generation for system-to-implementation verification?

Panelists will discuss these and other issues to illuminate some of the steps toward a standard ESL design and verification methodology.
CAD Challenges for Leading-Edge Multimedia Designs

Chair: Andrew B. Kahng - University of California at San Diego, La Jolla, CA
Speakers: Patrick Blouet - STMicroelectronics, Crolles, France
          Ira Chayut - NVIDIA, Santa Clara, CA
          Dac Pham - IBM Corp., Austin, TX

Abstract
Multimedia designs are among the most complex leading-edge integrated circuits that are made today. In this session, CAD architects for three industry-leading multimedia products will discuss new challenges that arise across the CAD flow – from system and architecture level through physical implementation - as we approach billion-transistor devices. The first talk will focus on system-level specification and codesign of embedded software for a multimedia processor. The second talk will discuss new time and space challenges for verification methodologies, which must be met to address the requirements of graphics processor time-to-market pressures. The third talk will discuss CAD challenges unique to a pioneering high-speed, multi-core processing engine for gaming and entertainment platforms.
BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP

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ABSTRACT
In this paper, we propose a new global router, BoxRouter, powered by the concept of box expansion and progressive integer linear programming (ILP). BoxRouter first uses a simple PreRouting strategy which can predict and capture the most congested regions with high fidelity compared to the final routing. Based on progressive box expansion initiated from the most congested region, BoxRouting is performed with progressive ILP and adaptive maze routing. It is followed by an effective PostRouting step which reroutes without rip-up to obtain smooth tradeoff between wirelength and routability. Our experimental results show that BoxRouter significantly outperforms the state-of-the-art published global routers, e.g., 79% better routability than [1] (with similar wirelength and 2x speedup), 4.2% less wirelength and 16x speedup than [2] (with similar routability). Given the fundamental importance of routing, such dramatic improvement shall sparkle renewed interests in routing which plays a key role in nanometer design and manufacturing closure.

Keywords: VLSI, Global Routing, Congestion

REFERENCES
ABSTRACT
Conventionally, signal net routing is almost always implemented as Steiner trees. However, non-tree topology is often superior on timing performance as well as tolerance to open faults and variations. These advantages are particularly appealing for timing critical net routings in nano-scale VLSI designs where interconnect delay is a performance bottleneck and variation effects are increasingly remarkable. We propose Steiner network construction heuristics which can generate either tree or non-tree with different slackwirelength tradeoff, and handle both long path and short path constraints. Incremental non-tree delay update techniques are developed to facilitate fast Steiner network evaluations. Extensive experiments in different scenarios show that our heuristics usually improve timing slack by hundreds of pico seconds compared to traditional tree approaches.

Keywords: Steiner network, routing, interconnect, redundancy

REFERENCES
ABSTRACT
Steiner routing is a fundamental yet NP-hard problem in VLSI design and other research fields. In this paper, we propose to model the routing graph by an RC network with routing terminals as input ports and Hanan nodes as output ports. We show that the faster an output reaches its peak, the higher the possibility for the correspondent Hanan node to be a Steiner point. Iteratively adding one or multiple selected Steiner points to build and improve Steiner trees leads to 1-cktSteiner and Blocked-cktSteiner (in short, B-cktSteiner) algorithms, respectively. When there are no routing obstacles, 1-cktSteiner obtains similar wirelength compared with the best existing algorithm FastSteiner. Both are less than 1% worse than the exact solution, but 1-cktSteiner is up to 11.3X faster than FastSteiner. Compared with the fastest existing heuristic FLUTE, B-cktSteiner has similar runtime but up to 1.9% shorter wirelength. Different from FastSteiner and FLUTE which are only applicable to non-obstacle cases, 1-cktSteiner and B-cktSteiner can be applied to routing with obstacles with minimal runtime increase. Compared with the best existing obstacle-avoiding algorithm An-OARSMan, 1-cktSteiner has similar runtime and reduces wirelength by 6.12%, and B-cktSteiner has an average speedup of 352X with a similar wirelength.

Keywords: Routing, Simulation, RSMT, OARSMT

REFERENCES
Timing-Driven Steiner Trees are (Practically) Free

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ABSTRACT
Traditionally, rectilinear Steiner minimum trees (RSMT) are widely used for routing estimation in design optimizations like floorplanning and physical synthesis. Since it optimizes wirelength, an RSMT may take a “non-direct” route to a sink, which may give the designer an unnecessarily pessimistic view of the delay to the sink. Previous works have addressed this issue through performance-driven constructions, minimum Steiner arborescence, and critical sink based Steiner constructions. Physical synthesis and routing flows have been reticent to adapt universal timing-driven Steiner constructions out of fear that they are too expensive (in terms of routing resource and capacitance). This paper studies several different performance-driven Steiner tree constructions in order to show which ones have superior performance. A key result is that they add at most 2%-4% extra capacitance, and are thus a promising avenue for today’s increasingly aggressive performance-driven P&R flows. We demonstrate using a production P&R flow that timing-driven Steiner topologies can be easily embedded into an incremental routing subflow to obtain significantly improved timing (3.6% and 5.1% improvements in cycle time for two industry testcases) at practically no cost of wirelength or routability.

Keywords: Timing-Driven, Rectilinear Steiner Tree, Arborescence

REFERENCES
[1] Personal communication with Dr. Weiping Shi.


Systematic Software-Based Self-Test for Pipelined Processors

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³ NEC Laboratories America, Princeton, NJ, USA

ABSTRACT

Software-based self-test (SBST) has recently emerged as an effective methodology for the manufacturing test of processors and other components in Systems-on-Chip (SoCs). By moving test related functions from external resources to the SoC’s interior, in the form of test programs that the on-chip processor executes, SBST eliminates the need for high-cost testers, and enables high-quality at-speed testing. Thus far, SBST approaches have focused almost exclusively on the functional (directly programmer visible) components of the processor. In this paper, we analyze the challenges involved in testing an important component of modern processors, namely, the pipelining logic, and propose a systematic SBST methodology to address them. We first demonstrate that SBST programs that only target the functional components of the processor are insufficient to test the pipeline logic, resulting in a significant loss of fault coverage. We further identify the testability hotspots in the pipeline logic. Finally, we develop a systematic SBST methodology that enhances existing SBST programs to comprehensively test the pipeline logic. The proposed methodology is complementary to previous SBST techniques that target functional components (their results can form the input to our methodology), and can reuse the test development effort behind existing SBST programs. We applied the methodology to two complex, fully pipelined processors. Results show that our methodology provides fault coverage improvements of up to 15% (12% on average) for the entire processor, and fault coverage improvements of 22% for the pipeline logic, compared to a conventional SBST approach.

Keywords: Processor testing, Functional Testing, Software-Based Self-Test.

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A Test Pattern Ordering Algorithm for Diagnosis with Truncated Fail Data

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ABSTRACT
In this paper, we propose a test pattern ordering algorithm for fault diagnosis. Test pattern ordering is effective in situations where the fail log is truncated and contains a limited number of fail data. In such cases, higher diagnostic resolution can be achieved with the test set appropriately ordered. Test pattern ordering is independent of the diagnosis algorithm used. The higher resolution achieved by test pattern ordering is obtained at no additional cost once the test patterns have been appropriately ordered. Experimental results on two industrial designs are presented to demonstrate the effectiveness of the proposed method.

Keywords: Test pattern ordering, diagnosis, truncated fail data.

REFERENCES
DFT for Controlled-Impedance I/O Buffers

Ahmad A. Al-Yamani
King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia

ABSTRACT
This paper presents an architecture that enhances the testability of controlled-impedance buffers (CIBs). By testing CIBs digitally, the new architecture overcomes most of the problems with the traditional testing method. Most of these problems are test cost related. While reducing the test cost, the new architecture allows for higher test quality that even includes delay testing capabilities.

Keywords: Built-in self test, design-for-testability, I/O test, I/O characterization.

REFERENCES
Variation-Aware Analysis: Savior of the Nanometer Era?

Chair: William H. Joyner - SRC
Panelists: Sani R. Nassif - IBM, Austin, TX
          Dennis Sylvester - Univ of Michigan, Ann Arbor, MI
          Vijay Pitchumani - Intel Corp., Santa Clara, CA
          Clive Bittlestone - Texas Instruments, Dallas, TX
          Norma Rodriguez - AMD, Sunnyvale, CA
          Riko Radojcic - Qualcomm, San Diego, CA

ABSTRACT
VLSI engineers have traditionally used a variety of CAD analysis tools (e.g. SPICE) to deal with variability. As we go into deep sub micron issues, the analysis is becoming harder due to many secondary effects becoming primary. Panelists will debate the variability trend and present the order of importance of many variability trends (Vdd, Vt, Interconnect, Leff, Gate Width) and their impact on design tools and methodologies. What new design tools, new modeling methodologies, and new (or old) design styles will combine to address variability? Will conservative design to accommodate variability halt the progress of Moore’s Law? Is life as we know it over, or are we facing an opportunity for innovation in tools and design that will move us forward over the barriers that technology has placed in our path?

Keywords: Variability, Yield, DFY
A Fully Physical Model for Leakage Distribution under Process Variations in Nanoscale Double-Gate CMOS

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ABSTRACT
Double-gate CMOS is projected to replace classical bulk and SOI technologies around the 32nm node. Predicting the impact of process variations on yield for these novel devices is necessary at an early stage of the design cycle, to enable optimal technology and circuit design choices. This paper presents a fully physical model for double-gate leakage distribution due to gate length ($L$) and body thickness ($t_{si}$) variations, both for single devices and stacks. The model is derived directly from the solution of Poisson’s and Schrödinger’s equations, and thus captures the effect of unique double-gate phenomena such as volume inversion and quantum confinement. It is scalable to $L = 13$nm and $t_{si} = 3$nm, with less than 2% error for $3\sigma$ variation as large as 20% of nominal process parameters.

Keywords: Double-gate, Multiple-gate, FinFET, Tri-gate, Process Variations, Leakage Distribution

REFERENCES
A PLA based Asynchronous Micropipelining Approach for Subthreshold Circuit Design

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**Conexant Systems, Inc, Colorado

ABSTRACT

Power consumption is a dominant issue in contemporary circuit design. Sub-threshold circuit design is an appealing means to dramatically reduce this power consumption. However, sub-threshold designs suffer from the drawback of being significantly slower than traditional designs. To reduce the speed gap between sub-threshold and traditional designs, we propose a sub-threshold circuit design approach based on asynchronous micropipelining of a levelized network of PLAs. We describe the handshaking protocol, circuit design and logic synthesis issues in this context. Our preliminary results demonstrate that by using our approach, a design can be sped up by about 7x, with an area penalty of 47%. Further, our approach yields an energy improvement of about 4x, compared to a traditional network of PLA design. Our approach is quite general, and can be applied to traditional circuits as well.

Keywords: Sub-threshold, Micro-pipelining, PLA, Asynchronous

REFERENCES

Subthreshold Logical Effort: A Systematic Framework for Optimal Subthreshold Device Sizing

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ABSTRACT
Subthreshold circuit designs have been demonstrated to be a successful alternative when ultra-low power consumption is paramount. However, the characteristics of MOS transistors in the subthreshold regime are significantly different from those in strong-inversion. This presents new challenges in design optimization, particularly in complex gates with stacks of transistors. In this paper, we demonstrate a new optimal sizing scheme for subthreshold designs which takes these issues into account. We derive a closed-form solution for the correct sizing of transistors in a stack, both in relation to other transistors in the stack, and to a single transistor with equivalent current drivability. Experimental results show that our framework provides a performance improvement of up to 13.5% over the conventional logical effort method on ISCAS benchmark circuits, while one component circuit demonstrated an improvement of 33.1%.

Keywords: Subthreshold logic, logical effort, ultra-low power design

REFERENCES
ABSTRACT

Multi-Vdd is an effective method to reduce both leakage and dynamic power. A key challenge in a multi-Vdd design is to limit the design cost and the demand for level shifters. This can be tackled by grouping cells of different supply voltages into a small number of voltage islands. Recently, an elegant algorithm [7] is proposed for generating voltage islands that balance the power versus design cost tradeoff under performance requirement, according to the placement proximity of the critical cells. One prerequisite of [7] is an initial voltage assignment at the standard cell level that meets timing. In this paper, we present a novel method to produce quality voltage assignment to [7], which not only meets timing but also forms good proximity of the critical cells to provide [7] with a smooth input. The algorithm is based on effective delay budgeting and efficient computation of physical proximity by Voronoi diagram. Our experiments on real industrial designs show that our algorithm leads to 25 - 75% improvement in the voltage island generation, with the computation time only linear to the design size.

Keywords: Low power, Voltage assignment, Voronoi diagram

REFERENCES

An Efficient and Versatile Scheduling Algorithm Based On SDC Formulation

Jason Cong and Zhiru Zhang
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ABSTRACT
Scheduling plays a central role in the behavioral synthesis process, which automatically compiles high-level specifications into optimized hardware implementations. However, most of the existing behavior-level scheduling heuristics either have a limited efficiency in a specific class of applications or lack general support of various design constraints.

In this paper we describe a new scheduler that converts a rich set of scheduling constraints into a system of difference constraints (SDC) and performs a variety of powerful optimizations under a unified mathematical programming framework. In particular, we show that our SDC-based scheduling algorithm can efficiently support resource constraints, frequency constraints, latency constraints, and relative timing constraints, and effectively optimize longest path latency, expected overall latency, and the slack distribution. Experiments demonstrate that our proposed technique provides efficient solutions for a broader range of applications with higher quality of results (in terms of system performance) when compared to the state-of-the-art scheduling heuristics.

Keywords: Scheduling, Behavioral synthesis, SDC

REFERENCES


Register Binding for Clock Period Minimization

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Chung Li, Taiwan, R.O.C.

ABSTRACT
In modern high-speed circuit design, the clock skew has been widely utilized as a manageable resource to improve the circuit performance. However, in high-level synthesis stage, the circuit is never optimized for the utilization of clock skew. This paper is the first attempt to the high-level synthesis of non-zero clock skew circuits. First, we show that the register binding in high-level synthesis stage has a significant impact on the clocking constraints between registers. As a result, different register binding solutions lead to different smallest feasible clock periods. Then, based on that observation, we formulate the problem of register binding for clock period minimization. Given a constraint on the number of registers, our objective is to find a minimum-period register binding solution. Experimental data show that, in most benchmark circuits, the lower bound of the clock period can be achieved without any extra overhead on the number of registers.

Keywords: High-Level Synthesis, Clock Skew, Timing Optimization.

REFERENCES
Towards the Automatic Exploration of Arithmetic-Circuit Architectures

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School of Computer and Communication Sciences, Lausanne, Switzerland

ABSTRACT
The optimization of arithmetic circuits has always been essentially a manual task: arithmetic experts study the best architectures for arithmetic components and write libraries of generators, and designers instantiate library components and rely on logic synthesizers to obtain good implementations. In this paper we look at the capabilities of commercial synthesizers when it comes to arithmetic circuits, and observe that they are essentially unable to switch from one arithmetic architecture to another (e.g., from a ripple-carry to a carry-lookahead adder). Therefore, users relying on logic synthesis miss most optimization potentials. We therefore investigate algorithms for factorization which can prepare structured VHDL or Verilog for synthesizers to implement, and show first steps into pruning the search space from many irrelevant or equivalent solutions. Our results are still very limited in complexity but we show that our techniques successfully concentrate on the automatic exploration of very different solutions, and discover architectures known and unknown to expert designers, such as different types of adders, the carry-save representation, or improved multipliers. This is a first step toward a class of arithmetic optimizers which sit on top of classic logic synthesizers.

REFERENCES
ABSTRACT
Design space exploration during high level synthesis is often conducted through ad-hoc probing of the solution space using some scheduling algorithm. This is not only time consuming but also very dependent on designer’s experience. We propose a novel design exploration method that exploits the duality between the time and resource constrained scheduling problems. Our exploration automatically constructs a high quality time/area tradeoff curve in a fast, effective manner. It uses the MAX-MIN ant colony optimization to solve both the time and resource constrained scheduling problems. We switch between the time and resource constrained algorithms to quickly traverse the design space. Compared to using force directed scheduling exhaustively at every time step, our algorithm provides a significant solution quality savings (average 17.3% reduction of resource counts) with similar run time on a comprehensive benchmark suite constructed with classic and real-life samples. Our algorithms scale well over different applications and problem sizes.

Keywords: Design Space Exploration, Ant Colony Optimization, MAX-MIN Ant System, Instruction Scheduling Algorithms

REFERENCES
Rapid Estimation of Control Delay from High-Level Specifications

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**School of ECE, Purdue Univ., West Lafayette, IN
***Dept. of Comp. Sc. & Engg., Indian Institute of Technology, New Delhi

ABSTRACT
We address the problem of estimating controller delay from high-level specifications during behavioral synthesis. Typically, the critical path of a synthesized behavioral design goes through both the datapath and the control logic; yet most scheduling algorithms account only for datapath and ignore control delay, leading to timing uncertainties in the resulting designs. We present an estimation technique for computing a fast, robust, scalable, and reasonably accurate approximation of the control delay from behavioral specifications. The delay estimate is formulated in terms of the properties of the input specification and other inputs to the synthesis process such as resource constraints.

Keywords: High Level Synthesis, FSM, Control Delay, Estimation

REFERENCES
PANEL: Design Challenges for Next-Generation Multimedia, Game and Entertainment Platforms

Chair: Bryan Lewis - Gartner Dataquest, San Jose, CA
Panelists: John Cohn - IBM Corp., Burlington, VT
Richard Tobias - Pixelworks, Inc., Campbell, CA
Jeong-Taek Kong - Samsung Electronics Co., Ltd., Giheung, KOREA
Chris Malachowsky - NVIDIA Corp., Santa Clara, CA
Brendan Traw - Intel Corp., Hillsboro, OR

ABSTRACT
Modern multimedia, gaming and entertainment devices epitomize high-growth, consumer-driven applications for silicon. 2006 has been a year that launched several high-profile gaming systems, and major changes in home networking. This year has also witnessed the emergence of the digital home and the ePC, as well as continued struggles for control of the home gateway. Mobile digital convergence has continued with the fusion of media, telephony, and digital-mobile TV. The industry’s ability to rapidly evolve such consumer-centric systems brings to bear all of the technology competencies required for cutting-edge IC designs, as well as for tools and methodologies that support those designs.

Multimedia and gaming chips are pushing the leading edge of EDA technology forward on fronts that include architectural synthesis, high-speed clocking, power management, verification, and IP reuse. As just one example, GPU operations per second are growing significantly faster than desktop CPU operations per second, while at the same time, GPU design teams often place less emphasis than microprocessor teams on circuits and layout, and more emphasis on architecture and design enablement. The confluence of these trends leads to design and CAD solutions that are unique in the market space.

In this panel session, the panelists have been selected to represent five key “constituencies”: the digital home (Intel), mobile digital TV (Samsung), graphics engines (NVIDIA), advanced displays (Pixelworks), and gaming/multimedia processing (IBM). The panel will address such questions as:

- What are the underlying chip architectures and roadmaps for key multimedia/entertainment platforms?
- What are the key design and technology challenges (or “brick walls”) for next-generation products, and how will these challenges be addressed?
- Where will we see the next “convergence” in devices and platforms?
- What other challenges arise from complex supplier and competitor relationships, standards, and other aspects of a globalized market?

Other design challenges to be discussed include design enablement (compilers, programming models, etc.), design for IP reuse (configurability, derivatives), and IP management in a world of increasing “co-opetition”.

Keywords: Multimedia, gaming, entertainment, design methodology.
ABSTRACT
Since performance on FPGAs is dominated by the routing architecture rather than wirelength, we propose a new architecture-aware approach to initial FPGA placement that models the relationship between performance and the routing grid, using concepts from graph embedding and metric geometry. Our approach, CAPRI, can be viewed as an embedding of a graph representing the netlist into a metric space that is representative of the FPGA. First, we develop an analytic metric of distance that models delays along the FPGA routing grid. We then embed a netlist into the defined metric space using matrix projections and online bipartite matching. Experimental comparisons with the popular FPGA tool, VPR, show that with CAPRI’s initial solution, the resulting placements show median improvements of 10% in critical path delays for the larger MCNC benchmarks. Total placement runtime is also improved by 2x on average.

Keywords: FPGAs, Placement, Metric Embedding

REFERENCES
Efficient SAT-based Boolean Matching for FPGA Technology Mapping

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ABSTRACT

Most FPGA technology mapping approaches either target Lookup Tables (LUTs) or relatively simple Programmable Logic Blocks (PLBs). Considering networks of PLBs during technology mapping has the potential of providing unique optimizations unavailable through other techniques. This paper proposes a Boolean matching approach for FPGA technology mapping targeting networks of PLBs. To overcome the demanding memory requirements of previous approaches, the Boolean matching problem is formulated as a Boolean Satisfiability (SAT) problem. Since the SAT formulation provides a trade-off between space and time, the primary objective is to increase the efficiency of the SAT-based approach. To do this, the original SAT problem is decomposed into two easier SAT problems. To reduce the problem search space, a theorem is introduced to allow conflict clauses to be shared across problems and extra constraints are generated. Experiments demonstrate a 340% run time improvement and 27% more success in mapping than previous SAT-based approaches.

Keywords: FPGA technology mapping, Boolean matching, Boolean satisfiability

REFERENCES

Optimal Simultaneous Mapping and Clustering for FPGA Delay Optimization

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ABSTRACT
Both technology mapping and circuit clustering have a large impact on FPGA designs in terms of circuit performance, area, and power dissipation. Existing FPGA design flows carry out these two synthesis steps sequentially. Such a two-step approach cannot guarantee that the final delay of the circuit is optimal, because the quality of clustering depends significantly on the initial mapping result. To address this problem, we develop an algorithm that performs mapping and clustering simultaneously and optimally under a widely used clustering delay model. To our knowledge, our algorithm, named SMAC (simultaneous mapping and clustering) is the first delay-optimal algorithm to generate a synthesis solution that considers a combination of both steps. Compared to a synthesis flow using state-of-the-art mapping and clustering algorithms DAOmap [7] + T-VPACK [17] -- SMAC achieves a 25% performance gain with a 22% area overhead under the clustering delay model. After placement and routing, SMAC is 12% better in performance.

Keywords: FPGA, technology mapping, clustering, dynamic programming

REFERENCES
Simultaneous Time Slack Budgeting and Retiming for Dual-Vdd FPGA Power Reduction

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ABSTRACT
Field programmable dual-Vdd interconnects are effective to reduce FPGA power. Assuming uniform length interconnects, existing work has developed time slack budgeting to minimize power based on estimating the lower bound of power reduction using dual-Vdd for given time slack. In this paper, we show that such lower bound estimation cannot be extended to mixed length interconnects that are used in modern FPGAs. We develop a technique to estimate power reduction using dual-Vdd for mixed length interconnects, and apply linear programming (LP) to solve slack budgeting to minimize power for mixed length interconnects. Experiments show 53% power reduction on average compared to single-Vdd interconnects. Furthermore, this paper presents a simultaneous retiming and slack budgeting algorithm to reduce power in dual-Vdd FPGAs considering placement and flip-flop binding constraints. The algorithm is based on mixed integer and linear programming (MILP) and achieves up to 20% power reduction compared to retiming followed by slack budgeting. We propose a runtime efficient flow to apply simultaneous retiming and slack budgeting only when it is necessary. To the best of our knowledge, this paper is the first in-depth study of simultaneous retiming and slack budgeting for dual-Vdd programmable FPGA power reduction while considering layout constraints.

Keywords: Low power, retiming, FPGA

REFERENCES
VIRTUS: A New Processor Virtualization Architecture for Security-Oriented Next-Generation Mobile Terminals

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ABSTRACT
We propose a new processor virtualization architecture, VIRTUS, to provide a dedicated domain for pre-installed applications and virtualized domains for downloaded native applications. With it, security-oriented next-generation mobile terminals can provide any number of domains for native applications. VIRTUS features three new technologies: VMM asymmetrization, dynamic interdomain communication and virtualization-assist logic, and it is first in the world to virtualize an ARM-based multiprocessor.

Keywords: Multiprocessor, Processor Virtualization

REFERENCES
A Network Security Processor Design Based on an Integrated SOC Design and Test Platform

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ABSTRACT
In this paper we present a generic Network Security Processor (NSP) design suitable for a wide range of security related protocols in wired or wireless network applications. Following the platform-based design methodology, we develop four specific platforms, i.e., architecture platform, EDA platform, Design-for-Testability (DFT) platform, and prototyping platform, for our NSP design. With these platforms, design of the NSP chip becomes more efficient and systematic. A prototype chip of the NSP has been implemented and fabricated with a 0.18μm CMOS technology. The chip area is 5mm×5mm (with 1M gates approximately), including I/O pads. The operating clock rate is 80MHz. The best performance of the crypto-engines is 1.025Gbps for AES, 1.652Mbps for RSA, 125.9/157.65Mbps for HMACSHA1/MD5, and 2.56Gbps for random number generator. Comparison result shows that our NSP is efficient in terms of performance, flexibility and scalability.

Keywords: AES, RSA, HMAC-MD5, HMAC-SHA1, RNG, AMBA

REFERENCES
Software Architecture Exploration for High-Performance Security Processing on a Multiprocessor Mobile SoC

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ABSTRACT
We present a systematic methodology for exploring the security processing software architecture for a commercial heterogeneous multiprocessor system-on-chip (SoC) for mobile devices. The SoC contains multiple host processors executing applications and a dedicated programmable security processing engine. We developed an exploration methodology to map the code and data of security software libraries onto the platform, with the objective of maximizing the overall application-visible performance. The salient features of the methodology include (i) the use of real performance measurements from a prototyping board that contains the target platform to drive the exploration, (ii) a new data structure access profiling framework that allows us to accurately model the communication overheads involved in offloading a given set of functions to the security processor, and (iii) an exact branch-and-bound based design space exploration algorithm that determines the best mapping of security library functions and data structures to the host and security processors. We used the proposed framework to map a commercial security library to the target mobile application SoC. The resulting optimized software architecture outperformed several manually-designed software architectures, resulting in upto 12.5X speedup for individual cryptographic operations (encryption, hashing) and 2.2X-6.2X speedup for applications such as a Digital Rights Management (DRM) agent and Secure Sockets Layer (SSL) client. We also demonstrate the applicability of our framework to software architecture exploration in other multiprocessor scenarios.

Keywords: Software partitioning, computation offloading

REFERENCES
IMPRES: Integrated Monitoring for Processor Reliability and Security

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ABSTRACT
Security and reliability in processor based systems are concerns requiring adroit solutions. Security is often compromised by code injection attacks, jeopardizing even 'trusted software'. Reliability is of concern where unintended code is executed in modern processors with ever smaller feature sizes and low voltage swings causing bit flips. Countermeasures by software-only approaches increase code size by large amounts and therefore significantly reduce performance. Hardware assisted approaches add extensive amounts of hardware monitors and thus incur unacceptably high hardware cost. This paper presents a novel hardware/software technique at the granularity of micro-instructions to reduce overheads considerably. Experiments show that our technique incurs an additional hardware overhead of 0.91% and clock period increase of 0.06%. Average clock cycle and code size overheads are just 11.9% and 10.6% for five industry standard application benchmarks. These overheads are far smaller than have been previously encountered.

Keywords: Detecting Code Injection Attacks, Basic Block Checksumming, Checksum Encryption, Bit Flips Detection

REFERENCES


A Parallelized Way to Provide Data Encryption and Integrity Checking on a Processor-Memory Bus

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ABSTRACT
This paper describes a novel engine, called PE-ICE (Parallelized Encryption and Integrity Checking Engine), enabling to guarantee confidentiality and integrity of data exchanged between a SoC (System on Chip) and its external memory. The PE-ICE approach is based on an existing block-encryption algorithm to which the integrity checking capability is added. Simulation results show that the performance overhead of PE-ICE remains low (below 4%) compared to block-encryption-only systems (which provide data confidentiality only).

Keywords: Data Confidentiality and Integrity, Architectures, Bus Encryption.

REFERENCES
Symmetry Detection for Large Boolean Functions using Circuit Representation, Simulation, and Satisfiability

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ABSTRACT
Classical two-variable symmetries play an important role in many EDA applications, ranging from logic synthesis to formal verification. This paper proposes a complete circuit-based method that makes uses of structural analysis, integrated simulation and Boolean satisfiability for fast and scalable detection of classical symmetries of completely-specified Boolean functions. This is in contrast to previous incomplete circuit-based methods and complete BDD-based methods. Experimental results demonstrate that the proposed method works for large Boolean functions, for which BDDs cannot be constructed.

Keywords: Boolean functions, classical symmetries, And-Inverter Graphs, simulation, Boolean satisfiability.

REFERENCES


Exploiting K-Distance Signature for Boolean Matching and $G$-Symmetry Detection

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ABSTRACT
In this paper, we present the concept of k-distance signature which is a general case of many existing signatures. By exploiting k-distance signature, we propose an Algorithm for Input Differentiation (AID) which is very powerful to distinguish inputs of Boolean functions. Moreover, based on AID, we propose a heuristic method to detect $G$-symmetry of Boolean functions and a Boolean matching algorithm. The experimental results show that our methods are not only effective but also very efficient for Boolean matching and $G$-symmetry detection.

REFERENCES
ABSTRACT

The gain-based technology mapping paradigm has been successfully employed for finding minimum delay and minimum area mappings. However, existing gain-based technology mappers fail to find circuits with minimal leakage power. In this paper, we introduce algorithms and modeling strategies that enable efficient gain-based technology mapping for minimum leakage power. The proposed algorithm is probability-aware and can rigorously take into account input state probability distribution to generate a circuit mapping with minimum leakage at a given percentile. Minimizing leakage at high percentiles is essential for minimizing peak leakage, which strongly influences the cooling limits and packaging costs.

The algorithms have been tested on the ISCAS85 benchmark suite. Results indicate that the mappings produced by the new algorithm consume, on average 14% lesser leakage power at the 99% percentile with 1% delay penalty when compared with the approaches used in previous gain-based mappers [2]. Also, compared to a dominant-state mapper, our approach produces mappings with 15% lesser mean value of leakage. The new algorithm also reduces leakage at high quantiles by 12.8% on average, compared to a dominant state leakage minimizing mapper and the maximum savings can be as high as 21.49% across the benchmarks. Compared to the bin based mapper [10], the runtime of the algorithm is 15X faster.

Keywords: Leakage, Technology Mapping, Logical Effort.

References
Gate Sizing: FinFETs vs 32nm Bulk MOSFETs

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ABSTRACT
FinFET devices promise to replace traditional MOSFETs because of superior ability in controlling leakage and minimizing short channel effects while delivering a strong drive current. We investigate in this paper gate sizing of finFET devices, and we provide a comparison with 32nm bulk CMOS. Wider finFET devices are built utilizing multiple parallel fins between the source and drain. Independent gating of the finFET’s double gates allows significant reduction in leakage current. We perform temperature-aware circuit optimization by modeling delay using temperature-dependent parameters, and by imposing constraints that limit the maximum allowable number of parallel fins. We show that finFET circuits are superior in performance and produce less static power when compared to 32nm circuits.

Keywords: FinFET, thermal modeling, gate sizing

REFERENCES
This paper presents a technique for preprocessing combinational logic before technology mapping. The technique is based on the representation of combinational logic using And-Inverter Graphs (AIGs), a network of two-input ANDs and inverters. The optimization works by alternating DAG-aware AIG rewriting, which reduces area by sharing common logic without increasing delay, and algebraic AIG balancing, which minimizes delay without increasing area. The new technology-independent flow is implemented in a public-domain tool ABC. Experiments on large industrial benchmarks show that the proposed methodology scales to very large designs and is several orders of magnitude faster than SIS and MVSIS while offering comparable or better quality when measured by the quality of the network after mapping.

**Keywords:** Technology-independent logic synthesis, And-Inverter Graphs, NPN equivalence, technology mapping.

**REFERENCES**


Energy-Scalable OFDM Transmitter Design and Control

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ABSTRACT
Orthogonal Frequency Division Multiplexing (OFDM) is the modulation of choice for broadband wireless communications. Unfortunately, it comes at the cost of a very low energy efficiency of the analog transmitter. Numerous circuit-level and signal processing techniques have been proposed to improve that energy efficiency. However more disruptive improvement can be achieved at system-level, capitalizing on energy-scalable design and circuit reconfiguration to match the user requirements and operation environment. We describe the design of such an energy-scalable reconfigurable transmitter as well as its control strategy. Based on measurement carried out on the physical realization of this transmitter, the benefit of system-level energy management is shown. Energy-efficiency scalability ranges over 30%, which translates in an average system-level energy improvement of up to 40% compared to a non-scalable system.

Keywords: OFDM, Energy Management, Energy-aware design, Energy-scalability.

REFERENCES


Systematic Temperature Sensor Allocation and Placement for Microprocessors

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ABSTRACT
Modern high performance processors employ advanced techniques for thermal management, which rely on accurate readings of on-die thermal sensors. As the importance of thermal effects on reliability and performance of integrated circuits increases careful planning and embedding of thermal monitoring mechanisms into these systems will be crucial. Systematic tools for analysis of thermal behavior and determination of best allocation and placement of thermal sensing elements is therefore a highly relevant problem. In this paper, we propose novel optimization techniques for determining the optimal locations and allocations for thermal sensors to provide a high fidelity thermal profile of a complex microprocessor system. Our algorithm identifies an optimal physical location for each sensor such that the sensor’s the attraction towards steep thermal gradient is maximized. We also present a hybrid allocation and placement strategy showing the trade-offs associated with number of sensors used and expected accuracy. Our results show that our tool is able to create a sensor distribution for a given microprocessor architecture providing thermal measurements with maximum error of 3.18° C and average maximum error of 1.63° C across a wide set of applications.

Keywords: Temperature, Sensor, Allocation, Placement.

REFERENCES
HybDTM: A Coordinated Hardware-Software Approach for Dynamic Thermal Management

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ABSTRACT
With ever-increasing power density and cooling costs in modern high-performance systems, dynamic thermal management (DTM) has emerged as an effective technique for guaranteeing thermal safety at run-time. While past works on DTM have focused on different techniques in isolation, they fail to consider a synergistic mechanism using both hardware and software support and hence lead to a significant execution time overhead.

In this paper, we propose HybDTM, a methodology for fine-grained, coordinated thermal management using a hybrid of hardware techniques, such as clock gating, and software techniques, such as thermal-aware process scheduling, synergistically leveraging the advantages of both approaches. We show that while hardware techniques can be used reactively to manage thermal emergencies, proactive use of low-overhead software techniques can rely on application-specific thermal profiles to lower system temperature. Our technique involves a novel regression-based thermal model which provides fast and accurate temperature estimates for run-time thermal characterization of applications running on the system, using hardware performance counters, while considering system-level thermal issues. We evaluate HybDTM on an actual desktop system running a number of SPEC2000 benchmarks, in both uniprocessor and simultaneous multi-threading (SMT) environments, and show that it is able to successfully manage the overall temperature with an average execution time overhead of only 9.9% (16.3% maximum) compared to the case without any DTM, as opposed to 20.4% (29.5% maximum) overhead for purely hardware-based DTM.

Keywords: dynamic thermal management, thermal model, hybrid hardware-software management

REFERENCES
A Systematic Method For Functional Unit Power Estimation in Microprocessors

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ABSTRACT
We present a new method for mathematically estimating the active unit power of functional units in modern microprocessors such as the Pentium 4 family. Our method leverages the phasic behavior in power consumption of programs, and captures as many power phases as possible to form a linear system of equations such that the functional unit power can be solved. Our experiment results on a real Pentium 4 processor show that power estimations attained as such agree with the measured power very well, with deviations less than 5% only.

Keywords: Power Estimation, Performance Counter, Microprocessor

REFERENCES
Low-Power Architectural Trade-Offs in a VLSI Implementation of an Adaptive Hearing Aid Algorithm

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ABSTRACT
This paper analyzes the power-area trade-off of functionally equivalent architectural implementations of a speech enhancement algorithm for hearing aids. Gate-level simulations and measurements show that an optimum degree of resource sharing (0.60mW in a 0.25 μm CMOS process) is more energy-efficient than both the fully time-multiplexed (1.42mW) and the isomorphic architecture (1.54 mW), without overly large area overhead (0.77mm2 against 0.43mm2 and 4.31mm2, respectively).

Keywords: Hearing aids, low-power architecture, speech enhancement

REFERENCES
Extending the Lifetime of Fuel Cell Based Hybrid Systems


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ABSTRACT

Fuel cells are clean power sources that have much higher energy densities and lifetimes compared to batteries. However, fuel cells have limited load following capabilities and cannot be efficiently utilized if used in isolation. In this work, we consider a hybrid system where a fuel cell based hybrid power source is used to provide power to a DVFS processor. The hybrid power source consists of a room temperature fuel cell operating as the primary power source and a Li-ion battery (that has good load following capability) operating as the secondary source. Our goal is to develop policies to extend the lifetime of the fuel cell based hybrid system. First, we develop a charge based optimization framework which minimizes the charge loss of the hybrid system (and not the energy consumption of the DVFS processor). Next, we propose a new algorithm to minimize the charge loss by judiciously scaling the load current. We compare the performance of this algorithm with one that has been optimized for energy, and demonstrate its superiority. Finally, we evaluate the performance of the hybrid system under different system configurations and show how to determine the best combination of fuel cell size and battery capacity for a given embedded application.

Keywords: Fuel cell, Battery, Hybrid systems, DVFS system, Task scaling

REFERENCES

High-Level Power Management of Embedded Systems with Application-Specific Energy Cost Functions

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ABSTRACT

Most existing dynamic voltage scaling (DVS) schemes for multiple tasks assume an energy cost function (energy consumption versus execution time) that is independent of the task characteristics. In practice the actual energy cost functions vary significantly from task to task. Different tasks running on the same hardware platform can exhibit different memory and peripheral access patterns, cache miss rates, etc. These effects result in a distinct energy cost function for each task.

We present a new formulation and solution to the problem of minimizing the total (dynamic and static) system energy while executing a set of tasks under DVS. First, we demonstrate and quantify the dependence of the energy cost function on task characteristics by direct measurements on a real hardware platform (the TI OMAP processor) using real application programs. Next, we present simple analytical solutions to the problem of determining energy-optimal voltage scale factors for each task, while allowing each task to be preempted and to have its own energy cost function. Based on these solutions, we present simple and efficient algorithms for implementing DVS with multiple tasks. We consider two cases: (1) all tasks have a single deadline, and (2) each task has its own deadline. Experiments on a real hardware platform using real applications demonstrate a 10% additional saving in total system energy compared to previous leakage-aware DVS schemes.

REFERENCES

Communication Latency Aware Low Power NoC Synthesis

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ABSTRACT
Communication latency and power consumption are two competing objectives in Network-on-Chip (NoC) design. This paper proposes a novel method that unifies these two objectives in a multi-commodity ow (MCF) formulation. With an improved fully polynomial approximation algorithm, power efficient design of an 8 x 8 NoC can be found for given average latency constraints with certain communication bandwidth requirements. Experimental results suggest that (1) compared with mesh, torus and hypercube topologies, the optimized design can improve power latency product by up to 52.1%, 29.4% and 35.6%, respectively. (2) by sacrificing 2% latency, power consumption of the optimized design can be improved by up to 19.4%, which indicates the importance of power and latency co-optimization in NoC design.

Keywords: Network-on-Chip, Latency, Power, Topology

REFERENCES
Optimality Study of Resource Binding with Multi-Vdd

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ABSTRACT
Deploying multiple supply voltages (multi-Vdd) on one chip is an important technique to reduce dynamic power consumption. In this work we present an optimality study for resource binding targeting designs with multi-Vdd. This is similar to the voltage-island design concept, except that the granularity of our voltage island is on the functional-unit level as opposed to the core level. We are interested in achieving the maximum number of low-Vdd operations and, at the same time, minimizing switching activity during functional unit binding. To the best of our knowledge, there is no known optimal solution to this problem. To compute an optimal solution for this problem and examine the quality gap between our solution and previous heuristic solutions, we formulate this problem as a min-cost network flow problem, but with special equal-flow constraints. This formulation leads to an easy reduction to the integer linear programming (ILP) solution and also enables efficient approximate solution by Lagrangian relaxation. Experimental results show that the optimal solution computed based on our formulation provides 7% more low-Vdd operations and also reduces the total switching activity by 20% compared to one of the best known heuristic algorithms that consider multi-Vdd assignments only.

Keywords: Behavioral synthesis, resource binding, low power design

REFERENCES
SMERT: Energy-Efficient Design of a Multimedia Messaging System for Mobile Devices

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ABSTRACT
Customized multimedia content delivery has become one of the most desirable applications to mobile device users. However its intense usage of wireless and user interfaces poses a great challenge to device usability and battery lifetime. In this paper, we describe our design and implementation of an energy-efficient multimedia messaging system to address this challenge. We construct a hierarchical system for users to access multimedia content, leveraging widely available short message service (SMS), an embedded system-based new interfacing device, and the Internet capability of mobile devices. Being the first of its type, the new system not only reduces energy overhead but also improves the usability of the service.

Keywords: Energy-efficient design, mobile services, multimedia messaging

REFERENCES
Signature-Based Workload Estimation for Mobile 3D Graphics

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ABSTRACT

Until recently, most 3D graphics applications had been regarded as too computationally intensive for devices other than desktop computers and gaming consoles. This notion is rapidly changing due to improving screen resolutions and computing capabilities of mass-market handheld devices such as cellular phones and PDAs. As the mobile 3D gaming industry is poised to expand, significant innovations are required to provide users with high-quality 3D experience under limited processing, memory and energy budgets that are characteristic of the mobile domain.

Energy saving schemes such as Dynamic Voltage and Frequency Scaling (DVFS), as well as system-level power and performance optimization methods for mobile devices require accurate and fast workload prediction. In this paper, we address the problem of workload prediction for mobile 3D graphics. We propose and describe a signature-based estimation technique for predicting 3D graphics workloads. By analyzing a gaming benchmark, we show that monitoring specific parameters of the 3D pipeline provides better prediction accuracy over conventional approaches. We describe how signatures capture such parameters concisely to make accurate workload predictions. Signature-based prediction is computationally efficient because first, signatures are compact, and second, they do not require elaborate model evaluations. Thus, they are amenable to efficient, real-time prediction. A fundamental difference between signatures and standard history-based predictors is that signatures capture previous outcomes as well as the cause that led to the outcome, and use both to predict future outcomes. We illustrate the utility of signature-based workload estimation technique by using it as a basis for DVFS in 3D graphics pipelines.

Keywords: 3D Graphics, embedded systems, workload estimation, dynamic voltage scaling.

REFERENCES

ABSTRACT
Graphics-intensive computer games are no longer restricted to high-performance desktops, but are also available on a variety of portable devices ranging from notebooks to PDAs and mobile phones. Battery life has been a major concern in the design of both the hardware and the software for such devices. Towards this, dynamic voltage and frequency scaling (DVFS) has emerged as a powerful technique. However, the showcase application for DVFS algorithms so far has largely been video decoding, primarily because it is computationally expensive and its workload exhibits a high degree of variability. This paper investigates the possibility of applying DVFS to interactive computer games, which to the best of our knowledge has not been studied before. We show that the variability in the workload associated with a popular First Person Shooter game like Quake II is significantly higher than video decoding. Although this variability makes game applications an attractive candidate for DVFS, it is unclear if DVFS algorithms can be applied to games due to their interactive (and hence highly unpredictable) nature. In this paper, we show using detailed experiments that (surprisingly) interactive computer games are highly amenable to DVFS. Towards this we present a novel workload characterization of computer games, based on the game engine for Quake II. We believe that our findings might potentially lead to a number of innovative DVFS algorithms targeted towards game applications, exactly as video decoding has motivated a variety of schemes for DVFS.

Keywords: Dynamic Voltage and Frequency Scaling, Computer Games, Computer Graphics, Animation, Multimedia, Graphics Workload Characterization, Power-aware Design

REFERENCES
Backlight Dimming in Power-Aware Mobile Displays

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ABSTRACT
This paper presents a temporally-aware backlight scaling (TABS) technique for video streams. The goal is to maximize energy saving in the display system by means of dynamic backlight dimming subject to a user-specified tolerance on the video distortion. The video distortion itself comprises of (i) an intraframe (spatial) distortion component due to frame-sensitive backlight scaling and transmittance function tuning and (ii) an inter-frame (temporal) distortion component due to large-step backlight dimming across multiple frames and modulated by the physiological characteristics of the human visual system. The proposed backlight scaling technique is capable of efficiently computing the flickering effect online and subsequently using a measure of the temporal distortion to appropriately adjust the slack on the intra-frame spatial distortion. The proposed technique has been implemented on the Apollo Testbed II hardware platform. Actual current measurements on this platform demonstrate the superiority of TABS compared to previous backlight dimming techniques.

Keywords: LCDs, Backlight scaling, Human Visual System

REFERENCES
Minimization for LED-backlit TFT-LCDs

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ABSTRACT
This paper presents an algorithm for minimizing power consumption of LED backlights in transmissive TFT-LCD monitors. The proposed algorithm reduces power consumption by scaling the luminous intensity of the red, green, and blue LED backlights independently according to the image histograms of each color channel. The algorithm consists of two phases. The first phase, chromaticity scaling, finds the optimal ratios of red, green, and blue backlights subject to a perceived color difference constraint. The second phase, luminance scaling, finds the optimal dimming factor subject to a perceived lightness difference constraint. The perceived color and lightness differences are measured by the CIELAB Color Difference Equation $2\Delta E^*_{ab}$, a standard metric for measuring color variation. Psychophysical experiments were performed with 35 observers to uncover the optimal luminance scaling function. An experimental LED backlight module was implemented and installed on a 19” side-lit TFT-LCD monitor to replace the original CCFL backlight. Within limited perceivable difference $2\Delta E^*_{ab}$, up to 76% of power consumption can be reduced for the benchmark images.

Keywords: TFT-LCD power minimization, LED backlight, chromaticity-luminance scaling, CIELAB color difference.

REFERENCES
Leakage Power Reduction of Embedded Memories on FPGAs Through Location Assignment

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ABSTRACT
Transistor leakage is poised to become the dominant source of power dissipation in digital systems, and reconfigurable devices are not immune to this problem. Modern FPGAs already have a significant amount of memory on the die, and with each generation the proportion of embedded memory to logic cells is growing. While assigning high $V_{th}$ can limit the leakage power, embedded memory timing is critical to performance and will draw an increasingly significant amount of leakage current. However, unlike in many processor based systems, on-chip memory accesses are often fully deterministic and completely under the control of the scheduler. In this paper we explore a variety of techniques to battle the problem of leakage in FPGA embedded memories that range in complexity and effectiveness. Through the addition of sleep and drowsy modes, controlled by the scheduler, the amount of leakage power can be reduced by several orders of magnitude. We show how even very simple schemes offer large amounts of benefit, and that further reductions are possible through careful leakage-aware data placement.

Keywords: Embedded memory, leakage power, location assignment

REFERENCES
A Fast HW/SW FPGA-Based Thermal Emulation Framework for Multi-Processor System-on-Chip

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ABSTRACT
With the growing complexity in consumer embedded products and the improvements in process technology, Multi-Processor System-On-Chip (MPSoC) architectures have become widespread. These new systems are complex to design as they must execute multiple complex applications (e.g. video processing, 3D games), while meeting additional design constraints (e.g. energy consumption or time-to-market). Moreover, the rise of temperature in the die for MPSoC components can seriously affect their final performance and reliability. Therefore, mechanisms to efficiently evaluate complete HW/SW MPSoC designs in terms of energy consumption, temperature, performance and other key metrics are needed. In this paper, we present a new HW/SW FPGA-based emulation framework that allows designers to rapidly extract a number of critical statistics from processing cores, memories and interconnection systems being emulated on a FPGA. This information is then used to interact in real-time with a SW thermal model running on a host computer via an Ethernet port. The results show speed-ups of three orders of magnitude compared to cycle-accurate MPSoC simulators, which enable a very fast exploration of a large range of MPSoC design alternatives at the cycle-accurate level. Finally, our HW/SW framework allows designers to test run-time thermal management strategies with real-life inputs without any loss in the performance of the emulated system.

Keywords: FPGA, Emulation, MPSoC, Thermal Studies.

REFERENCES
An Adaptive FPGA Architecture with Process Variation Compensation and Reduced Leakage

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ABSTRACT
Process induced threshold voltage variations bring about fluctuations in circuit delay, that affect the FPGA timing yield. We propose an adaptive FPGA architecture that compensates for these fluctuations. The architecture includes an additional characterizer circuit that classifies logic and routing blocks on each die according to their performance. Based on this classification, the architecture adaptively body-biases these resources by either speeding up the slow blocks or by slowing down the leaky ones. This procedure mitigates the effect of the variations and provides a better yield. We further diminish leakage by slowing down areas of the FPGA that have a positive slack. Overall, this architecture minimizes the timing variance of within-die and die-to-die $V_{th}$ variations by up to 3.45X and reduces leakage power in the non-critical areas of the FPGA by 3X with no effect on frequency.

Keywords: FPGA, Process Variations, Leakage, Body-biasing

REFERENCES
FLAW: FPGA Lifetime Awareness

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ABSTRACT
Aggressive scaling of technology has an adverse impact on the reliability of VLSI circuits. Apart from increasing transient error susceptibility, the circuits also become more vulnerable to permanent damage and failures due to different physical phenomenon. Such concerns have been recently demonstrated for regular microarchitectures. In this work we demonstrate the vulnerability of Field Programmable Gate Arrays (FPGA)s to two different types of hard errors, namely, Time Dependent Dielectric Breakdown (TDBB) and Electro-migration. We also analyze the performance degradation of FPGAs over time caused by Hot Carrier Effects (HCE). We also propose three novel techniques to counter such aging based failures and increase the lifetime of the device.

Keywords: FPGA, Time Dependent Dielectric Breakdown, Electro-migration, Hot Carrier Effects

REFERENCES
Solution-Processed Infrared Photovoltaic Devices

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ABSTRACT
Physically flexible, solution-processed solar cells have the potential to harvest light conveniently, cheaply and efficiently. Absorption of the considerable power in the infrared region of the solar spectrum is necessary for efficient solution-processed solar cells. We use lead sulphide (PbS) colloidal nanoparticles (quantum dots) that are quantum size effect tunable, allowing tailoring of absorption onset between 900 and 2000 nm. A number of device architectures will be described within, leading to photovoltaic devices which exhibit external quantum efficiencies exceeding 1%.

Keywords: Quantum dots, Photovoltaics, Solution processing, Infrared, Nanocrystals

REFERENCES
Circuits for Energy Harvesting Sensor Signal Processing

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ABSTRACT
The recent explosion in capability of embedded and portable electronics has not been matched by battery technology. The slow growth of battery energy density has limited device lifetime and added weight and volume. Passive energy harvesting from solar radiation, thermal sources, or mechanical vibration has potentially wide application in wearable and embedded sensors to complement batteries. The amount of energy from harvesting is typically small and highly variable, requiring circuits and architectures which are low power and can scale their power consumption with user requirements and available energy. We describe several circuit techniques for achieving these goals in signal processing applications for wireless sensor network nodes such as using Distributed Arithmetic to implement energy scalable signal processing algorithms. In addition, we propose increasing vibration energy harvesting efficiency by eliminating AC/DC conversion electronics, and have investigated self-timed circuits, power-on-reset circuitry, and memory for energy harvesting AC power supplies. These techniques can also be applied to energy harvesting from other sources. A chip will be fabricated to test the proposed circuits.

Keywords: energy harvesting, self-timed circuits, AC power supplies, dynamic memory, power-on-reset

REFERENCES
ABSTRACT
This article outlines several projects aimed at generating electrical energy by passively tapping a variety of human body sources and activities. After summarizing different energy harvesting modalities and techniques, I spotlight work done in my research group at the MIT Media Laboratory, including a system that scavenges electricity from the forces exerted on a shoe during walking. This system uses a flexible piezoelectric foil stay to harness sole-bending energy and a reinforced PZT dimorph to capture heel-strike energy. The piezoelectric generators drive a battery-less, active RF tag, which transmits a short-range wireless ID while walking, thereby enabling location based services and active environments. Other systems that we have developed are also discussed, including a battery-less pushbutton that can send an RF ID code with a single push, sensor nodes that harvest mobility rather than energy, and power management schemes that exploit sensor diversity to achieve energy efficiency.

Keywords: Energy Harvesting, Power Scavenging, Parasitic Power.

REFERENCES


Harvesting Aware Power Management for Sensor Networks

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ABSTRACT
Energy harvesting offers a promising alternative to solve the sustainability limitations arising from battery size constraints in sensor networks. Several considerations in using an environmental energy source are fundamentally different from using batteries. Rather than a limit on the total energy, harvesting transducers impose a limit on the instantaneous power available. Further, environmental energy availability is often highly variable and a deterministic metric such as residual battery capacity is not available to characterize the energy source. The different nodes in a sensor network may also have different energy harvesting opportunities. Since the same end-user performance may be achieved using different workload allocations at multiple nodes, it is important to adapt the workload allocation to the spatio-temporal energy availability profile in order to enable energy-neutral operation of the network. This paper describes power management techniques for such energy harvesting sensor networks. Platform design considerations as well as power scaling techniques at the node-level and network-level are described.

Keywords: Energy harvesting, Power scaling, Heliomote, Power management

REFERENCES
Synthesis of Synchronous Elastic Architectures

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ABSTRACT
A simple protocol for latency-insensitive design is presented. The main features of the protocol are the efficient implementation of elastic communication channels and the automatable design methodology. With this approach, fine-granularity elasticity can be introduced at the level of functional units (e.g. ALUs, memories). A formal specification of the protocol is defined and an efficient scheme for the implementation of elasticity that involves no datapath over-head is presented. The opportunities this protocol opens for microarchitectural design are discussed.

Keywords: Latency-insensitive design, latency-tolerance, protocols, synthesis.

REFERENCES

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ABSTRACT
We propose a statistical approach for minimizing on-chip communication bus width and number of buses with reduced communication energy under timing yield constraint. The slack is exploited to maximize sharing of buses and to reduce energy by simultaneously scaling the voltage during the communication synthesis. Because of the diversity of applications to be run on a single SoC, there exists variability of data size to be transferred among the on-chip communicating modules. This variability of data size is modeled as a normally distributed random variable. The resulting synthesis problem is relaxed to the convex quadratic optimization problem and is solved efficiently using a convex optimization tool. The effectiveness of our approach is demonstrated by applying optimization to an automatically generated benchmark and a real-life application. By varying the value of timing yield constraint, a trade-off between minimization of buses and energy reduction is explored. The experimental results show the significant reduction of communication energy with the increasing timing yield. However, the timing yield offers a limitation to minimize the size of bus width and number of buses, if the yield is increased beyond a certain limit.

Keywords: Communication Bus Synthesis, Voltage Scaling.

REFERENCES


Optimization of Area under a Delay Constraint in Digital Filter Synthesis Using SAT-Based Integer Linear Programming

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ABSTRACT
In this paper, we propose an exact algorithm for the problem of area optimization under a delay constraint in the synthesis of multiplierless FIR filters. To the best of our knowledge, the method presented in this paper is the only exact algorithm designed for this problem. We present the results of the algorithm on real-sized filter instances and compare with an improved version of a recently proposed exact algorithm designed for the minimization of area. We show that in many cases delay can be minimized without any area penalty. Additionally, we describe two approximate algorithms that can be applied to instances which cannot be solved, or take too long, with the exact algorithm. We show that these algorithms find similar solutions to the exact algorithm in less CPU time.

Keywords: Multiple constant multiplication, multiplierless digital filter design, area optimization, delay optimization.

REFERENCES
Behavior and Communication Co-Optimization for Systems with Sequential Communication Media

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ABSTRACT
In this paper we propose a new communication synthesis approach targeting systems with sequential communication media (SCM). Since SCMs require that the reading sequence and writing sequence must have the same order, different transmission orders may have a dramatic impact on the final performance. However, the problem of determining the best possible communication order for SCMs is not adequately addressed by prior work. The goal of our work is to consider behaviors in communication synthesis for SCM, detect appropriate transmission order to optimize latency, automatically transform the behavior descriptions, and automatically generate driver routines and glue logics to access physical channels. Our algorithm, named SCOOP, successfully achieves these goals by behavior and communication co-optimization. Compared to the results without optimization, we can achieve an average 20% improvement in total latency on a set of real-life benchmarks.

Keywords: Communication, FIFO, Optimization, Scheduling, Reordering

REFERENCES
**Synthesis of High-Performance Packet Processing Pipelines**

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**ABSTRACT**
Packet editing is a fundamental building block of data communication systems such as switches and routers. Circuits that implement this function are critical and define the features of the system. We propose a high-level synthesis technique for a new model for representing packet editing functions. Experiments show our circuits achieve a throughput of up to 40Gb/s on a commercially available FPGA device, equal to state-of-the-art implementations.

**Keywords:** Packet processors, Networking, FPGAs, high-level synthesis

**REFERENCES**
ABSTRACT
Increasing employment of chip multiprocessors in embedded computing platforms requires a fresh look at conventional code parallelization schemes. In particular, any compiler-based parallelization scheme for chip multiprocessors should account for the fact that interprocessor communication is cheaper than off-chip memory accesses in these architectures. Based on this observation, this paper proposes a constraint network based approach to code parallelization for chip multiprocessors. Constraint networks have proven to be a useful mechanism for modeling and solving computationally intensive tasks in artificial intelligence. They operate by expressing a problem as a set of variables, variable domains and constraints and define a search procedure that tries to satisfy the constraints (an acceptable subset of them) by assigning values to variables from their specified domains. This paper demonstrates that it is possible to use a constraint network based formulation for the problem of code parallelization for chip multiprocessors. Our experimental evaluation shows that not only a constraint network based approach is feasible for our problem but also highly desirable since it outperforms all other parallelization schemes tested in our experiments.

Keywords: chip multiprocessing, constraint network, compiler

REFERENCES
Buffer Memory Optimization for Video Codec Application Modeled in Simulink

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ABSTRACT
Reduction of the on-chip memory size is a key issue in video codec system design. Because video codec applications involve complex algorithms that are both data-intensive and control-dependent, memory optimization based on global and precise analysis of data and control dependency is required. We generate a memory-efficient C code from a restricted Simulink model, which can represent both data and control dependency explicitly, by applying two buffer memory optimization techniques: copy removal and buffer sharing. Copy removal is performed while parsing the Simulink model. Buffer sharing requires global scheduling and formal lifetime analysis. Experimental results on an H.264 video decoder show that the buffer memory size and execution time of the C code generated by the proposed method are 71% and 32% less than those of the C code produced by Simulink’s C code generator, respectively. When compared to the hand written C code, the memory size was reduced by 27% while its execution time was increased by only 3%.

Keywords: memory size reduction, video codec application, Simulink

REFERENCES
ABSTRACT
Numerous variations of configurable caches, having variable parameters like total size, line size, and associativity, have been proposed in commercial microprocessors in recent years. Tuning a configurable cache to a target application has been shown to reduce memory-access power by over 50%. However, searching the configuration space for the best configuration can require much time or power, even when using recent cache tuning heuristics. We sought to determine, for a particular domain of applications, the smallest subset of cache configurations that would still enable effective tuning. For a suite of 34 benchmarks and a cache with 18 possible configurations, we determine through an exhaustive search of all possible subsets, that only 3 or 4 candidate configurations are necessary to support tuning. We introduce a new heuristic, adapted from an efficient and effective heuristic developed for data mining, to quickly determine the best configurations for any sized subset, with near optimal results. We then consider a configurable cache with 17,640 possible configurations and improve our heuristic to include a pre-pruning step, yielding near optimal tuning results. We conclude that only 3 or 4 possible cache configurations are needed to offer a near optimal configuration for every benchmark in our suite - resulting in a 91% reduction in design space exploration time over a state-of-the-art cache tuning heuristic.

Keywords: Configurable cache tuning, cache optimization, low energy.

REFERENCES


High-Performance Operating System Controlled Memory Compression

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ABSTRACT
This article describes a new software-based on-line memory compression algorithm for embedded systems and presents a method of adaptively managing the uncompressed and compressed memory regions during application execution. The primary goal of this work is to save memory in disk-less embedded systems, resulting in greater functionality, smaller size, and lower overall cost, without modifying applications or hardware. In comparison with algorithms that are commonly used in on-line memory compression, our new algorithm has a comparable compression ratio but is twice as fast. The adaptive memory management scheme effectively responds to the predicted needs of applications and prevents on-line memory compression deadlock, permitting reliable and efficient compression for a wide range of applications. We have evaluated our technique on an embedded portable device and have found that the memory available to applications can be increased by 150%, allowing the execution of applications with larger working data sets, or allowing existing applications to run with less physical memory.

Keywords: Virtual memory, Compression

References
A Cost-Effective Implementation of an ECC-protected Instruction Queue for Out-of-Order Microprocessors

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ABSTRACT
Major sources of transient errors in microprocessors today include noise and single event upsets. As feature sizes and voltages are reduced to create faster, more efficient, and computationally more powerful processors, these errors will increase significantly. We show that (contrary to conventional wisdom) error correction codes (ECC) can be efficiently utilized to handle these errors as instructions are being processed through the microprocessor pipeline. We will analyze some of the tradeoffs involved in a hardware implementation of ECC for the instruction queue with respect to performance, power, area, and reliability. Specifically, for an environment with high error rates, we show that we can correct all single bit errors with a negligible drop in performance. Our approach can be generalized to other data structures within the microprocessor, including the register file and reorder buffer.

Keywords: Reliability, Error Correcting Codes, Instruction Queue.

REFERENCES
ABSTRACT
This panel discusses the following topics. With the ongoing trend towards more and more
digitization in applications ranging from multimedia to telecommunications, there is a big debate
about whether there will remain a need for analog circuits in scaled technologies. Analog circuits
do not seem to take advantage of nanometer CMOS; rather they suffer from it. So if the question
is asked “Will analog scale?”, you get conflicting opinions. One camp argues for an almost-all-
digital future: analog/RF content should be limited, because it’s difficult, expensive, risky, and
can be done with DSP. The opposing camp counters that some critical circuits simply do not
want (or need) to scale, and analog is only “risky” when you let digital designers do it. So, what
is the future role of analog circuits in scaled CMOS, and can analog EDA tools help in this?
Keywords: Analog design; mixed-signal design; RF design; analog design methodologies;
analog CAD tools

REFERENCES
NATURE: A Hybrid Nanotube/CMOS Dynamically Reconfigurable Architecture

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ABSTRACT
Recent progress on nanodevices, such as carbon nanotubes and nanowires, points to promising directions for future circuit design. However, nanofabrication techniques are not yet mature, making implementation of such circuits, at least on a large scale, in the near future infeasible. However, if photolithography could be used to implement circuits using these nanodevices, then hybrid nano/CMOS chips could be fabricated and the benefits of nanotechnology could be utilized immediately. A startup company, called Nantero, has developed and implemented a non-volatile nanotube random-access memory (NRAM) using photo-lithography that is considerably faster and denser than DRAM, has much lower power consumption than DRAM or flash, has similar speed to SRAM and is highly resistant to environmental forces (temperature, magnetism). In this paper, we propose a novel high performance reconfigurable architecture, called NATURE, that utilizes CMOS logic and NRAMs. Use of the highly-dense NRAMs allows large on-chip configuration storage, enabling fine-grain run-time reconfiguration and temporal logic folding of a circuit before being mapped to the architecture. This can significantly increase the logic density of NATURE (by over an order of magnitude for larger circuits) while remaining competitive in performance. Compared to traditional reconfigurable architectures, NATURE also allows the designer the flexibility to adjust the level of logic folding in order to improve performance or perform area-performance trade-offs. Experimental results establish its efficacy and give comparisons with today’s mainstream FPGA technology which does not allow logic folding.

Keywords: NRAM, run-time reconfiguration, logic folding

REFERENCES
Modeling and Analysis of Circuit Performance of Ballistic CNFET

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ABSTRACT
With the advent of carbon nanotube technology, evaluating circuit and system performance using these devices is becoming extremely important. In this paper, we propose a quasi-analytical device model for intrinsic ballistic CNFET, which can be used in any conventional circuit simulator like SPICE. This simple quasianalytical model is seen to be effective in a wide variety of CNFET structures as well as for a wide range of operating conditions in the digital circuit application domain. We also provide an insight how the parasitic fringe capacitance in state-of-the-art CNFET geometries impacts the overall performance of CNFET circuits. We show that unless the device width can be significantly reduced, the effective gate capacitance of CNFET will be strongly dominated by the parasitic fringe capacitances and the superior performance of intrinsic CNFET over silicon MOSFET cannot be achieved in circuit.

Keywords: Ballistic carbon nanotube FET (CNFET), circuit compatible model, parasitic capacitance, circuit performance.

REFERENCES
Topology Aware Mapping of Logic Functions onto Nanowire-based Crossbar Architectures

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ABSTRACT
Highly regular, nanodevice based architectures have been proposed to replace pure CMOS based architectures in the emerging post CMOS era. Since bottom-up self-assembly is used to build these architectures, regular nanowire crossbars are emerging as a promising candidate. While these regular structures resemble CMOS programmable logic arrays (PLAs), PLA logic synthesis methodologies fail to solve the associated problems since the length and connectivity constraints imposed by individual nanowires in these crossbars translate into challenges hitherto not considered. These strict topological constraints should be considered while mapping Boolean functions onto nanowire crossbars during logic synthesis. We develop a mathematical model for this problem, an algorithm to solve it and three heuristics to improve the algorithm runtime.

Keywords: Nanoelectronic, PLA, Crossbar, Logic synthesis

REFERENCES
A New Hybrid FPGA with Nanoscale Clusters and CMOS Routing

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Abstract
In this paper we propose a hybrid FPGA using nanoscale clusters with an architecture similar to clusters of traditional CMOS FPGAs. The proposed cluster is made of a crossbar of nanowires configured to implement the required LUTs and intra-cluster MUXes. A CMOS interface is also proposed to provide configuration and latching for the nanoscale cluster. Inter-cluster routing is assumed to remain at CMOS scale. Experimental analysis is performed to evaluate area and performance of the hybrid FPGA and results are compared with traditional fully CMOS FPGA (scaled to 22nm). Up to 75% area reduction was obtained from implementing MCNC benchmarks on hybrid FPGA. Performance of the hybrid FPGA is shown to be close to that of CMOS FPGA.

Keywords: Reconfigurable Nanoscale Devices, Molecular Electronics, FPGA

REFERENCES
Directed-Simulation Assisted Formal Verification of Serial Protocol and Bridge

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Abstract
Robust verification of protocol conversion and arbitration schemes of SoC bridges forms a significant component of the overall SoC verification. Formal verification provides a way to achieve this, but a naive approach often leads to explosion of the state space, and is impractical for most of today's protocols and bridges. This problem is further complicated in the presence of serial protocols, where control and data are mixed together and transactions continue for very great depths. White-box verification is not a feasible solution, since these bridges are often imported or generated from other sources, and internal information is not readily available. In this paper, we propose a black-box and hybrid approach to this problem, by judiciously mixing simulation and formal verification. We illustrate our approach by applying it to two dual stage bridges that perform serial to parallel protocol conversion and vice versa.

Keywords: Formal verification, Model checking, Serial Protocol.

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http://www.cse.ucsc.edu/classes/cmpe123/Fall02/files/I2C_BUS_SPECIFICATION.pdf
Guiding Simulation with Increasingly Refined Abstract Traces

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Abstract
We combine abstraction refinement and simulation to provide a more efficient approach to checking invariant properties whose only counter-examples are very long traces. We allow each transition of an abstract error trace to map to multiple transitions of the concrete error trace and simulate pseudorandom vectors to build segments of the concrete trace. This approach addresses the capacity limitation of the formal verification engine as well as the short-sightedness of the simulator, thus providing a more effective technique for deep, subtle bugs.

Keywords: model checking, abstraction refinement, simulation

References
MINING GLOBAL CONSTRAINTS FOR IMPROVING BOUNDED SEQUENTIAL EQUIVALENCE CHECKING

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ABSTRACT
In this paper, we propose a novel technique on mining relationships in a sequential circuit to discover global constraints. In contrast to the traditional learning methods, our mining algorithm can find important relationships among several nodes efficiently. The nodes involved may often span several timeframes, thus improving the deductibility of the problem instance. Experimental results demonstrate that the application of these global constraints to SAT-based bounded sequential equivalence checking can achieve one to two orders of magnitude speedup. In addition, because it is orthogonal to the underlying SAT solver, it can help to enhance the efficacy of typical SAT based verification flows.

Keywords: Mining, SAT, Multi-node Constraint.

REFERENCES


ABSTRACT
In deep submicron feature sizes continue to shrink aggressively beyond the natural capabilities of the 193 nm lithography used to produce those features thanks to all the innovations in the field of resolution enhancement techniques (RET). With reduced feature sizes and tighter pitches die level variations become an increasingly dominant factor in determining manufacturing yield. Thus a prediction of design-specific features that impact intra-die variability and correspondingly its yield is extremely valuable as it allows for altering such features in a manner that reduces intra-die variability and improves yield. In this paper, a manufacturing yield model which takes into account both physical layout features and manufacturing fluctuations is proposed. The intra-die systematic variations are evaluated using a physics-based model as a function of a design’s physical layout. The random variations and their across-die spatial correlations are obtained from data harvested from manufactured test structures. An efficient algorithm is proposed to reduce the order of the numerical integration in the yield model. The model can be used to (i) predict manufacturing yields at the design stage and (ii) enhance the layout of a design for higher manufacturing yield.

Keywords: Manufacturing Yield, Systematic Variation, Random Variation, Spatial Correlation, CMP

REFERENCES
Novel Full-Chip Gridless Routing Considering Double-Via Insertion

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ABSTRACT

As the technology node advances into the nanometer era, via-open defects are one of the dominant failures. To improve via yield and reliability, redundant-via insertion is a highly recommended technique proposed by foundries. Traditionally, double-via insertion is performed at the post-layout stage. The increasing design complexity, however, leaves very limited space for post-layout optimization. It is thus desirable to consider the double-via insertion at both routing and post-routing stages. In this paper, we present a new full-chip gridless routing system considering double-via insertion for yield enhancement. To fully consider double vias, the router applies a novel two-pass, bottom-up routability-driven routing framework. We also propose a new post-layout double-via insertion algorithm to achieve a higher insertion rate. Based on a bipartite graph matching formulation, we develop an optimal double-via insertion algorithm for the cases with up to three routing layers and the stack-via structure, and then extend the algorithm to handle the general cases. Experiments show that our methods significantly improve the via count, the number of dead vias, double-via insertion rates, and running times.

Keywords: Manufacturability, redundant via insertion, routing

REFERENCES


Optimal Jumper Insertion for Antenna Avoidance under Ratio Upper-Bound

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ABSTRACT
Antenna effect may damage gate oxides during plasma-based fabrication process. The antenna ratio of total exposed antenna area to total gate oxide area is directly related to the amount of damage. Jumper insertion is a common technique applied at routing and post-layout stages to avoid and to fix the problems caused by the antenna effect. This paper presents an optimal algorithm for jumper insertion under the ratio upper-bound. It handles Steiner trees with obstacles. The algorithm is based on dynamic programming while works on free trees. The time complexity is $O(|V|^2)$ and the space complexity is $O(|V|^2)$, where $|V|$ is the number of nodes in the routing tree and $\alpha$ is a factor depending on how to find a non-blocked position on a wire for a jumper.

Keywords: Antenna Effect, Jumper Insertion

REFERENCES
ABSTRACT
Due to the shrinking of feature size and reduction in supply voltages, nanoscale circuits have become more susceptible to radiation induced transient faults. In this paper, we present a symbolic framework based on BDDs and ADDs that enables analysis of combinational circuit reliability from different aspects: output susceptibility to error, influence of individual gates on individual outputs and overall circuit reliability, and the dependence of circuit reliability on glitch duration, amplitude, and input patterns. This is demonstrated by the set of experimental results, which show that the mean output error susceptibility can vary from less than 0.1%, for large circuits and small glitches, to about 30% for very small circuits and large enough glitches. The results obtained with the proposed symbolic framework are within 7% average error and up to 5000X speedup when compared to HSPICE detailed circuit simulation. The framework can be used for selective gate sizing targeting radiation hardening which is done only for gates with error impact exceeding a certain threshold. Using such a technique, soft error rate (SER) can be reduced by 25-67% for various threshold values, when applied to a subset of ISCAS’85 and mcnc’91 benchmarks.

Keywords: SER, reliability symbolic techniques

REFERENCES


A Design Approach for Radiation-hard Digital Electronics

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ABSTRACT
In this paper, we present a novel circuit design approach for radiation hardened digital electronics. Our approach is based on the use of shadow gates, whose task it is to protect the primary gate in case it is struck by a heavy cosmic ion. We locally duplicate the gate to be protected, and connect a pair of transistors (or diodes) between the outputs of the original and shadow gates. These transistors turn on when the voltages of the two gates deviate during a radiation strike. Our experiments show that at the level of a single gate, our circuit structure has a delay overhead of about 4% on average, and an area overhead of over 100%. At the circuit level, however, we do not need to protect all gates. We present a methodology to selectively protect specific gates of the circuit in a manner that guarantees radiation tolerance for the entire circuit. With this methodology, we demonstrate that at the circuit level, the delay overhead is about 4% and the placed-and-routed area overhead is 30%, compared to an unprotected circuit (for delay mapped designs)

Keywords: SEU, Radiation-hard

REFERENCES
A Family of Cells to Reduce the Soft-Error-Rate in Ternary-CAM

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ABSTRACT
Modern integrated circuits require careful attention to the soft-error rate (SER) resulting from bit upsets, which are normally caused by alpha particle or neutron hits. These events, also referred to as single-event upsets (SEUs), will become more problematic in future technologies. This paper presents a ternary content-addressable memory (CAM) design with high immunity to SEU. Conventionally, error-correcting codes (ECC) have been used in SRAMs to address this issue, but these techniques are not immediately applicable to CAMs because they depend on processing the full contents of the memory word outside the array, which is not possible in a normal CAM access. We propose a family of TCAM cells that reduce the SER at the cost of some area increase. An SER reduction of up to 40% can be obtained with a 18% increase of area; another design reduces the SER by 16% with only a 5% increase in area.

Keywords: Content-AddressableMemory, Soft-Error Rate.

REFERENCES
Process Variation Aware OPC with Variational Lithography Modeling

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ABSTRACT
Optical proximity correction (OPC) is one of the most widely used resolution enhancement techniques (RET) in nanometer designs to improve subwavelength printability. Conventional model-based OPC assumes nominal process parameters without considering process variations, due to prohibitive runtimes of lithography simulations across process windows. This is the first paper to propose a true process-variation aware OPC (PV-OPC) framework. It is enabled by the variational lithography modeling and guided by the variational edge placement error (V-EPE) metrics. Due to the analytical nature of our models, our PV-OPC is only about 2-3 times slower than the conventional OPC, but it explicitly considers the two main sources of process variations (dosage and focus) during OPC. Thus our post PV-OPC results are much more robust than the conventional OPC ones, in terms of both geometric printability and electrical characterization under process variations.

Keywords: Lithography modeling, process variation, OPC

REFERENCES


Modeling of Intra-die Process Variations for Accurate Analysis and Optimization of Nano-scale Circuits

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ABSTRACT
This paper proposes the use of Karhunen-Loève Expansion (KLE) for accurate and efficient modeling of intra-die correlations in the semiconductor manufacturing process. We demonstrate that the KLE provides a significantly more accurate representation of the underlying stochastic process compared to the traditional approach of dividing the layout into grids and applying Principal Component Analysis (PCA). By comparing the results of leakage analysis using both KLE and the existing approaches, we show that using KLE can provide up to 4 - 5X reduction in the variability space (number of random variables) while maintaining the same accuracy. We also propose an efficient leakage minimization algorithm that maximizes the leakage yield while satisfying probabilistic constraints on the delay.

Keywords: Statistical, Process Variations, Leakage, Karhunen-Loeve, intra-die, correlations

REFERENCES
Computation of Accurate Interconnect Process Parameter Values for Performance Corners under Process Variations

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Abstract
This paper introduces a fast analytical model for determining accurate parasitic values for best- and worst-case delays of a stage under interconnect process variations. The inputs to the model are the nominal values for each interconnect and device parameter and the amount of variation in each interconnect parameter. The outputs of the model are the interconnect parameter dimensions within the range of process variation that yield the best- and worst-case delay of a stage. Simulations show that our model accurately predicts the performance corners of a stage while those predicted by traditional best/worst-case analysis methodologies can have an error of up to 28.42%.

Keywords: Corners, STA, Delay, Variations, Interconnect

REFERENCES
Standard Cell Characterization Considering Lithography Induced Variations

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ABSTRACT
As VLSI technology scales toward 65nm and beyond, both timing and power performance of integrated circuits are increasingly affected by process variations. In practice, people often treat systematic components of the variations, which are generally traceable according to process models, in the same way as random variations in process corner based methodologies. Consequently, the process corner models are unnecessarily pessimistic. In this paper, we propose a new cell characterization methodology which captures lithography induced gate length variations. A new technique of dummy poly insertion is suggested to shield inter-cell optical interferences. This technique together with standard cells characterized using our methodology will let current design flows comprehend the variations almost without any changes. Experimental results on industrial designs indicate that our methodology can averagely reduce timing variation window by 8%-25%, power variation window by 55% when compared to a worst case approach. For an industrial low power design, over 300ps reduction on the path delay variation is obtained by using cells characterized according to our methodology.

Keywords: OPC, design flow, RET, process CD, standard cell, CAD

REFERENCES
**Building A Verification Test Plan: Trading Brute Force For Finesse**

**Chair:** Sharad Malik - Princeton University, Princeton, NJ  
**Panelists:** Janick Bergeron – Synopsys, Ottawa, Canada  
Harry Foster - Mentor Graphics, Dallas, TX  
Andrew Piziali - Cadence Design Systems, Parker, TX  
Raj Shekher Mitra - Texas Instruments, Bangalore, India  
Catherine Ahlschlager - Sun Microsystems, Sunnyvale, CA  
Doron Stein - Cisco Systems, Inc., Netanya, Israel

**Keywords:** Design Verification, Verification Test Plan, Functional Simulation, Formal Verification, Coverage

**PANEL SUMMARY**

The increasing complexity of today’s designs has only served to further intensify the pain of functional verification. Any strategy for success here must include a verification test plan – one that trades brute force with finesse. In so doing, not only is the pain reduced, but additional benefits are quickly derived, such as greater predictability, more aggressive innovation and late stage spec changes which can be made with confidence.

Certainly, verification teams have a need to know, while a design is being verified, if their efforts are progressing according to schedule. In order to declare verification done, the team needs to be able to effectively assess the risk of bug escapes. Teams typically use a verification coverage plan to help them address these issues, but increasing complexity and IP integration place rising demands upon verification teams.

In the past, test plans described the scenarios under which you needed to test a device. With the changes imposed by emerging technologies, test plans have needed to expand and evolve to adapt. While coverage is at the core of functional verification, it is a topic of much discussion and debate.

What are the different coverage metrics being used today, and do these metrics properly address the functional verification challenge? How do you begin to integrate multiple verification processes into a single test plan? This panel will attempt to address these important questions.

As chip complexity and IP integration have increased, companies have begun testing at higher levels of abstraction, moving more and more to ESL techniques to better understand the overall system functionality. Industry leading companies have begun to embrace the use of formal verification, emulation and acceleration to drive greater verification success in the drive for greater quality and schedule predictability. But, what value do these new verification processes bring, and what usage and integration challenges do they pose?

In this panel users and suppliers debate the optimal mix of formal, simulation, hardware acceleration and emulation, examining ways to ensure new features aren’t dropped pretapeout from ‘inadequate verification’.

It’s no longer just a test plan discussion, but an examination of how test plans are going to need to change given emerging technologies.
Electronics Beyond Nano-scale CMOS

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ABSTRACT
This paper presents nano-scale CMOS outlook, discusses the three tenets that have made electronics successful in the past, and using these tenets conclude that there is nothing on the horizon yet that has promise to replace CMOS. Therefore, we will make CMOS work for a foreseeable future.

Keywords: CMOS, Power, Nano, Variability.

References
Are Carbon Nanotubes the Future of VLSI Interconnections?

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ABSTRACT
Increasing resistivity of copper with scaling and rising demands on current density requirements are driving the need to identify new wiring solutions for deep nanometer scale VLSI technologies. Metallic carbon nanotubes (CNTs) are promising candidates that can potentially address the challenges faced by copper and thereby extend the lifetime of electrical interconnects. This paper examines the state-of-the-art in CNT interconnect research and discusses both the advantages and challenges of this emerging nanotechnology.

Keywords: Carbon nanotubes, interconnects, VLSI.

REFERENCES
ABSTRACT
Silicon technology based nonvolatile memories (NVM) have achieved widespread adoption for code and data storage applications. In the last 30 years, the traditional floating gate bitcell has been scaled following Moore’s law, but recently scaling limits have been encountered which will require alternative solutions after the 65 nm technology node. Both evolutionary and novel solutions are being pursued in the industry. While the traditional floating gate technology will scale to the 65 nm node, novel device structures and array architectures will be needed past that node.

Keywords: Nonvolatile memories; floating gate; SONOS; nanocrystal; MRAM; phase change memory; FeRAM

REFERENCES
ABSTRACT

Formal languages are increasingly used to describe the functional requirements (specifications) of circuits. These requirements are used as a means to communicate design intent and as basis for verification. In both settings it is of utmost importance that the specifications are of high quality. However, formal requirements are seldom the object of validation, even though they can be hard to understand and interactions between them can be subtle. In this paper we present techniques and guidelines to explore and assure the quality of a formal specification. We define a technique to interactively explore the semantics of a specification by simulating its behavior for user-defined scenarios. Furthermore, we define techniques to automatically check specifications against a set of user-provided assertions, which must be satisfied, and a set of possibilities, which must not be contradicted. The proposed techniques support the user in the iterative development and refinement of high-quality specifications.

Keywords: Requirements Analysis, Hardware Design, Specification, Property Assurance, Property Simulation.

REFERENCES


Test Generation Games from Formal Specifications

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ABSTRACT
In this paper, we present methods for automatic test generation from formal specifications. These are used to create intelligent test benches that are able to cover corner case behaviors in much less time. We have developed a prototype tool for intelligent test generation within the layered test bench architecture proposed in RVM. We present results on verification IPs of standard bus protocols to show the effectiveness of our approach.

Keywords: Test Generation, Vacuity, Realizability

REFERENCES
Optimal Link Scheduling on Improving Best-Effort and Guaranteed Services Performance in Network-on-Chip Systems

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ABSTRACT
With the advent of the multiple IP-core based design using Network on Chip (NoC), it is possible to run multiple applications concurrently. For applications with hard deadline, guaranteed services (GS) are required to satisfy the deadline requirement. GS typically underutilizes the network resources. To increase the resources utilization efficiency, GS applications are always complement with the best-effort services (BE). To allow more resource available for BE, the resource reservation for GS applications, which depends heavily on the scheduling of the computation and communication, needs to be optimized. In this paper we propose a new approach based on optimal link scheduling to judiciously schedule the packets on each of the links such that the maximum latency of the GS application is minimized with minimum network resources utilization. To further increase the performance, we propose a novel router architecture using a shared-buffer implementation scheme. The approach is formulated using integer linear programming (ILP). We applied our algorithm on real applications and experimental results show that significant improvement on the overall execution time and link utilization can be achieved.

Keywords: Network-on-Chip, Latency, Routing

References
Prediction-based Flow Control for Network-on-Chip Traffic

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ABSTRACT
Networks-on-Chip (NoC) architectures provide a scalable solution to on-chip communication problem but the bandwidth offered by NoCs can be utilized efficiently only in presence of effective flow control algorithms. Unfortunately, the flow control algorithms published to date for macronetworks, either rely on local information, or suffer from large communication overhead and unpredictable delays. Hence, using them in the NoC context is problematic at best. For this reason, we propose a predictive closed-loop flow control mechanism and make the following contributions: First, we develop traffic source and router models specifically targeted to NoCs. Then, we utilize these models to predict the cases of possible congestion in the network. Based on this information, the proposed scheme controls the packet injection rate at traffic sources in order to regulate the total number of packets in the network. Evaluations involving real and synthetic traffic patterns show that the proposed controller delivers a superior performance compared to the traditional switch-to-switch flow control algorithms.

Keywords: Multi-processor systems, networks-on-chip, flow control, congestion control.

REFERENCES
ABSTRACT
In this work we present a multi-path routing strategy that guarantees in-order packet delivery for Networks on Chips (NoCs). We present a design methodology that uses the routing strategy to optimally spread the traffic in the NoC to minimize the network bandwidth needs and power consumption. We also integrate support for tolerance against transient and permanent failures in the NoC links in the methodology by utilizing spatial and temporal redundancy for transporting packets. Our experimental studies show large reduction in network bandwidth requirements (36.86% on average) and power consumption (30.51% on average) compared to singlepath systems. The area overhead of the proposed scheme is small (a modest 5% increase in network area). Hence, it is practical to be used in the on-chip domain.

keywords: Systems on Chip, networks on chip, routing, multipath, fault-tolerance, re-order buffers, flow control.

REFERENCES
DyXY - A Proximity Congestion-Aware Deadlock-Free Dynamic Routing Method for Network on Chip

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ABSTRACT
A novel routing algorithm, namely dynamic XY (DyXY) routing, is proposed for NoCs to provide adaptive routing and ensure deadlock-free and livelock-free routing at the same time. A new router architecture is developed to support the routing algorithm. Analytical models based on queuing theory are developed for DyXY routing for a two-dimensional mesh NoC architecture, and analytical results match very well with the simulation results. It is observed that DyXY routing can achieve better performance compared with static XY routing and odd-even routing.

Keywords: Network-on-Chip, Packet Routing, Queuing Theory.

REFERENCES
The Importance of Adopting a Package-Aware Chip Design Flow

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Abstract
In this paper, we talk about the short- and long-term implications of ignoring the relationship between the chip, package and PCB during I/O planning and how these issues will manifest themselves as we move toward 65 and 45nm technology. It also introduces a whole new approach to chip/package I/O planning and optimization. This new approach simultaneously synthesizes the entire interconnect from the I/O driver to the package ball and establishes an interconnect plan that is optimized for both chip and package.

Keywords: Co-Design, Chip, Package, Substrate, I/O, Synthesis, Prototyping, Exploration, RDL, Concurrent, Flip Chip, Routing
Silicon Carrier for Computer Systems

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ABSTRACT
System-on-Package (SOP) based on silicon carriers has the potential to provide modular design flexibility and high-performance integration of heterogeneous chip technologies for a wide range of two- and three-dimensional product applications. Key technology enablers include silicon through-vias, high-density wiring, high-I/O chip interconnection, and supporting test and assembly technologies. This paper describes the electrical characterization of key technical elements of the silicon carrier and discusses the significance of those elements in enhancing the overall system performance. The paper also discusses some methodologies that may allow silicon carrier technical elements to be easily integrated within existing EDA tools.

Keywords: Silicon carrier, System on Package, CMOS scaling, Micro-bumps, electrical modeling, Chip-Package Co-design, computer system.

REFERENCES
ABSTRACT
This paper describes the design methodology, simulation, and tools used to design a 4.25 Gb/s high output swing laser driver (LD) and the electrical to optical interface from the LD to the laser diode. The quality of the optical output of a fiber optic communication channel is mainly determined by the LD and the electrical interface from the LD to the laser diode. Of particular importance in the interface is how well the LD overcomes the impact of the parasitic, resistive, capacitive, and inductive elements associated with the bondpad, bondwires, package, PCB transmission lines, passive components, and laser diode and its bondwires. The EDA tools used to model the electrical parasitics focus on RF and microwave applications and provide high frequency S-parameter models. This environment requires a stable time domain model of the electrical to optical interface. The presented LD integrated circuit operates from 155 Mb/s to 4.25 Gb/s with rise and fall times of 70 ps or less and a wide output voltage range, and a modulation current range of 5 mA to 85 mA.

Keywords: Laser driver, laser diode, electrical to optical interface.

REFERENCES
Power-Centric Design of High-Speed I/Os

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ABSTRACT

With increasing aggregate off-chip bandwidths exceeding terabits/second (Tb/s), the power dissipation is a serious design consideration. Additionally, design of I/O links is constrained by a complex set of specifications such as voltage levels, voltage noise, signal deterministic jitter, random jitter, slew rate, BER etc. These specifications lead to complex tradeoffs for both circuits and circuit architecture in order to minimize power. This paper presents a design framework that enables the analysis of tradeoffs in the design of an I/O transmitter. The design framework includes BER analysis with a channel model coupled with logic sizing optimization that is constrained by the desired signaling specification.

Keywords: I/O, Serial Link, Power Minimization, Convex Optimization, Channel Model.

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A 10.6mW/0.8pJ Power-Scalable 1GS/s 4b ADC in 0.18μm CMOS with 5.8GHz ERBW

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ABSTRACT
We present a 4-bit power scalable flash analog-to-digital converter in digital 0.18-μm CMOS, targeting low power ultra-wide band receivers. To minimize static power consumption, we exploit dynamic comparators with built-in digitally tunable thresholds. The converter has been realized and tested outperforming recent comparable designs even in more advanced technologies. The main performance figures include 5.8GHz effective resolution bandwidth and 0.8pJ/conversion-step at 1-GS/s and Nyquist conditions.

Keywords: Ultra-low power high-speed converter design, flash converters, Ultra-Wide Band.

REFERENCES
SOC-NLNA: Synthesis and Optimization for Fully Integrated Narrow-Band CMOS Low Noise Amplifiers

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ABSTRACT
In this paper we present SOC-NLNA, a systematic synthesis methodology for fully integrated narrow-band CMOS Low Noise Amplifiers (LNA) in high performance System-on-Chip (SoC) designs. SOC-NLNA is based on deterministic numerical nonlinear optimization and the Normal Boundary Intersection (NBI) method for Pareto optimization. To enable SoC integration, we simultaneously optimize both devices and passive components to yield integrated inductor values that are significantly less than those generated by traditional design techniques. When the synthesized LNAs are simulated using Cadence SpectreRF, SOC-NLNA yields up to 35 and 58 percent improvement in noise figure and gain. Leveraging the efficiency of our methodology, we are able to generate the Pareto surfaces between LNA performance metrics in seconds.

Keywords: Low Noise Amplifier, LNA Optimization, Analog Synthesis

REFERENCES
Chameleon ART: A Non-Optimization Based Analog Design Migration Framework

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ABSTRACT
Presented in this paper is a tool that automatically migrates analog designs from one process to another while keeping circuit and layout topologies. A netlist migration engine recalculates the new device dimensions in the target technology followed by a layout migration engine that compacts the design according to the new process design rules. The overall framework preserves design intelligence embedded in the original IP such as symmetry, hierarchy, placement and routing. The circuit migration engine, being very fast, can retarget large analog blocks in only a few minutes while giving same or better performance of the original design. The migration of 3 different circuits is presented to validate the overall methodology. These circuits have been fabricated and measured.

Keywords: Analog Reuse, Design Extraction, Circuit Sizing, Layout Compaction, Layout Retargeting.

REFERENCES
ABSTRACT
The design of complex analog front-ends demands the exploration of a huge design space at different levels of abstraction and using a multitude of simulators. One of the main issues is to guarantee the consistency of the models and the model parameters between the different abstraction levels. A methodology and a tool, called NETLISP, has been developed for the purpose of guaranteeing the consistency between different levels of abstraction. The tool was successfully applied to the design of a multi-mode multi-band analog front-end, showing its applicability on real large-scale designs.

Keywords” Design flow, front-end, object-oriented design, model consistency

REFERENCES
Efficient Simulation of Critical Synchronous Dataflow Graphs

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ABSTRACT

Simulation and verification using electronic design automation (EDA) tools are key steps in the design process for communication and signal processing systems. The synchronous dataflow (SDF) model of computation is widely used in EDA tools for system modeling and simulation in the communication and signal processing domains. Behavioral representations of practical wireless communication systems typically result in critical SDF graphs — they consist of hundreds of components (or more) and involve complex inter-component connections with highly multirate relationships (i.e., with large variations in average rates of data transfer or component execution across different subsystems). Simulating such systems using conventional SDF scheduling techniques generally leads to unacceptable simulation time and memory requirements on modern workstations and high-end PCs. In this paper, we present a novel simulation-oriented SDF scheduler (SOS) that strategically integrates several techniques for graph decomposition and SDF scheduling to provide effective, joint minimization of time and memory requirements for simulating large-scale and heavily multirate SDF graphs. We have implemented the SOS scheduler in the Advanced Design System (ADS) from Agilent Technologies. Our results from this implementation demonstrate large improvements in simulating real-world wireless communication systems (e.g. 3GPP, Bluetooth, 802.16e, CDMA 2000, and XM radio).

Keywords: Synchronous dataflow, Scheduling, Simulation.

REFERENCES

Exploring Trade-Offs in Buffer Requirements and Throughput Constraints for Synchronous Dataflow Graphs

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ABSTRACT
Multimedia applications usually have throughput constraints. An implementation must meet these constraints, while it minimizes resource usage and energy consumption. The compute intensive kernels of these applications are often specified as Synchronous Dataflow Graphs. Communication between nodes in these graphs requires storage space which influences throughput. We present exact techniques to chart the Pareto space of throughput and storage trade-offs, which can be used to determine the minimal storage space needed to execute a graph under a given throughput constraint. The feasibility of the approach is demonstrated with a number of examples.

Keywords: Synchronous Dataflow, buffering, throughput, optimization.

REFERENCES

GreenBus - A Generic Interconnect Fabric for Transaction Level Modelling

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ABSTRACT

In this paper we present a generic interconnect fabric for transaction level modelling tackling three major aspects. First, a review of the bus and IO structures that we have analysed, which are common in today's system on chip environments, and require to be modelled at a transaction level. Second our findings in terms of the data structures and interface API's that are required in order to model those (and we believe other) busses and IO structures. Third the surrounding infrastructure that we believe can, and should be in place to support the modelling of those busses and IO structures. We will present the infrastructure that we have built, and indicate where our future work will head.

Keywords: On-Chip Communication, SystemC, TLM, SoC

REFERENCES

ABSTRACT
This paper presents a heterogeneous specification methodology built on top of the standard SystemC kernel. The methodology enables abstract specification supporting heterogeneity, which in this context entails the ability to describe and connect parts of the system specification under different models of computation (MoCs). A main and distinguishing contribution of the methodology is that the support is provided while maintaining the standard kernel of SystemC unchanged, by means of a set of specification rules and a heterogeneous support library built on top of the SystemC standard library. This is possible thanks to an abstraction technique that can integrate any new MoC that can be abstracted over the underlying discrete-event simulation kernel. Primitives, guidelines and rules of the specification methodology, including those related to heterogeneous support, and the basis of the abstraction technique are described. Experimental results demonstrate the benefits of the methodology.

Keywords: Heterogeneous Specification, SystemC.

REFERENCES
A Model-driven Design Environment for Embedded Systems

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ABSTRACT

This paper presents a prototype environment for HW/SW co–design of embedded systems based on the Unified Modeling Language (UML) and SystemC. The environment supports a model-driven SoC design methodology which provides a graphical high-level representation of hardware and software components, and allows either C/C++/SystemC code generation from models and a reverse engineering process from code to graphical UML models.

Keywords: HW/SW Co-design, UML, MDA, SystemC.

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ABSTRACT
DNA self-assembly is an emerging technology with potential as a future replacement of conventional lithographic fabrication. A key challenge is the specification of appropriate DNA sequences that are optimal according to specified metrics and satisfy various design rules. To meet this challenge we developed a thermodynamics-based design automation tool to evaluate the vast DNA sequence space (2.8k base pairs) and select appropriate sequences. We use this tool to design DNA nanostructures that were previously impossible with existing text distance based tools. We also show that for nanoscale structures our approach produces superior results compared to existing tools.

Keywords: DNA self-assembly, nanostructure design, optimized self-assembly.

References
Automated Design of Pin-Constrained Digital Microfluidic Arrays for Lab-on-a-Chip Applications

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ABSTRACT
Microfluidics-based biochips, also referred to as lab-on-a-chip (LoC), are devices that integrate fluid-handling functions such as sample preparation, analysis, separation, and detection. This emerging technology combines electronics with biology to open new application areas such as point-of-care diagnosis, on-chip DNA analysis, and automated drug discovery. We propose a design automation method for pin-constrained LoCs that manipulate nanoliter volumes of discrete droplets on a microfluidic array. In contrast to the direct-addressing scheme that has been studied thus far in the literature, we assign a small number of independent control pins to a large number of electrodes in the LoC, thereby reducing design complexity and product cost. We apply the proposed method to a microfluidic array for a set of multiplexed bioassays.

Keywords: Pin-constrained design, virtual partitioning, microfluidic biochips.

REFERENCES
Placement of Digital Microfluidic Biochips Using the T-tree Formulation

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ABSTRACT
Droplet-based microfluidic biochips have recently gained much attention and are expected to revolutionize the biological laboratory procedure. As biochips are adopted for the complex procedures in molecular biology, its complexity is expected to increase due to the need of multiple and concurrent assays on a chip. In this paper, we formulate the placement problem of digital microfluidic biochips with a tree-based topological representation, called T-tree. To the best knowledge of the authors, this is the first work that adopts a topological representation to solve the placement problem of digital microfluidic biochips. Experimental results demonstrate that our approach is much more efficient and effective, compared with the previous unified synthesis and placement framework.

Keywords: Microfluidics, biochip, placement, floorplanning

REFERENCES
A High Density, Carbon Nanotube Capacitor for Decoupling Applications

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ABSTRACT
We present a novel application for carbon nanotube devices, implementing a high density 3-D capacitor, which can be useful for decoupling applications to reduce supply voltage variations. The capacitor consists of staggered layers of interleaved carbon nanotubes, alternately connected to anode and cathode contacts. The device can realize a capacitance/area, significantly larger than the ITRS's projected requirements for year 2018. The capacitance per unit area can exceed 1pF/μm², with a quality factor greater than 100 at 1GHz.

Keywords: Carbon nanotube, interconnect, capacitor, three-dimensional.

REFERENCES
ABSTRACT
A novel method to solve the state encoding problem in Signal Transition Graphs is presented. It is based on the structural theory of Petri nets and can be applied to large specifications with hundreds of signals. This new method opens the door to incorporate logic synthesis in the design flow of large control circuits obtained from high-level specifications. The experimental results validate the quality of the encoded circuits and show the significant improvements that can be obtained by the synthesis of large controllers.

Keywords: Asynchronous circuits, Petri nets, state encoding.

REFERENCES
An Efficient Retiming Algorithm Under Setup and Hold Constraints

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ABSTRACT
In this paper we present a new efficient algorithm for retiming sequential circuits with edge-triggered registers under both setup and hold constraints. Compared with the previous work [17], which computed the minimum clock period in \(O(|V|^3|E|\log |V|)\) time, our algorithm solves the same problem in \(O(|V|^2|E|)\) time. Experimental results validate the efficiency of our algorithm.

Keywords: Retiming

REFERENCES
ExtensiveSlackBalance: an Approach to Make Front-end Tools Aware of Clock Skew Scheduling

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ABSTRACT
In the traditional ASIC flow, clock skew scheduling (CSS), as a method to improve timing, is usually employed during the CTS (clock tree synthesis) step while front-end tools do not take clock skew as a manageable resource. This limits the potential of the subsequent CSS. To overcome such limitations, we design an enhanced CSS algorithm ExtensiveSlackBalance and integrate it into the back-annotation and re-optimization iterations of the current industrial flow. Experiment results show that, the clock frequency can be improved to 26.2% on average compared to 6.4% in the traditional ASIC flow.

Keywords: clock skew, skew scheduling, logic synthesis, back-annotation

REFERENCES
Budgeting-Free Hierarchical Design Method for Large Scale and High-Performance LSIs

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ABSTRACT
This paper describes a new hierarchical design method for large scale and high-performance LSIs, which eliminates the need to perform budgeting. The budgeting step in hierarchical design partitions the total propagation time constraint for a path between any two flip-flops (FFs) in different hierarchical blocks into budgets for the different segments of the path that lie within different blocks. In practice, budgeting may result in the need for additional iterations of the synthesis and physical design flow, or may achieve suboptimal results in terms of area, power, or clock frequency. The proposed method makes the design process budgeting-free by moving the borders of the hierarchical blocks so that all borders of the hierarchical blocks are FFs. For a commercial 500MHz LSI with 141 million transistors, the design team required 2 months to archive the target frequency through try-and-try-again budgeting, while our budgeting-free method produced a design that meets the performance target within days.

Keywords: Hierarchical Design, Budgeting, Physical Synthesis

References
Variability Driven Gate Sizing for Binning Yield Optimization

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ABSTRACT
Process variations result in a considerable spread in the frequency of the fabricated chips. In high performance applications, those chips that fail to meet the nominal frequency after fabrication are either discarded or sold at a loss which is typically proportional to the degree of timing violation. The latter is called binning. In this paper we present a gate sizing-based algorithm that optimally minimizes the binning yield-loss. We make the following contributions: 1) prove the binning yield function to be convex, 2) do not make any assumptions about the sources of variability, and their distribution model, 3) we integrate our strategy with statistical timing analysis tools (STA), without making any assumptions about how STA is done, 4) if the objective is to optimize the traditional yield (and not binning yield) our approach can still optimize the same to a very large extent. Comparison of our approach with sensitivity-based approaches under fabrication variability shows an improvement of on average 72% in the binning yield-loss with an area overhead of an average 6%, while achieving a 2.69 times speedup under a stringent timing constraint. Moreover we show that a worstcase deterministic approach fails to generate a solution for certain delay constraints. We also show that optimizing the binning yield-loss minimizes the traditional yield-loss with a 61% improvement from a sensitivity-based approach.

Keywords: Gate Sizing, Process Variations, Speed Binning

REFERENCES
Elmore Model for Energy Estimation in RC Trees

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Abstract
This paper presents analysis methods for energy estimation in RC trees driven by time-varying voltage sources, e.g., buffers, time-varying power supplies, and resonant clock generators. An Elmore energy model that is the computational analog of the conventional Elmore delay model for RC trees is described. Simulation results indicate that the error in energy estimation is less than 2.5% in the worst-case in comparison to HSPICE simulations, with over a 1000X speed-up.

Keywords: Energy estimation, RC trees, interconnect.

References
Self-Calibration Technique for Reduction of Hold Failures in Low-Power Nano-scaled SRAM

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ABSTRACT
Increasing source voltage (Source-Biasing) is an efficient technique for reducing gate and sub-threshold leakage of SRAM arrays. However, due to process variation, a higher source voltage can significantly increase data flipping in standby mode (Hold Failures) resulting in faulty memories. This imposes serious concerns in reducing standby power with source-bias. In this paper, we analyze the effect of source bias on hold failures under both inter-die and intra-die variations. We propose a self-calibrating SRAM for aggressively reducing leakage while maintaining the hold failures under control.

Keywords: Adaptive source biasing, hold failures, low power SRAM

REFERENCES
**A Novel Variation-Aware Low-Power Keeper Architecture for Wide Fan-in Dynamic Gates**

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**ABSTRACT**

Substantial increase in leakage current and threshold voltage fluctuations are making design of robust wide fan-in dynamic gates a challenging task. Traditionally, a PMOS keeper transistor has been employed to compensate for leakage current of pull down (NMOS) network. However, to maintain acceptable noise margin level in sub-100 nm technologies, large PMOS is necessary, which results in substantial contention (during pull down) and severe loss of performance. In this paper, a novel keeper architecture is proposed which is capable of significantly reducing the contention and improving the performance and power consumption. Using circuit simulations, superior characteristics of the proposed keeper is demonstrated in comparison to those of the traditional as well as state-of-the-art keepers. It is shown that for an 8-input OR gate, in presence of 15% $V_{th}$ fluctuations, the proposed architecture can lead to 20%, 15%, and more than 40% reduction in power consumption, mean delay, and standard deviation of delay, respectively, when compared to traditional keeper circuit.

**Keywords:** Dynamic gates, process variation, keeper design, low-power design, reliability, robustness, VLSI.

**REFERENCES**


Standard Cell Library Optimization for Leakage Reduction

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Abstract
Scaling device geometries have caused leakage-power consumption to be one of the major challenges of deep sub-micron design and a major source for parametric yield loss. We propose a library optimization approach involving generation of additional variants for each cell master, by biasing gate-lengths of devices. We employ transistor-level gate-length assignment to exploit asymmetries in standard cell circuit topology as well slack distribution of the design. The enhanced library is used by a power optimizer to reduce design leakage without violating any timing constraints. Such transistor-level optimization of cell libraries offers significantly better leakage-delay tradeoff than simple cell-level biasing (CLB) proposed previously. Experimental results on benchmarks show transistor-level biasing (TLB) can improve the CLB leakage optimization results by 8-17%. There is a corresponding improvement in design leakage distribution as well.

Keywords: Gate-length biasing, Library optimization, Leakage reduction

References
ABSTRACT

In this paper, we propose an adaptive low-power bus encoding algorithm based on weighted code mapping (WCM) and the delayed bus technique. The WCM algorithm transforms an original bus data vector to a low-energy code through one-to-one mapping. The code mapping is determined by the data probabilistic distribution in the original sequence. The WCM algorithm considers both the self and coupling capacitance of the bus wires. In addition, we found that applying the delayed-bus technique can further reduce the bus energy. A window-based adaptive encoding algorithm is proposed to improve the energy saving by adaptively changing the code mapping when significant data changes are detected. Experimental results show that the proposed algorithm outperforms the existing heuristic bus encoding algorithms by 20~60% in energy dissipation.

Keywords: low power, bus encoding, adaptive algorithm, data probabilistic distribution, weighted code mapping, delayed bus, window based change detection

REFERENCES

A Thermally-Aware Performance Analysis of Vertically Integrated (3-D) Processor-Memory Hierarchy

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ABSTRACT
Three-dimensional (3-D) integrated circuits have emerged as promising candidates to overcome the interconnect bottlenecks of nanometer scale designs. While they offer several other advantages, it is expected that the benefits from this technology can potentially be offset by thermal considerations which impact chip performance and reliability. The work presented in this paper is the first attempt to study the performance benefits of 3-D technology under the influence of such thermal constraints. Using a processor-cache-memory system and carefully chosen applications encompassing different memory behaviors, the performance of 3-D architecture is compared with a conventional planar (2-D) design. It is found that the substantial increase in memory bus frequency and bus width contribute to a significant reduction in execution time with a 3-D design. It is also found that increasing the clock frequency translates into larger gains in system performance with 3-D designs than for planar 2-D designs in memory intensive applications. The thermal profile of the vertically stacked chip is generated taking into account the highly temperature sensitive leakage power dissipation. The maximum allowed operating frequency imposed by temperature constraint is shown to be lower for 3-D than for 2-D designs. In spite of these constraints, it is shown that the 3-D system registers large performance improvement for memory intensive applications.

Keywords: 3D ICs, processor-memory, performance modeling, thermal analysis, three dimensional, vertical integration, VLSI.

REFERENCES
Exploring Compromises among Timing, Power and Temperature in Three-Dimensional Integrated Circuits

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ABSTRACT
Three-dimensional integrated circuits (3DICs) have the potential to reduce interconnect lengths and improve digital system performance. However, heat removal is more difficult in 3DICs, and the higher temperatures increase delay and leakage power, potentially negating the performance improvement. Thermal vias can help to remove heat, but they create routing congestion, which also leads to longer interconnects. It is therefore very difficult to tell whether or not a particular system may benefit from 3D integration. In order to help understand this trade-off, physical design experiments were performed on a low-power and a high-performance design in an existing 3DIC technology. Each design was partitioned and routed with varying numbers of tiers and thermal-via densities. A thermal-analysis methodology is developed to predict the final performance. Results show that the lowest energy per operation and delay are achieved with 4 or 5 tiers. These results show a reduction in energy and delay of up to 27% and 20% compared to a traditional 2DIC approach. In addition, it is shown that thermal-vias offer no performance benefit for the low-power system and only marginal benefit for the high-performance system.

Keywords: 3DIC, temperature dependency, design flow, trade off

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ABSTRACT
The chip/package I/Os count has continuously been growing as the systems become more complicated. High density I/Os interconnection and efficient escape routing with high performance and low cost will greatly benefit the whole electronic system. We analyze the properties of the hexagonal array, which can hold about 15% more I/Os compared with the traditional square grid array. We propose three escape routing strategies for the hexagonal array: column-by-column horizontal escape routing, two-sided horizontal/vertical escape routing, and multi-direction hybrid channel escape routing. We can escape I/Os in the hexagonal array in the same or less number of routing layers compared with square grid array. The practical examples show the efficiency of our strategies. Using hexagonal array, we can reduce the number of escape routing layers as well as increase the density of I/Os.

Keywords: Escape routing, flip chip, BGA, hexagonal array.

REFERENCES
System Level Signal and Power Integrity Analysis Methodology for System-In-Package Applications

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ABSTRACT
This paper describes a methodology for performing system level signal and power integrity analyses of SiP-based systems. The paper briefly outlines some new modeling and simulation techniques that have been developed to enable the proposed methodology. Some results based on the application of this methodology on test systems are also presented. Categories and Subject Keywords: Causality, modal decomposition, nodal admittance matrix method, power integrity, signal integrity, System-In-Package (SiP), finite difference method.

REFERENCES
PELE: Pre-emphasis & Equalization Link Estimator to Address the Effects of Signal Integrity Limitations

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ABSTRACT
This paper discusses a methodology employed to create a tool that quantifies the effects of signal integrity limitations particularly for high-speed applications. The tool is based on a platform of routines which predict performance over high-speed links. It contains routines that optimize transmitter pre-emphasis and receiver equalization that lead to superior BER performance. The tool is qualified against Agilent’s ADS simulator and correlated to measurements.

Keywords: Analysis and optimization, signal integrity; layout; simulation beyond the die

REFERENCES
A Multilevel Technique for Robust and Efficient Extraction of Phase Macromodels of Digitally Controlled Oscillators

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ABSTRACT

PPV phase macromodels are important for speeding up simulation of oscillator related circuits, such as PLLs, without sacrificing accuracy. Prior numerical methods for extracting PPVs face very significant robustness and accuracy problems when confronted with digitally controlled oscillators (DCOs, core building blocks in digital phase-locked loops), due to large RC time-constants from gated capacitors. In this paper, we present a hierarchical harmonic balance based technique for numerically extracting the PPV of DCOs from their SPICE-level circuit descriptions. The proposed method applies hierarchical circuit partitioning and multi-level Newton methods to achieve dramatically superior convergence and PPV accuracy in the presence of large RC time-constants. We validate the method on a large DCO with many gated capacitors and demonstrate that it can extract the PPV efficiently and robustly, succeeding when prior methods fail. The method also provides speedups of an order of magnitude for large circuits, in addition to having significantly smaller memory requirements.

Keywords: Simulation, macromodel, VCO, DCO, PLL, DPLL, PPV

REFERENCES


ABSTRACT
This paper presents a systematic methodology for developing structural nonlinear macromodels for analog circuits. The methodology includes two steps: first, a nonlinear system is represented as a system with nonlinear inputs and linearly coupled blocks. Then, the linear couplings are removed. The methodology also uses a novel description of circuit nonlinearities as a successive composition of three operators. The generated nonlinear models are scalable, tunable according to the required accuracy, and offer insight into the circuit operation.

Keywords: Analog circuits, Structural macromodel, Nonlinear macromodel

REFERENCES
ABSTRACT
In this paper, we propose a novel envelope-following method which is uniformly applicable to both non-autonomous and oscillatory circuits. A key feature of our technique is the use of an efficient minimum least squares solution technique to solve an underdetermined envelope system directly. This leads to a general purpose approach which is much easier to solve than previous phase condition based envelope-following method, improving numerically robustness dramatically. We validate our method on a variety of autonomous and non-autonomous circuits, including a PLL in transition to lock. The new method provides speedups of 1-2 orders of magnitude over transient simulation, while obtaining results that are equally or more accurate.

Keywords: envelope following, least squares, phase condition

REFERENCES
ABSTRACT
Sigma-Delta ($\Sigma\Delta$) ADCs have been widely adopted in data conversion applications due to the good performance. However, oversampling and complex circuit behavior render the simulation of these designs prohibitively time consuming. In this paper, a lookup table (LUT) based modeling technique is presented for efficient analysis of $\Sigma\Delta$ ADCs. In the proposed approach, various transistor-level circuit nonidealities are systematically characterized at the buildingblock level and the complete ADC is simulated much more efficiently using these table models. As such, our approach can provide up to four orders of magnitude runtime speedup over SPICE-like simulators, hence significantly shortening the CPU time required for evaluating system performances such as SNDR (signal-noise-distortion-ratio). The proposed LUT modeling technique is further extended to assess performance variations due to parameter fluctuations. The resulting parameterized LUT modeling technique not only facilitates scalable performance variation analysis of complex $\Sigma\Delta$ ADC designs, but also allows us to feasibly extract statistical performance correlation models for low-cost test solutions.

Keywords: Sigma-Delta, Lookup table and statistical modeling.

REFERENCES
Clock Buffer and Wire Sizing Using Sequential Programming

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ABSTRACT
This paper investigates methods for clock skew minimization using buffer and wire sizing. First, a technique that significantly improves solution quality and stability of sequential programming-based buffer/wire sizing is used. Then, a new formulation of clock skew minimization that uses quadratic programming and considers sub-critical skews in addition to the most critical skews is presented. The quality of results are verified to be more robust using Monte Carlo simulations to account for process sensitivity. For the same power budget, the sequential quadratic programming (SQP) method has better expected skew, standard deviation, and overall CPU time on average.

Keywords: Clock tree synthesis, skew, robust design.

REFERENCES
Modeling and Minimization of PMOS NBTI Effect for Robust Nanometer Design

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ABSTRACT

Negative bias temperature instability (NBTI) has become the dominant reliability concern for nanoscale PMOS transistors. In this paper, a predictive model is developed for the degradation of NBTI in both static and dynamic operations. Model scalability and generality are comprehensively verified with experimental data over a wide range of process and bias conditions. By implementing the new model into SPICE for an industrial 90nm technology, key insights are obtained for the development of robust design solutions: (1) the most effective techniques to mitigate the NBTI degradation are VDD tuning, PMOS sizing, and reducing the duty cycle; (2) an optimal VDD exists to minimize the degradation of circuit performance; (3) tuning gate length or the switching frequency has little impact on the NBTI effect; (4) a new switching scenario is identified for worst case timing analysis during NBTI stress.

Keywords: NBTI, Reliability, Threshold Voltage, Temperature, Performance Degradation, Variability.

REFERENCES


A Parallel Low-Rank Multilevel Matrix Compression Algorithm for Parasitic Extraction of Electrically Large Structures

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ABSTRACT
Simulation of distributed electromagnetic effects of electrically large structures is no longer a luxury but a necessity in the accurate prediction of modern day circuit performance. In this regard, integral equation based methods have steadily gained in popularity but suffer from the time and memory bottlenecks arising from the resultant dense matrix. Fast linear complexity solvers have been introduced in the past but with the growing complexity of circuit layouts parallel implementations are the only viable options in addressing practical circuit layouts. In this paper, we present a parallel implementation of the low-rank compression based fast solver with linear cost reduction capacity with respect to the number of processors. The main problems in parallelizing a hierarchical algorithm are discussed and the advantages of the implemented scheme are highlighted. The new solver enables the simulation of full-chip problems consisting of millions of unknowns with acceptable accuracy and modest time and memory requirements.

Key Words: Parasitics, Parallel, MPI, Compression

REFERENCES
ABSTRACT
Reliability failure mechanisms, such as time dependent dielectric breakdown, electromigration, and thermal cycling have become a key concern in processor design. The traditional approach to reliability qualification assumes that the processor will operate at maximum performance continuously under worst case voltage and temperature conditions. However, the typical processor spends a very small fraction of its operational time at maximum voltage and temperature. In this paper, we show how this results in a reliability “slack” that can be leveraged to provide increased performance during periods of peak processor demand. We develop a novel, real time reliability model based on workload driven conditions. We then propose a new dynamic reliability management (DRM) scheme that results in 20-35% performance improvement during periods of peak computational demand while ensuring the required reliability lifetime.

Keywords: Dynamic Reliability Management, Modeling, Oxide Breakdown, Electromigration, Thermal Cycling

References
Chair: Joe Brandenburg - Consultant, Portland, OR
Panelists: Raul Camposano - Synopsys, Mountain View, CA
Mike Gianfagna - Aprio Technologies, Santa Clara, CA
Andrew Kahng - Blaze DFM, Sunnyvale, CA
Naeem Zafar - Pyxis Technology, Santa Clara, CA
Joe Sawicki - Mentor Graphics, Wilsonville, OR
Atul Sharan - Clear Shape Technologies, Sunnyvale, CA

ABSTRACT
How can design teams employ new tools and develop response methodologies yet still stay within design budgets? How much effort does it require to be an early adopter and what kind of measurable results compensate for this effort? Panelists discuss how their design-for-manufacture (DFM) tools fit into a fixed design methodology, budget and timeline, and give examples of expected ROI (monetary, quality, reduced time-to-market, and comprehensive yield).

The aim of this panel is to provide a serious comparison of related DFM technologies on the market and some idea of the cost and difficulty of integrating the tools into a fixed design budget and timeline. Specific results will be cited, along with examples of expected ROI (monetary, quality, reduced time-to-market, and comprehensive yield enhancement).

The audience should walk away with enough information to make an informed decision on which companies would make sense for their DFM challenges, to reach their own yield and throughput goals.

Keywords: Design for manufacture, DFM, Design for yield, ROI, RET, OPC, Yield optimization
Early Cutpoint Insertion for High-Level Software vs. RTL
Formal Combinational Equivalence Verification

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ABSTRACT
Ever-growing complexity is forcing design to move above RTL. For example, golden functional models are being written as clearly as possible in software and not optimized or intended for synthesis. Thus, equivalence verification between the high-level software functional model and the RTL is needed. The typical approach is to convert the high-level software into RTL or gate-level hardware, via software path enumeration, symbolic execution, or highlevel synthesis techniques, and then use hardware combinational equivalence checking. The principle contribution of this paper is to introduce cutpoints — as in gate-level combinational equivalence verification — early during the analysis of the software model, thereby avoiding exponential path enumeration and the potential logical complexity blow-up of merging execution paths that can occur in the usual approach. The method is conservative, but in our experiments, we did not encounter spurious counterexamples, and the method showed large improvements in runtime and memory usage on a family of IA-32 subset instruction length decoders, an industry-suggested challenge problem.

Keywords: software, RTL, formal equivalence checking, cutpoints

REFERENCES
ABSTRACT
This paper discusses the use of transistor abstraction to enable the functional verification of FPGA fabrics with RTL models. It first describes the multiplexer structures that are used on a massive scale in FPGAs and the specific challenges that they pose to transistor abstraction tools. It then reviews previous approaches and shows that the cone model of the DESB system is particularly well suited to abstract FPGA logic because it makes pass-gate branches in multiplexer structures well apparent. Based on this model, methods are described to isolate multiplexer structures, take into account logic correlation between signals, and generate RTL models that are both simulation efficient and highly readable. Finally, Altera’s ABX tool that implements these concepts is briefly described.

Keywords: Cone model, FPGA, functional verification, logic equivalence checking, multiplexer, Register Transfer Level, transistor abstraction.

REFERENCES
Automatic Invariant Strengthening to Prove Properties in Bounded Model Checking

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Abstract
In this paper, we present a method that helps improve the performance of Bounded Model Checking by automatically strengthening invariants so that the termination proof may be obtained by analyzing shorter paths. The strengthening technique identifies sets of states as byproducts of the termination checks. It then uses SAT-based preimage computations to extend those sets. Our approach may substantially speed up the verification of both failing and passing properties. We present experimental results showing that our new method improves the performance of BMC significantly.

Keywords: Bounded Model Checking, SAT

References
Fast Falsification Based on Symbolic Bounded Property Checking

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Thomas Kropf and Wolfgang Rosenstiel
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ABSTRACT
Symbolic property verification is an increasingly popular debugging method based on Binary Decision Diagrams (BDDs). The lack of optimization of the state space search is often responsible for the excessive growth of the BDDs. In this paper we present an accelerated symbolic property verification by means of a new guiding technique that automatically finds the set of interesting variables by exploiting the property and the transition relation of a design. Our property based state space guiding can substantially speed up the verification process. The heuristic picks up the interesting state or the input variables automatically and utilizes them in guiding the state space traversal. This guiding approach is a novel one as it is automatic, efficient and stable for fast falsification. Furthermore it does not degrade as much for full validation.

Keywords: Property Checking, Fast Falsification, Guiding.

REFERENCES


Unknown-Tolerance Analysis and Test-Quality Control for Test Response Compaction using Space Compactors

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ABSTRACT
For a space compactor, degradation of fault detection capability caused by the masking effects from unknown values is much more serious than that caused by error masking (i.e. aliasing). In this paper, we first propose a mathematical framework to estimate the percentage of observable responses under unknown-induced masking for a space compactor. We further develop a prediction scheme which can correlate the percentage of observable responses with the modeled-fault coverage and with a n-detection metric for a given test set. As a result, the quality of a space compactor can be measured directly based on its test quality, instead of based on indirect metrics such as the number of tolerated unknowns or the aliasing probability. With the prediction scheme above, we propose a construction flow for space compactors to achieve the desired level of test quality while maximizing the compaction ratio.

Keywords: Test response compaction, design for test

REFERENCES

ABSTRACT
The paper presents an efficient method for synthesis of scan chain selection logic. It is capable of
acting as a flexible X-control logic for test response compactors. The same circuitry can also be
employed to selectively gate scan chains for diagnostic purposes.

Keywords: Compression, scan chain selection, unknown states, VLSI test.

REFERENCES
Fault Detection and Diagnosis with Parity Trees for Space Compaction of Test Responses

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ABSTRACT
This paper shows that accurate fault detection and diagnosis are possible when applying a parity tree for space compaction of test responses and continuously observing the parity-tree output. We exploit that each set of faults results in a unique parity-tree output sequence that can be used as a unique fault signature for truly accurate fault detection and diagnosis. Our theoretical analysis shows that probabilities for fault cancellation and fault aliasing are extremely low and decrease with circuit size. Experimental results show that for a typical scan chain architecture in large industrial circuits, fault coverage is not affected by parity-tree space compaction for up to 256 scan chains, while diagnostic resolution is reduced by only 1% to 2%.

Keywords: Test data compression, fault detection, fault diagnosis.

REFERENCES
Multiple-Detect ATPG Based on Physical Neighborhoods

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ABSTRACT
Multiple-detect test sets detect single stuck line faults multiple times, and thus have a higher probability of detecting complex defects. But current definitions of what constitutes a new test for a single stuck line fault do not leverage defect locality. Recent work has proposed a new metric to capture quality of a multiple-detect test set based on the number of unique states on lines in the physical neighborhood of a targeted line. This paper presents a new ATPG strategy that uses this metric to generate higher quality multiple-detect test sets.

Keywords: Multiple-Detect, N-detect, neighborhoods, ATPG, defects

REFERENCES
ABSTRACT
Floorplanning algorithms have traditionally underperformed experienced designers, even when relatively simple interconnect metrics are concerned. However, the sheer scale of modern systems on chip makes an all-manual design flow infeasible. In this paper, we propose a new efficient automated approach to the floorplan repair problem, where a set of violated design constraints are satisfied by applying small changes to an existing rough floorplan. Such a floorplan can be produced by a human designer, by a scalable placement algorithm, or result from engineering adjustments to a pre-existing floorplan. In all cases, overlapping modules must be separated, and in some instances, modules may need to be repositioned to satisfy other requirements.

The algorithmic framework we propose is built upon an expressive graph-based encoding of constraints. While capable of representing floorplans with or without overlapping modules, it can also support the outline of the core area, fixed module locations, region constraints, proximity and alignment constraints, etc. Instead of applying randomized local search in the hope of satisfying these constraints, we track all implications of imposed constraints and resolve violations by invoking gradual modifications to the floorplan.

The primary focus of this paper is on a particularly efficient conflict-directed algorithm for floorplan repair and legalization. It is shown to completely eliminate overlaps from layouts produced by Capo 9.4, Feng Shui 5.1 and APlace 2.01 on IBM-HB benchmarks with hard blocks, typically requiring negligible runtime and increasing interconnect length by only several percent. Furthermore, we are able to generate legal solutions for these instances that surpass previously reported results in wirelength by an average of roughly 7%.

Keywords: Floorplanning, Legalization, Constraints

REFERENCES


ABSTRACT

In a placed circuit, there are a lot of movable cells that can be flipped to further reduce the total wirelength, without affecting the original placement solution. We aim at solving this flipping problem optimally. However, solving such a problem optimally is non-trivial given the gigantic sizes of modern circuits. We are able to identify a large portion of cells (about 75%) of which the orientation (flipped or not flipped) can be determined independent of the orientations of all the other cells. We have derived three non-trivial conditions to identify those so called independent cells, strictly solvable cells and conditionally solvable cells. In this way, we can greatly reduce the number of cells whose orientations are dependent on each other. Finally, the cell flipping problem of the remaining dependent cells can be formulated as a Mixed Integer Linear Programming (MILP) problem and solved optimally. However, this may still be too slow for extremely large circuits and we have applied two other methods, Linear Programming (LP) and Linear Programming followed by Mixed Integer Linear Programming (LP+MILP) to solve the problem. Experimental results show that by identifying those independent and solvable cells first and applying the LP+MILP technique, we can solve this flipping problem effectively and obtain results just 0.01% more than the optimal. In addition, we can improve the wirelength and number of overflow tiles by 5% and 9% respectively on the floorplanning benchmarks.

Keywords: Floorplanning, Placement, Wirelength, Orientation, Flipping

REFERENCES

A New LP Based Incremental Timing Driven Placement for High Performance Designs

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ABSTRACT
In this paper, we propose a new linear programming based timing driven placement framework for high performance designs. Our LP framework is mainly net-based, but it takes advantage of the path-based delay sensitivity with limited-stage slew propagation, thus it enjoys certain hybrid feature of net and path-based timing driven placement. Our LP formulation considers not only cells on the critical paths, but also cells that are logically adjacent to the critical paths (i.e., the criticality ad jacency network) in a unified manner. We further present a timing aware spreading method to preserve timing in legalization for high performance designs. Our algorithm has been tested on a set of 65nm industry circuits from a multi-GHz microprocessor, and shown to achieve much improved timing on hand-tuned circuits.

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