DAC74, pages 1 - 13

Philosophic Comments on Data Base Context and Management in Design Automation

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The word "context" in the title is chosen quite specifically. In design automation the data base structure and organization are relevant but not of primary concern: rather, the content of a data base and its interaction with various processes are of greater importance. It might appear that the word "environment" is more appropriate in this context, but this is true only if it is further qualified. Therefore, I have chosen to use the word "context", since where a design automation data base is utilized it should explain its own meaning by virtue of being there; otherwise, it is not performing the function for which it was designed…

DAC74, pages 14-18

CRITIC: An Integrated Circuit Design Rule Checking Program

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INTRODUCTION

The ever growing complexity of integrated circuits has motivated the development of CAD programs to help pinpoint potential errors in the IC artwork. This has become extremely important because of the large loss of time and money which occurs when an artwork error is found after an IC is manufactured. More subtle and perhaps even more serious is an undetected non-catastrophic violation of a design rule that reduces IC manufacturing yield and therefore needlessly increases cost over a long period of time.

A computer-aided approach is quite natural for this application because of the huge amount of tedious work involved in IC artwork checking by human eye and the relative geometrical simplicity of most design rule checks. Experience has proven that even the most careful checking of artwork by eye misses many potential errors.

A design rule checking program called CRITIC (Computer Recognition of Illegal Technology in Integrated Circuits) has been in active production use at RCA for over two years, particularly for COS/MOS, PMOS and SOS ICs and also for high speed bipolar IC development. It is capable of checking design rules involving such geometrical properties of figures as minimum width and interrelationships such as minimum clearance, minimum enclosure and one figure inside another. It can perform these checks for figures on any number of single mask levels or between figures on different mask levels. It should be pointed out that the program is general and could also be applied to technologies other than Integrated Circuits, such as printed circuit boards…

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DAC74, pages 19-25

Master Slice LSI Computer Aided Design System

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ABSTRACT

This paper presents a Computer Aided Design (CAD) system which is intended for practical use in master-slice LSI design and testing. This system includes five sub-systems; PLACEMENT, ROUTING, IMPROVE, ARTWORK, and TEST GENERATION.

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DAC74, pages 26-46

Advanced LILAC - An Automated Layout Generation System for MOS/LSIs

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Introduction

The demand for large scale integrated circuits (LSIs) having more than twenty thousand gates per chip is increasing year by year. To reduce the time necessary for designing LSIs many kinds of systems have been developed and introduced. [2][3][4][5][6][7][8] Since the time required for the chip layout during the development of MOS/LSIs take up more than half of total design time, a sophisticated CAD system is urgently needed. In the layout design of MOS/LSIs the CAD system for Aids to manual design is not a sufficient design tool. There are two categories of configurations in IC layout CAD; 1) Interactive Graphic CAD [1][2], 2) Batch Processing system. The system including automatic design procedures often uses large computers under the batch processing system.

Several papers reported automated placement and routing of a chip layout. These involved either individual programs, i.e. Partitioning [3][4], Placement [5], Wire Routing [6][7], or total systems [8]. The object of programs was restricted to polycell layout.

Recently, logic circuits have overcome restrictions of the polycell approach, and generally contain new devices -- PLA(Programmable Logic Arrays) [9], ROM(Read Only Memory), or SR(Shift Register). In the CAD system with restricted polycell layout, it is impossible to design the chip layout of an LSI -- containing large functional blocks like PLAs.

This paper describes the layout model and algorithm applied to an advanced LILAC system which is capable of automatically designing MOS/LSI chip layouts containing PLAs. The system, which is a fully automated design system, inputs logic description and outputs layout drawing. No intervention is needed. The system configulation is shown in Figure 1. The main features of the system are: 1) generation of logic file, 2) partitioning (to generate groups of elements consisting of blocks), 3) determination of the number and location of the external wiring area which is the interconnection channel between blocks, 4) assignment of the external wiring to the each area, 5) cell placement, 6) terminal assignment of the cell, 7) routing in a block, 8) routing of the external wiring area, 9) output of data for XY plotter to magnetic tape…

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DAC74, pages 47-51

Computer-Aided Process Design and Simulation for Forging of Turbine Blades

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ABSTRACT

Turbine and compressor blades for jet engines and gas turbines are forged from high-strength alloys and require close control of the process parameters. The design and manufacture of the dies require particular attention, for they impart their geometry to the final product. For precision forging, the die surface must be corrected for local elastic deflections and thermal shrinkage.

Considering turbine blades as a geometric family, a system of programs was developed to aid in forging process design. Given data on the configuration of the blade, the material properties and the forging conditions, this system of programs calculates (a) the optimum forging plane to minimize lateral forces, (b) the required stock volume and weight, (c) the forging load and the torque on the dies, (d) the optimum flash dimensions for uniform metal flow, (e) the average temperature of the blade during forging and (f) the local stresses and elastic deflections during forging. A simulation of the process aids in preform design and in minimization of flash losses by determining the proper position of the preform in the die.

This system of programs requires the ability to visualize the forging die to facilitate the design process. Computer graphics has been used in two phases to aid this visualization; first, in the design of the dies using the system and second, in explaining its capabilities to others.

The first phase relies on the use of interactive graphics techniques to provide information about the die, which includes representations of (a) the preform determined by the programs, (b) the cutter paths necessary to cut the part, and (c) the die itself. Interactive graphics allows the user to make decisions and modify his design rapidly.

The second phase uses motion picture techniques to present the findings of this project. Computer animation has been added to conventional techniques to help audiences conceptualize the forging process. The animation allows the audience to view the process in slow motion by illustrating metal flow behavior and the variations of die stresses during forging. This technique has proved to be successful in demonstrating the capabilities of the system to a wide range of audiences.

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DAC74, pages 52-61

Metasystem: A Hierarchically Structured Graphic Tool

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INTRODUCTION

This paper describes a first system for generating programmed systems for computer aided fabric design. Two aspects of the system are explored. First the design strategy which led to the construction of a mechanism to provide for a variety of design tools is explained. The hierarchical structure of the system as well as the nature of its modules are detailed. Second the facilities available in the system are presented. The designing systems produced by this higher level system incorporate features of our previous systems such as display and modification of the design on a graphic unit. In addition three new functions are available in the system. The first is a tool which allows the artist to introduce his design concepts directly into the system in a manner that is most natural to him. The second new facility provides the point paper designer with a means of tracing a design into the system on an electronic tablet and simultaneously viewing it gridded, according to a specified gauge, on the screen. The third function assists the point paper designer develop his design into repeat by reinspecting the elements of his gridded design whether it was traced or optically scanned. As a result of this reinspection, areas of the design are now identified and may be enlarged, reduced, moved or erased from the design.

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DAC74, pages 62-69

An Integer Arithmetic Path Expansion Algorithm

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ABSTRACT

Graphical display systems are often built around a minicomputer with limited word size, core, and instruction repertoire. Thus, plotting algorithms which do not need floating point software or hardware are particularly valuable. Since the usual (CRT) graphical display has limited resolution, the typical floating point evaluations of square roots and transcendental functions are often unnecessarily accurate.

Extending the integer arithmetic functional plotting concepts, integer algorithms are presented for the calculation of Euclidean distance, plotting of lines perpendicular and parallel to a given line segment, and the calculations of the intersection of two (slant) lines, all to an accuracy of one screen unit. These algorithms are combined into an algorithm to plot the outline of a path expanded from a centerline of straightline segments, with unrestricted orientations.

The algorithms have been implemented on a PDP-8 minicomputer with a Tektronics 611 storage scope. They are routinely used to display integrated circuit mask descriptions.

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DAC74, pages 70-81

An Interactive Man-Machine Approach to the Computer Logic Partitioning Problem

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ABSTRACT

The problem of partitioning computer logic has been attacked in the past by manual and automatic techniques. We describe an interactive approach which combines aspects of both approaches and creates results which are better than those obtainable by either approach independently. An overview of the system is presented, several algorithms discussed and experimental results are given.

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DAC74, pages 82-90

An Improved Graph-Theoretic Model for the Circuit Layout Problem

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Abstract

The use of topological methods for the circuit layout problem is surveyed first. In the second part an improved model is proposed, which allows pin and gate assignment in function of the layout.
Keywords: design automation, computer-aided design, integrated circuit layout, printed circuit board design

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A Partitioning Technique For LSI Chips Including a Bunching Algorithm

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This paper discusses a partitioning technique which initially orders circuits according to a scoring mechanism, and thus uses a two-stage interchange technique to arrive at a final partition.

Paper not received in time for publication

DAC74, pages 92-97

A Simple Computer-Aided Artwork System that Works

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INTRODUCTION

The need for computer assistance in handling artwork for various industrial processes has spawned a number of different systems designed to input, edit and prepare artwork with varying degrees of human interaction during the process. The system described here for processing integrated circuit artwork was begun when there were fewer commercial systems available than there are now. In the intervening five years this system has matured such that the Solid State Division of RCA uses it in the production of its COS/MOS circuits, as well as for many of the other solid state devices it manufactures…

DAC74, pages 98-106

Automated Inspection of Electronic Assemblies

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ABSTRACT

Automated Visual Inspection Systems for electronic assemblies have been investigated. Three major phases have been researched: scanning devices, software algorithms, and possible computer systems.

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DDAC74, pages 107-118

Map: A User-Controlled Automated Mask Analysis Program

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ABSTRACT
The Mask Analysis Program is a totally general and application independent FORTRAN program for the analysis and manipulation of graphic data. It is particularly useful in integrated circuit design analysis.

DAC74, pages 119-126

Automated Design and Manufacture of Printed Circuit Boards

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ABSTRACT

This paper presents a case history of an automated design, documentation, assembly, and testing system for printed circuit boards. Included are the merits, pitfalls, and economics of such a system.

DAC74, pages 127-136

A Simple, Efficient Design Automation Processor

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Introduction

This paper describes a design automation processor which was developed as a design, pedagogical, and research tool at Vanderbilt University. The processor was intended to provide a design aid for the development of small scale switching systems (e.g., controllers, interfaces, etc.). These designs were intended to be realized using TTL logic and TI #18763 wire-wrap boards. While the initial implementation was limited to this technology, flexibility for growth was included in the system design. In addition, although the system is primarily designed for wire-wrapped technology, a wire router is included to provide a printed circuit capability…

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DAC74, pages 137-142

Microprogramming Design Support System

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INTRODUCTION

Recently microprogramming technique has been used in many areas such as computers, peripheral devices, terminals, and so on. Control word organization varies with each control equipment. Also integrated control technique or centralized control technique requires the integration of microprograms depending on system configuration. Therefore generalized and sophisticated design support system has been desired. Microprogramming Design support System, MDS, has been developed to meet such requirements…

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DAC74, pages 143-148

Computer Aided Schematics

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ABSTRACT

The paper presents an example of how a computer aided system has aided in the generation of publications in a shorter time frame and at a 33 percent cost savings. A program which produces schematics is examined in detail.

DAC74, pages 149-158

Automatic Test-Generation and Test-Verification of Digital Systems

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ABSTRACT

The widespread use of large scale and medium scale integrated circuits, coupled with the trend towards larger boards, made manual generation of test patterns very expensive, somewhat ineffective, and rather difficult to update for design changes. The advent of MOS LSI's with extremely large gate density made manual test-verification, the process of finding failures detected by a given test pattern, an impossibility. Therefore, a series of programs was developed, over the years, to completely automate the test cycle -- using logic description files as input, the final output for test generation is a test deck compiled in the language of card test equipment and, in the case of test-verification, lists of detected and undetected failures. All this is accomplished within the global constraint of complete (nearly 100%) coverage and prevailing test floor practices.

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DAC74, pages 159-165

MSI and LSI Impact on Digital Systems Testing

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INTRODUCTION

Basically, there are two approaches to testing digital networks, namely, functional and structural. [1] There are few available publications dealing with functional testing methods. This is due mainly to the lack of a universal algorithm for testing networks that function differently. Moreover, functional testing usually does not yield a complete test of a given network, therefore it does not have as much academic value as structural testing…

In this paper a few functional testing techniques are briefly described. They are heuristic methods used in the computer industry mainly for trouble-shooting purposes. Structural testing has recently been summarized by Professor Susskind [1]. It is the purpose of this paper to show recent testing techniques and to indicate the need for inclusion of self-testing capabilities to chips during the fabrication process.

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DAC74, pages 166-168

A System of Computer Programs for Efficient Test Generation for Combinational Switching Circuits

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Abstract

Modules of computer programs for test generation, fault simulation and test minimization for combinational switching circuits have been written. They form a system of computer programs in which a special strategy directs the choice of a test set. The object is to minimize the number of tests which is required for the detection of logical faults in combinational switching circuits.

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DAC74, pages 169-176

A New Heuristic Test Generation Algorithm for Sequential Circuits

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Abstract

This paper describes a new heuristic algorithm for the computation of tests to detect failures in sequential logic circuits. In the algorithm, the values of logic blocks in a logic circuit are expressed in boolean vectors with six elements and main process of the algorithm is the operations among these values. Presented in this paper are basic principles for the algorithm, their application procedure with an example and our experiences through the implemented system.

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DAC74, pages 177-185

A Programmable Configurator

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ABSTRACT

This paper discusses a system for programmatic processing of data processing equipment orders. Major tasks performed include analysis of the marketing order for completeness, determination of the required equipment configuration, and parts selection based upon the determined configuration. The key feature is that a single program is able to handle any data processing order within the Burroughs product line. This program is driven by "rules" disk files which are maintained independently through the use of a high level language.

DAC74, pages 186-193

Speculation on the Future of Design Automation

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ABSTRACT

The future direction of the use of design automation for designing and developing digital data processing systems and hardware is highlighted. Some of the unsolved problems in design automation are indicated.

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DAC74, pages 194-199

An Experimental Comparison of Force Directed Placement Techniques

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ABSTRACT

Force-directed placement algorithms are experimentally compared using several sample problems. Significant differences are noted in the computational efficiency of the algorithms, and in the relationship of the placement solution to the routability of the resulting board.

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DAC74, pages 200-208

A Tool for Computer Design

Helmut Weber

FOOTNOTE: This is a translation from German of a presentation at the Symposium on "Computer Structures" Sept. 73 at Wildbad, Germany. The papers presented at Wildbad have been published in German in a book "Rechnerstrukturen" by R. Oldenburg, Munchen 1974.

Summary
Computers are designed in stages. After the architectural definition of the system a block diagram is developed. From this the detail logic and the microprogram is developed in several steps, and the logic structure is mapped to a physical structure.

This process consist essentially of transformations and expansions under constraints, leaving the desired function of the system being developed invariant.

This paper analyzes the development process critically and covers methods with which the invariance of the function of the systems can be guaranteed…

DAC74, pages 209-219

Transmission Line Models for Transient Analysis

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Introduction

Digital signals in some high speed computers and communication systems are required to have rise and fall times below 5 nanoseconds and pulse widths less than 100 nanoseconds. Designers who design systems which operate with short rise and fall times and narrow pulse widths face the problem that circuit paths whether they are twisted pair cables, printed circuit paths, striplines, microstrip lines, or another realization propagate signals as transmission lines. They have faced the problem that transmission lines introduce when they are not properly terminated or when the transient delay of the line is not included in the overall system time delay. Furthermore, the design of signal distribution circuits has been accomplished without adequate analytical support.

The analysis problem is more difficult. Obtaining a transient solution for a signal distribution circuit that is realized as an interconnection of transmission lines requires an effective transmission line model. Such a model could be used with a circuit analysis program such as SCEPTRE [1] to obtain a transient solution.

An approximation of a transmission by a ladder network with a few series RL and shunt RC sections is inaccurate. The accuracy of the approximation can be improved by subdividing the line into more sections at the expense of computing time required for a solution.

A method of incorporating a model of any two-conductor transmission line into a SCEPTRE transient analysis problem is described in this paper. This model is obtained by breaking the transient response of the transmission line into two components: the time-delay component and the waveshape component. The time-delay component is obtained with a subprogram that stores the signal generated at one end of the transmission line and introduces that signal at the other end after a time delay. The waveshape component is approximated with the response of an RLC circuit…

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DAC74, pages 220-228

A Combinatorial Programming Approach to the Joint Optimization of Land Use and Transportation

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INTRODUCTION

So far, mathematical models used in urban planning were descriptive or predictive. It is the purpose of this paper to describe a planning model, i.e. a model whose purpose is to produce a plan rather than to predict the consequences of a given plan. It produces a land use plan as well as a transportation plan and takes into account the interactions between land use and transportation…

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DAC74, pages 229-236

A Procedure for Generating Floor Plans Computer Aided Design

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ABSTRACT

The following study concerns itself with the generation of rough ideas of floor plans in a relatively short time and low cost. A methodical procedure is sought in the form of a computer program which may subsequently be used by someone unskilled on an interactive basis that will help the designer and his client gain an understanding of the layout.

The idea of user generated design is the foundation of this work. Client's values of required proxemic distances are translated into a spatial layout, in the form of dimensioned map, with great ease. Preference values are first used to build a polyomino reflecting the order of importance given to each pair-wise distances between cells.

The technique that transforms a set of proxemic distances generated by the client into a spatial layout (a polyomino) and which in turn was thought to be the minimum of absolute differences in the summation of distances between the pattern generated and a given set of preferences was first introduced by R. S. Frew in, "Towards a Theory of System Architecture" University of Waterloo, Canada.

The means of finding the order of links from the highest to lowest priority was retained but a new procedure has been developed to build patterns (polyominoes), the effectiveness of each judged under the same criteria stated above.

The present study, then, introduced a new procedure for pattern construction and in addition worked out and coded a procedure for the conversion of a polyomino into a dimensional map in which each of the elements can be of different proportion or size.

DAC74, pages 237-247

A Computer Aided Land Use Study Technique

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Abstract

This paper describes a computer-aided, decision-making technique by which the suitability of any site or area may be evaluated with respect to any type of usage or development. The method described provides the designer with the means for making judgments as to locational desirability even with limited data availability. The procedure also raises the level of decision parameter selection above the "local" level to include "universal" or "global" inter-relationships. The means for utilizing macro-level data and information to make micro-level decision is demonstrated. An actual case study for housing site suitability near Chicago is presented to illustrate the approach. The merits of the technique over previous approaches and the problem of designer "judgment" in computer-aided methods is also discussed.

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DAC74, pages 248-256

Interaction, Interfaces and Design

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INTRODUCTION

Many planning problems cannot be formulated in such a manner that a well developed optimizing technique can be applied to them to arrive at a satisfactory solution. This may be because of the structure of the problem itself, it may be because objectives and even parameters cannot be adequately described or it may be due to the need to include subjective factors. Additionally there is a class of problems for which the cost of the computation required to reach an optimum is not warranted by the expected gains…

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Department of Architectural Science, University of Sydney, Computer Report CR22, 1973.

A Minicomputer-Based Logic-Fault Simulator

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Introduction

A unit-gate-delay three-valued-logic parallel fault simulator handles up to 1500 gates on a minicomputer with 16K core. Capabilities, programming novelties, and performance statistics will be presented.

Paper not received in time for publication.

DAC74, pages 258-265

Functional Testing of LSI Gate Arrays

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Introduction

This is a report on the testing of LSI gate arrays. A large number of combinational and sequential digital networks were tested using the traditional s-a-1, s-a-0 fault model. These random logic functions were implemented with LSI gate array devices. This report describes the environment within which these devices were tested and the testing results. Also, some problems encountered in testing these devices and solutions to these problems are summarized…

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DAC74, pages 266-272

Timing Analysis for Digital Simulation using Assignable Delays

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Abstract

The techniques to be described in this paper are generally applicable to any time domain, parallel fault, digital logic simulation system. The particular implementation was done on the CC-TEGAS3 system and quoted results are from this system.

The first technique to be considered provides accuracy of fault simulation when using assignable nominal delays for different element types. The second technique provides for handling fault induced activity in a network, in such a way as to considerably reduce the amount of simulation time required.

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DAC74, pages 273-278

A Computer Aided System (CAS) for the Design, Manufacture, Test, and Documentation of Digital Printed Circuit Boards

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ABSTRACT

This paper is an overview of a complete set of software packages for the design, manufacture, test and documentation of Digital Printed Circuit Boards.

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DA74, pages 279-283

Computer Aided Ship Design at MarAd

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Introduction

The preliminary ship design process is a natural for design automation as it involves an iterative series of calculations based upon a data base which describes the hull shape. Figure 1 illustrates the spiralling nature of the design verification from basic requirements of the ship to final design and indicates the sequential nature of the calculations…

DAC74, pages 284-299

RTL The Firmware Design Automation System

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INTRODUCTION

The development of firmware controlled devices poses several new requirements on Design Automation. Because firmware is central to system design and reflects heavily on system speed and cost, the basic assembly parameters change ofter during the early design phases. It is necessary to have an automation system which is able to react to design changes without reprogramming of system components. Thus the standard approach of simulating firmware with a special purpose language and a special purpose assembler or assembler/simulator is no longer practical. This paper discusses a general solution to the several requirements of firmware design.

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DAC74, pages 300-307

Automated Sign Design and Stencil Cutting System

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Abstract

The automation of artistic art form provided a real challenge in terms of new software and hardware design for a computer system. The complete system has been in operation daily since July 1972 and provides the necessary features to design and produce stencil art work for sign making.

DAC74, pages 308-313

An Iterative Technique for Printed Wire Routing

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Abstract

Wires are routed allowing crossings in the initial layout. By spreading the wires and increasing the crossover penalties, fewer crossings occur on each iteration until a crossing free layout is achieved.

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A Programmable Printed-Wiring Router

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ABSTRACT

This paper discusses BAAR, a program to route conductor paths on printed-wiring boards. It is based upon the Moore-Lee algorithm [1][2] and incorporates an effective path-cost function and a programmability feature. It is written in ALGOL for the Burroughs B6700 and is producing results which are very good in both of two respects: the quality of individual paths is comparable to what a human would produce, and completion rates are very high.

The particular path-cost function used is inherently capable of yielding much better paths than a simple Manhattan-distance function, but the principal advantage of the program lies in the feature whereby a user may design a routing strategy for a particular board topography and then "program" the router to execute that strategy. The result is an algorithm which is remarkably simple, without the usual host of preprocessors, postprocessors, and special-case routines, while at the same time constituting a tool of considerable power and flexibility.

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DAC74, pages 322-326

A System for Multilayer Printed Wiring Layout

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INTRODUCTION

The task of routing large multilayer printed wiring boards (most commonly back-planes) is a tedious, time-consuming and error-prone procedure if done manually. The size and general uniformity of the board plus the large number of connections makes the probability of error very high.

Ideally boards like this would be done by automatic routing programs. In practice, however, a number of reasons often make this impossible.

i) The physical design of the board does not lend itself to the programs.

ii) All or a large part of the connections to be made must comply with some specific rules which would be extremely difficult to communicate to a program.

Additionally, automatic routers frequently fail to make all the required connections. It is often advantageous to complete the job with manual editing and additions.

To aid this process, an interactive graphics system has been built. Because of the specialized nature of the problem, it was both necessary and possible to build the program in such a way as to allow the interactive graphics terminal to be a true design station instead of just an efficient data capture station.

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The IPAD System: A Future Management/Engineering/Design Environment

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The results of a feasibility study on an "Integrated Programs for Aerospace Vehicle Design (IPAD) System" are presented, along with details of its usage philosophy, its organization, and a preview of the future design environment offered by such a system. The results of the study show that an IPAD System is feasible within four years from go-ahead, it can be implemented in all major host computers, and provides a user-oriented computer environment applicable to many aerospace and nonaerospace engineering and scientific fields.

Two independent and parallel feasibility studies were funded by the NASA Langley Research Center, from March 1972 to August 1973, to define an IPAD System and its implementation schedule. This paper summarizes the IPAD System design approach generated by the General Dynamics Corporation and does not purport to be NASA's final views for IPAD.

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Feasibility Study of an Integrated Program for Aerospace Vehicle Design (IPAD)

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INTRODUCTION

The basic goal of the IPAD system is to increase the productivity of the product design organization. This IPAD study showed increases in individual productivity are feasible through automation and computer support of routine information handling. Such automation can directly decrease cost and flowtime in the product design process…

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DAC74, pages 347-351

Design Automation in Preliminary Design

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INTRODUCTION

This paper will explore the role of design automation in the preliminary design process. For this purpose, design automation is considered as the use of computer programs in the analysis and synthesis of a tactical weapon system. The weapon system consists of all the elements required to deliver a warhead onto an unfriendly target. The design process is considered and the role of computer programs is defined. From these studies the requirements for design automation are obtained, and the value of design automation is assessed.

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DAC74, pages 352-358

Germinal: Towards a General and Integrated System for Computer Aided Design

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In 1969 a symposium involving CAD took place in Davenport -USA-. We quote from the report [1]: "we felt that the confusion regarding the definition of the term "CAD" was, in itself, a characterization of the state-of-the-art". Four years later a certain confusion still remains. This is an evidence of the fact that the field of computer-aided design is still largely unexplored…

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DAC74, pages 359-365

Using Simulation to Evaluate System Performance

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Abstract

This paper presents some recent results obtained from using simulation to evaluate computer system performance when alternative job priority assignment algorithms are considered. Performance data are given for both individual computing centers and network computers (FOOTNOTE: We define a computing center to be either a single processor or a geographically local but independent group of interconnected processors. We define a network computer to be any interconnected group of computing centers. (Thus, a multiprocessor computing center is a local network computer.) We use the term network computer as opposed to computer network to avoid confusion with the logic networks used in computers and because the analysis of electrical networks by computers is commonly referred to as "computer network analysis."). A "pay-for priority" scheduling algorithm for the individual centers is explored and load leveling techniques for transmitting jobs between centers are evaluated. The effects of these algorithms on system performance are demonstrated through the use of a simulation model.

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DAC74, pages 366-371

Initial Design Concepts for an Advanced Design Automation System

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ABSTRACT

Most design automation systems attempt to automate only a small part of the physical description. Much is left to the designers. An exploratory design automation system is being developed at the University of Southern California. The system is intended to be highly interactive and has several features which will enhance the posibilities of automatic physical description. Different approaches and algorithms required to accomplish the "future" system are outlined.

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Engineering Data Management System (EDMS) for Computer Aided Design of Digital Computers

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Introduction

The automated production of digital systems has been taking very important role on designing, manufacturing and testing digital systems toward improvement of the quality, reduction of the development period and saving of the manpower.

Since a digital system has had a trend to be more large scale and more design works have been carried out in DA system, the volume of design data has been rapidly increased, and as the results, its coding miss, the operation of DA system and its data media have also been increased.

The current technology lets a DA system handle the data on various design levels such that pure logical, logical and physical and pure physical information are mixedly used on a PCB design. The design process has not been uniformly carried out, such that the simulation of digital system, the routing and a PCB and a unit design has been carried out at the same time, and made the operation and the management be more difficult and complicated. Therefore, only extention of traditional DA systems tends to be difficult to cope with these situations.

We have studied these problems and developed Engineering Data Management System - EDMS - so as to be open-ended general purpose DA system which can meet with the future innovation of the technology. The followings are main points which we have took into consideration.

(1) The construction of the data base using Data Management System (DMS) We use general purpose MELCOM 7000 DMS - Data Management System - for our DA system in which any network structure may be defined so that the data base may contain any engineering data without the replication, and the data may be efficiently retrieved, stored and modified in any level of the structure on DA programs.

(2) The standardization of the design language The format of the language is standardized so as to prevent miss of coding, to be remembered easily and to be managed in any level of the structure. For this purpose, we have developed a design language translator which checks the validity of the syntax and the value of the design data.

(3) The employment of special DA Monitor A DA monitor has been developed which manages the operation of EDMS and gives various status reports such as the status of DA jobs, and of design history of each designer and the analysis report of troubles in the DA system.

In this paper, we describe the design principle of the system and its implemented structure, and summarize the design language and DA Monitor, and finally we describe one of the experimental results applied to the development of new computer system.