A DFT Approach for Diagnosis and Process Variation-Aware Structural Test of Thermometer Coded Current Steering DACs *

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Abstract– A design for test (DFT) hardware is proposed to increase the controllability of a thermometer coded current steering digital to analog converter. A procedure is introduced to reduce the diagnosis and structural test time from quadratic to linear using the proposed DFT hardware. To evaluate the applicability of the proposed technique, principal component analysis is used to create virtual process variations to simulate in lieu of semiconductor fabrication data. An architecture specific soft fault model is suggested for the diagnosis problem. Random errors according to the fault model are introduced in the virtual test environment on top of the process variations and it is shown that diagnosis of a fault is possible with high accuracy with the proposed method. The same technique employing principal component analysis is furthermore used to provide process variation-aware reference test comparison values for a structural test of the DAC. The structural test provides a mechanism to test for even unmodeled manufacturing faults. The process variation-aware test values help detect defects even under process variations. The proposed DFT hardware and method are low cost and quite suitable for a built-in self diagnosis and test implementation.

Categories and Subject Descriptors

B.7.3 [**Hardware**]: INTEGRATED CIRCUITS: Reliability and Testing—*Built-in tests, Error-checking, Test generation*

General Terms

Design, Reliability, Verification

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Keywords

DFT, BIST, CS-DAC, current steering, test, process variation-aware test, diagnosis

1. INTRODUCTION

Digital to analog converters are used quite often in mixed signal circuits. Thermometer coded current steering (TCCS) digital to analog converters are widely used due to their suitability for high precision requiring applications. Due to increased application demands, the resolution requirements are increasing [10] [17]. These increased requirements augment the size of the circuitry, increasing the difficulty and time in detecting the location of defects or testing the circuit. The thermometer coded circuits though reduce the controllability of the circuit as each bit increment sums the current of a new current source with the previous ones. Hence, it is not possible to access each individual current source. Once one of the current sources is faulty, the faults build up cumulatively. The diagnosis of a fault and the test of the circuit usually are handled by exhaustively incrementing the input bits from 0 to $2^B - 1$ for a B bit converter and observing the differences of output current between each bit increment. This approach requires exponential diagnosis and test time, yet it fails to provide significant structural information. As bit numbers increase, a fast way to diagnose and test for faults is necessary. The provision of such a methodology will enable pinpointing defects and alleviating a major burden on further increasing the bit number of a TCCS DAC.

For data converter circuits, the consideration of soft faults is quite important due to their close relationship with performance parameters such as integral or differential nonlinearity. Soft (parametric) faults are related to the effects of process variations on circuit components. Such faults are present in abundance in analog circuits. As analog circuits are highly optimized, a minor fault can cause significant performance degradation, thereby making the detection of soft faults of utmost importance.

Most soft faults show their effects on circuit specifications. Yet, specification test of a chip does not provide significant insight as to the reasons of failure. The diagnosis of a fault, on the other hand, not only provides the ability to correct for design flaws, but also enables debug of manufacturing defects. Similarly, structural test provides valuable information regarding the manufacturing type of defects that may not show up in the specification tests. The decrease of struc-

tural test and diagnosis time using architecture specific DFT techniques is of paramount importance.

To eliminate the controllability problem, a DFT hardware is proposed. This hardware only necessitates two additional digital test signal pins. An architecture-specific soft fault model is suggested, which furthermore enables the construction of a diagnosis technique which uses the proposed DFT hardware. To ensure thorough experimental evaluation of the proposed ideas, a virtual manufacturing environment is created for simulations. Principal component analysis is used to create process variations whereby a systematic mismatch of current sources is incorporated. Faults are created virtually and it is thereby shown that the success rate of the diagnosis technique is quite high. A similar, principal component based approach is herein used to provide the test engineers with *process variation-aware* test reference points. Through usage of such test values, a correct identification of faulty components can be conducted. The result is not obscured by process variations and only components that indicate significant deviation from the estimations are eliminated. Both the diagnosis and test take linear-time, whereas current practices in the industry are approaching exponential time. The techniques presented in this paper can help refine designs faster and point out manufacturing defects with a low cost in terms of time and hardware, furthermore presenting the possibility of built-in implementation. This low cost technique can also help build higher resolution DAC's as proper diagnosis and testing are fundamental means towards developing improved circuits.

2. PREVIOUS WORK

Initially, fault models for analog circuits have been confined to hard faults. Though considering only hard faults, such a methodology was able to bring a structured approach for analog testing using inductive fault analysis (IFA) [7] [16]. IFA method operates on the circuit layout directly. Hard faults are created with no consideration of circuit functionality at random locations on the layout. IFA is appropriate for hard defects but cannot test for performance degradations.

The unavoidable necessity to consider soft (parametric) faults in the analog domain has led to the consideration of these faults by many researchers. In [8], a concurrent fault simulation technique is introduced. In [9], an ordering scheme to reduce the test time of parametric faults is presented. In [3], an oscillation based test scheme is used to detect faults. In [18], parametric faults are formulated to estimate yield coverage. Masking possibilities for soft faults are shown in [14]. Architecture specific faults are usually more efficient in targeting the correct diagnosis and structural test of a circuit. In particular, recently, architecture specific faults have been presented for the architecture of this work in [2] and [5], where mismatch between current sources of a CS-DAC has been the main fault model.

A branch of approaches for mismatch modeling have consisted of establishing relationships between electrical parameters of matched pairs [11]. This has been followed by statistical methods for mismatch [1] where a principal component analysis is used to evaluate particular effects of parameters on circuit functionality. In [19], BSIM parameters are used for modeling. In [6], a physics based model has been proposed where mismatch is attributed to a number of physical parameters.

Identification of a suitable model also necessitates consideration of a structural test scheme given the increased complexity of current circuits. These tests aim at catching manufacturing defects. For converter architectures, such a scheme was employed for an ADC in [12]. However, this technique is most suitable for a pipelined structure and would be costly in a high resolution DAC.

The area of structural test is closely related to diagnosis, as locating the actual position of the defect is of importance most of the time. For diagnosis, signature analysis has been used [13] [4]. Both require comprehensive fault simulation to create the signatures and are therefore costly. In [15], sensitivities are used for fault diagnosis.

3. THE PROBLEM

Figure 1 shows a current steering architecture. The top portion of the circuit constitutes the m most significant bits (MSB) whereas the bottom portion the n least significant bits (LSB) of a B bit DAC, where B is $m+n$. The LSB of the the top portion is furthermore interpolated by the bottom portion. Current sources are connected to the output branch according to the digital code input to the system. In a binary coded system, each current source is designed to supply current that changes in orders of 2. It becomes impossible to avoid major errors resulting from process variations, as bits with larger weights become much more important at the output response as compared to bits with smaller weights.

In a thermometer coded DAC, on the other hand, each current source is designed to supply equal current. It becomes easier to match current sources and hence better integral non-linearity (INL), differential non-linearity (DNL) and offset can be attained at the output. Furthermore, the thermometer code introduces the possibility of error correction. Error correction is usually implemented in digital circuitry, by taking advantage of the fact that all codes have to fit the regular expression of 0^*1^*; codes that do not fit, such as '00111101' can be automatically converted unambiguously to codes that do, such as '00111111'. Boundary errors are corrected according to the circuit implementation strategy, fault likelihood or arbitrarily. Corresponding thermometer codes for a 3 bit binary code are provided in Table 1 as a reminder.

The thermometer code introduces a controllability problem. Incrementing the binary digital input code to the DAC by one LSB at each step, a new current source is switched on and it is connected to the output branch. It is not possible to activate a number of arbitrary current sources simultaneously but all current sources consecutively indexed from 1 needs to be activated as a group. Eventually, a fault occurring in a current source is seen on the output branch current

Table 1: Thermometer Code for 3 Bit Binary Code

binary	thermometer
000	0000000
001	0000001
010	0000011
011	0000111
100	0001111
101	0011111
110	0111111
111	1111111

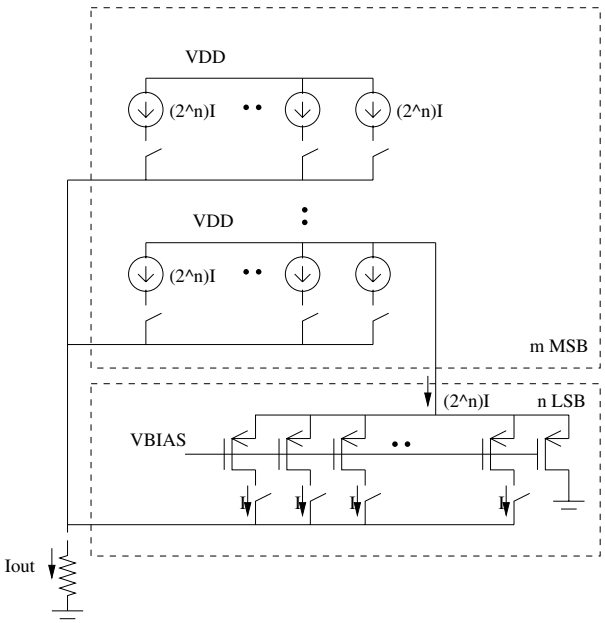

Figure 1: A current steering architecture

for each subsequent input code. This means that the faults are cumulative in the output of a thermometer-coded DAC.

If we were to assume that one of the current sources has a wider deviation from the nominal current value, we could than identify this faulty source by sequentially incrementing each input digital code and measuring output at the same time. Observation of the maximum of the differential output current at each step would yield the detection of the faulty current source. However, this is too costly as for B bit digital inputs, 2^B conditions should be tested. As resolution of DAC's is increasing at a fast pace, diagnosis time is becoming highly intolerable. For the test of DAC's, similarly, all input digital bits are usually scanned exhaustively to test the performance of the DAC.

This exhaustive test, yet, fails to provide a detailed information about the circuit. Manufacturing defects can best be identified by employing a structural test methodology. A structural test can detect unmodeled faults too, like a specification test, but it does this at a lower level, thereby reducing test cost and increasing observability. The increase in observability makes the detection of more faults possible. The structural test can help speed up the re-design process as well as enabling the observation of the effects of technology on the low level structural parts of the circuit. It then becomes necessary to identify ordinary process variations when conducting a structural test, as failure to consider such effects would result in incorrect interpretations regarding the test outcome. The reference test values to be used during the test should consider the effects of process variations. This consideration helps detect unexpected deviations caused by various faults while accepting perturbations caused by process variations.

4. THE DIAGNOSIS PROCEDURE

Matching of the components in a DAC is quite important to keep specifications like INL and DNL within provided bounds. In order to provide a good match, a layout structure named common centroid is almost always used. In this layout structure, matched components are dispersed in a matrix configuration on layout. For CS-DAC, current sources have to be matched. They are dispersed on layout so as to average out the effects of process variations. One such configuration is shown for a 4 bit example in Table 2. The MSB and LSB current sources are matched within themselves.

In thermometer code, m MSB's bits would require 2^m current sources. As can be noted in Table 2, current sources that are consecutively numbered are located on distinct symmetric locations on the layout. MSB and LSB current sources have distinct matrices and hence are matched separately. Considering the MSB's as an example, the matrix size is $2^{m/2}$ by $2^{m/2}$, each entry corresponding to one of the 2^m current sources. It should also be noted that m must be chosen an even number. The arguments above are also applicable to the LSB matrix by replacing m with n.

4.1 The Fault Model for Diagnosis

Architectural level fault models can be quite effective. In our case, a soft model is proposed. The model also considers the systematic mismatch between current sources as a result of process variations. To account for this systematic relationship, correlations are extracted from layout either statistically or using Pelgrom's mismatch model [11]. One current source is assumed to possess a value that is a percentage different from the process variation effected value. This source is assumed to be the faulty one. The diagnosis technique targets locating this faulty current source in linear time as opposed to a quadratic time with current techniques.

4.2 The Diagnosis Algorithm

The diagnosis procedure consists of checking the sum of each row and column of the location matrix. Let i be the enumeration over current sources where $i \in \{1..N\}$ and N is the total number of current sources either in the MSB or LSB matrices. Let C_j and R_j denote the $j'th$ column and row respectively. Let I_i denote the current of the $i'th$ source. Then, we can write

$$I_{C_j} = \sum_{i \in C_j} I_i \qquad \forall j \in \{1..\sqrt{N}\} \tag{1}$$

$$I_{R_j} = \sum_{i \in R_j} I_i \qquad \forall j \in \{1..\sqrt{N}\} \tag{2}$$

where I_{C_j} and I_{R_j} are the $j'th$ column and row current sums respectively. Then one can write

Table 2: Example Configuration for Thermometer coded 4 bits

1	12	15	3
13	5	7	10
9	8	6	14
4	16	11	2

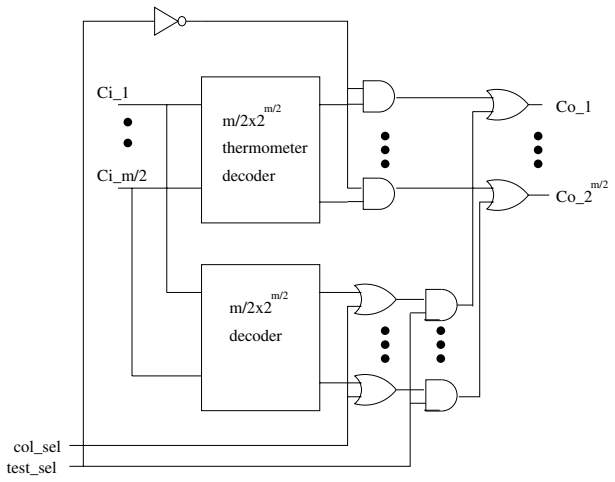

Figure 2: The DFT hardware

$$p = arg_{j\in\{1..\sqrt{N}\}} max(I_{C_j}, \sum_{k\neq j \wedge k\in\{1..\sqrt{N}\}} \frac{1}{(\sqrt{N}-1)} I_{C_k}) \tag{3}$$

$$r = arg_{j\in\{1..\sqrt{N}\}} max(I_{R_j}, \sum_{k\neq j \wedge k\in\{1..\sqrt{N}\}} \frac{1}{(\sqrt{N}-1)} I_{R_k}) \tag{4}$$

where p and r indicate the column and row indices of the faulty current source. This procedure corresponds to checking each column current sum with respect to the average current sum of the remaining columns and identifying the one that deviates the most. A similar step is handled within the row sums. Hence, the process necessitates activation and observation of $2 * \sqrt{N}$ current values. Letting $P = \sqrt{N}$, the process has a time complexity of $O(P)$, which is linear. Current practices, in contrast, exhibit $O(P^2)$ time complexity.

4.3 Required DFT Hardware

The procedure requires activation of current sources that are not consecutively enumerated. Hence a hardware that allows concurrent activation of current sources on each row and column should be designed. Such a modification is given in Figure 2 for the column decoding circuitry. A similar circuitry is also used for the row decoding circuitry, except that the column select input is inverted and input as the row select input. In Figure 2, the original circuitry corresponds to the column thermometer decoder only. This decoder, along with the row thermometer decoder, is used the select consecutively enumerated current sources. In test mode, the thermometer decoder is bypassed. If the column select bit is 0, then the binary input selects a column. The row DFT decoder, in this mode, selects all rows. Hence, eventually, only one column is selected. When the column select bit is 1, on the other hand, input bits are used to select a row and all columns are selected. Hence one row ends up being selected.

5. THE STRUCTURAL TEST PROCEDURE

For structural test, sums of row and column current sources need to be checked with respect to their expected values. In structural test, comparing with nominal values may not provide significant information about possible defects in the circuit, as process variations are most of the time present in the circuit. To overcome this problem, expected values for the test results need to be estimated by considering the process variations. This consideration will provide process variation-aware test reference points for each individual chip. So, even unmodeled faults can be detected by comparing the real chip measurement results with the estimated values.

5.1 Estimating Process Variation-Aware Test Results

Process variations are usually provided with a statistical or probabilistic equation for current sources. However, for each particular chip implemented on silicon, each current source will display a particular value sampled out of its own probability density function. Identification of a method capable of measuring a very limited number of these current sources and the consequent estimation of the values of the remaining ones enables the incorporation of the process variation information in our test reference points with small cost.

It is known that the current sources are correlated to each other due to their pair-wise distances on the chip. Yet statistically, these correlated variables can be individually represented as a sum of independent components through a technique called principal component analysis (PCA). If the currents of the current sources are normalized $\frac{I-\mu}{\sigma}$, then we can write

$$I' = U^T C \tag{5}$$

where I' is a vector consisting of normalized current source variables. The normalization step is handled by decrementing the mean and dividing by the variance of a current source. U is the matrix consisting of the eigenvectors of the correlation matrix. The entries of the C vector are the principal components. The largest eigenvalue corresponds to the principal component that provides the largest variation in data. Hence, principal components corresponding to the largest eigenvalues are satisfactory in accounting for most of the variation. The ratio of the sum of the selected eigenvalues to the sum of all eigenvalues can be used to ensure a minimum variation percentage with respect to accounting for the whole variation by selecting this ratio higher than the variation percentage. Equation 5 can be written in detailed from as:

$$\begin{pmatrix} I'_1 = u_{11}C_1 + u_{21}C_2 + .. + u_{N1}C_N \\ I'_2 = u_{12}C_1 + u_{22}C_2 + .. + u_{N2}C_N \\ . \\ . \\ I'_N = u_{1N}C_1 + u_{2N}C_2 + .. + u_{NN}C_N \end{pmatrix} \tag{6}$$

As a small number of principal components is satisfactory in providing most of the variation; we therefore first determine the number of principal components that are necessary to account for the selected minimum variation percentage. Selecting a reduced number, $M < N$, of these components is equivalent to reducing the number of unknowns by deleting some of the sum terms:

Table 3: Comparison of Real and Extracted Normalized Current Values

I	$(I - I_{extracted})$	$(I - I_{extracted})/I$
0.5325	0	0
0.1949	0	0
-0.2455	0.0278e-15	-0.0113e-14
-0.0931	-0.1943e-15	0.2087e-14
0.0219	-0.0833e-15	-0.3808e-14
-0.0167	-0.0555e-15	0.3328e-14
0.2214	-0.222e-15	-0.1003e-14
0.3334	0	0
-0.1268	-0.0833e-15	0.0657e-14
0.5184	0.111e-15	0.0214e-14
-0.1070	0.1665e-15	-0.1556e-14
0.0229	0.111e-15	0.4846e-14
-0.0977	-0.0278e-15	0.0284e-14
0.1205	0.0833e-15	0.0691e-14
-0.0824	0.0555e-15	-0.0674e-14
0.4668	-0.0555e-15	-0.0119e-14

$$\begin{pmatrix} I'_1 = u_{11}C_1 + u_{21}C_2 + .. + u_{M1}C_M \\ I'_2 = u_{12}C_1 + u_{22}C_2 + .. + u_{M2}C_M \\ . \\ . \\ I'_N = u_{1N}C_1 + u_{2N}C_2 + .. + u_{MN}C_M \end{pmatrix} \quad (7)$$

Then, M of these equations are chosen so that an M equation-M unknown system is obtained. The selection is made from the top of the equation list so that I_i values are able to be measured irredundantly by consecutively incrementing the input digital code. A choice of equations from non-consequent lines of Equation 7 would increase the number of measurements up to two-fold due to the additive nature of a thermometer coded structure necessitating two measurements to detect an individual current value. While an alternative set of M equations would result in C_i values that are likely to be slightly different, the increased error is bounded by the selected minimum variation percentage. Minimization of the associated error requires a selection of equations where the sum of discarded u_{ij} values is minimal leading to a possible increase in number of required measurements.

For each row, I_i values are measured on chip. The u_{ij} values, entries of U, are calculated using the correlation matrix. Hence, only C_i values are left to be determined. These reduced number of equations are then solved to find the C_i values where i takes values in the range of 1 up to the number of selected principal components. Using the remaining equations and substituting the determined C_i values, all I_i values are calculated. Hence, it becomes possible to obtain all I_i values without measuring the currents exhaustively. Then using the layout matrix, as we know where each current source is located, we can calculate the test results for each row and column. These test results will be used for that particular chip during test. The error introduced by PCA should be kept below the test thresholds to be used.

6. EXPERIMENTAL RESULTS

We have used layout information to extract the correlation matrix. The nominal values are extracted from the schematics of a CS-DAC design. Variances of current sources are assumed to be 10%. The remaining calculations are performed using MATLAB R12.

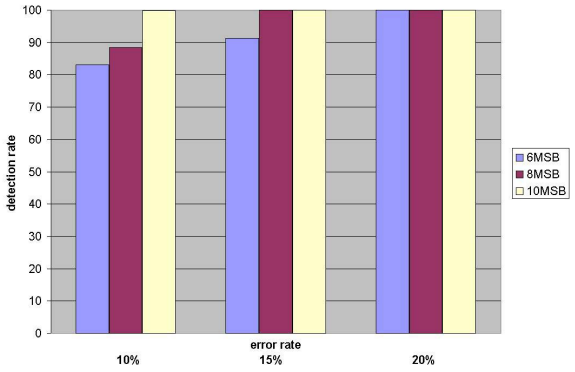

Figure 3: Detection rate versus error rate

For evaluating diagnosis accuracy, unit random principal components are generated. Using the correlation matrix and Equation 5, normalized current source values are found. This mimics the effects of process variations on a particular chip. On consecutive runs, the principal components are randomly updated and hence, a new chip is virtually created. The normalized current source values are denormalized by multiplying with their variances and summing their mean values. A fault is generated using the fault model that ranges from 10% variation to 20% variation. Then, the detection algorithm is run to detect the location of the faulty current source.

Considering the increased size of matching matrices, the diagnosis procedure is repeated on 6, 8 and 10 bit matching requirements corresponding to 64, 256 and 1024 matched current sources, respectively. The true detection rate is given in Figure 3 and can seen to be approximating 100%. It can be observed that the diagnosis procedure is increasingly accurate as the number of matched current sources increases. This is the result of averaging more current source column or row sums and being able to differentiate this average from the faulty one more efficiently. Increasing the fault rate makes the diagnosis easier. It can be observed that even at 20% error rate, we are able to attain around 100% detection. This implies that any fault exceeding this fault rate is also detected at a 100% rate.

For the structural test, we have used principal components that can account for 98% of the whole variation. After randomly creating principal components, only the number of principal components that account for 98% variation are used to estimate the remaining current sources. The normalized values of initial currents are given in Table 3 in the first column for all 16 current sources for a 4 MSB matching matrix. The middle and right-most columns indicate the absolute and relative error involved for each current source, respectively. Notice that these error rates are below noise levels for each current source and hence are negligible.

7. CONCLUSIONS

An approach for diagnosis and structural test of thermometer coded DAC's is provided, along with a method to reduce the test and diagnosis time from quadratic to linear. A DFT hardware is used to implement this method.

Using the provided soft fault model, diagnosis of minor deviations is possible. For structural test, process variation-aware test points are provided using principal component analysis. These low cost techniques will enable the development of converters of higher resolution by being able to locate and test defects by the proposed diagnosis and structural test procedures respectively.

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