A Noise-Driven Effective Capacitance Method With Fast Embedded Noise Rule Calculation for Functional Noise Analysis

Haihua Su David Widiger Chandramouli Kashyap
Frank Liu Byron Krauter
IBM Corporation
11400 Burnet Road
Austin, TX 78758
{haihua,widiger,chandrak,frankliu,krauter}@us.ibm.com

ABSTRACT

We present a noise-driven effective capacitance method for estimating the combined propagation noise and crosstalk noise. Gate propagation noise rules are efficiently calculated inside the Ceff procedure to determine a linear Thevenin model of the victim driver. A voltage-dependent current source model [2, 6] of the driver, along with a load capacitor is analyzed to generate the gate output waveform, from which noise rules are directly extracted. This method removes potential errors introduced in traditional look-up table or fitted-equation based noise rules. The linear driver Thevenin model can then be employed to analyze the propagation noise, while the same Thevenin resistance can be used to analyze the crosstalk noise. The combined coupling and propagation noise can then be estimated using superposition. In this work, we extend the popular timing-driven effective capacitance method into the noise domain. Similar to the effective capacitance method in timing analysis, this technique can successfully separate the nonlinear driver analysis from the linear interconnect analysis. In addition, the linear driver model can significantly ease the task of finding the worst-case peak alignment among all the victim and aggressor noise sources. Experimental results on both RC and RLC nets from industry designs show both accuracy and efficiency compared to SPICE results.

Categories and Subject Descriptors: B.8.2 [Hardware]: Performance Analysis and Design Aids

General Terms: Algorithms,

Keywords: Effective Capacitance, Glitch Propagation, Noise Analysis

1. INTRODUCTION

The continuous scaling of CMOS processes leads to increased noise in digital integrated circuits (ICs). Functional noise analysis attempts to capture noise glitches that can potentially alter the state of a storage element (e.g., a latch). Because of the nonlinearity of the victim driver, the combined propagation and coupling noise is typically much higher than a simple superposition of each individual noise [10], therefore the victim driver has to be carefully modeled to ensure reasonable noise results.

Two general approaches have been proposed for victim driver modeling and worst-case noise analysis. The first approach linearizes the victim driver and keeps the coupled aggressor and victim circuit a linear system. In this approach, the worst-case peak alignment between the victim and aggressors can be obtained using superposition. However, such an approach can introduce considerable amount of error if the linear model is not carefully obtained. If the driver resistance is too high, the propagation noise will be under-estimated while the crosstalk noise will be over-estimated. Similarly, an under-estimated driver resistance will over-estimate the propagation noise and under-estimate the crosstalk noise. For example, it has been reported in [10] that for a 130 nm technology, the simplified method can underestimate the noise peak by as much as 70%.

The second approach characterizes the driver using a simple nonlinear behavioral model consisting of a voltage dependent current source and parasitic capacitors [2, 4, 6]. To analyze such a model, a fast nonlinear transient analysis engine with numerical integration techniques has to be employed. One limitation of such a behavioral model is that it only works well for simple gates whose internal capacitance is non-dominant. For multiple-stage gates, each channel-connected-component (CCC) has to be analyzed separately. In addition, the introduction of nonlinearity in the circuit makes the worst-case peak alignment between the victim and aggressors costly. For each sink, the aligment has to be iteratively achieved, and in each iteration a nonlinear analysis of the behavioral model along with the interconnect circuit has to be performed.

The method presented in [10] belongs to the first approach, which computes a linear Thevenin model for the victim driver. For improved accuracy, its computation of the linear victim driver parameters involves the matching of the linear driver current to the nonlinear current through the interconnect driven by the nonlinear behavioral model being used in the second approach. In this model, several Thevenin model parameters, such as the Thevenin resistance

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and the Thevenin voltage pulse width are empirically chosen and therefore the characterization process becomes complicated. For example, in order to improve accuracy, the authors propose to superimpose two trianglar waveforms with different pulse widths. In addition, their model is only specific for noise and is not available in general industry flow.

2. OUR METHOD

In this paper, we propose a noise-driven effective capacitance method to linearize the victim driver. Propagation noise is a function of both the input noise glitch and the output effective capacitance, which is typically part of the total wiring capacitance due to resistive shielding. Similar to [10], noise glitches are allowed to propagate to the latch inputs, even though in the middle of the propagation path some significant glitch could cause a failure for the gate. Under this methodology, resistive shielding effect can be as significant as in timing since instead of a switching signal, a noisy signal of high amplitude and wide pulse width can be applied to the input of the gate.

Recently, the Ceff method has been criticized due to its historical reason of mapping the complicated interconnect model to one capacitance being used in cell libraries. However, the benefit of Ceff is not only in providing such a mapping, but also in providing a most efficient linearization engine for the nonlinear driver. Several Ceff papers [1,3] have emphasized on how to compute the driver linear Thevenin model and the actual value of C_{eff} is never used in the timing analysis flow. The major advantage of a linear driver model for coupling noise analysis lies in the fact that the computation-intensive victim and aggressors peak alignment can be avoided by superposition and that the entire interconnect can be efficiently analyzed using reduced order modeling methods [7,8].

The input to our algorithm is the input noise pulse width W_i and peak P_i at the victim driver, while the output of the algorithm is the linear Thevenin voltage source V_{TH}, resistor R_{TH} and the propagation noise at the net sinks. A numerical simulator is embedded to analyze the nonlinear driver behavioral model [2, 4, 6, 10] with a capacitor. Propagation noise rules capturing the output noise as functions of input noise and output capacitance are extracted from the resulting output waveform. The construction of the linear Thevenin model is based on the iterative effective capacitance algorithm. The essential process can be summarized as follows. First, for any particular effective capacitance C_{eff}, the gate Thevenin model parameters are first constructed to match the gate propagation noise rules assuming pure capacitive load of C_{eff}. Next, for a fixed Thevenin driver, the C_{eff} is updated so that the average current measured up to the noise peak arrival time is the same, when driving either the pure effective capacitance C_{eff} or a reduced-order model of the interconnect. Our experiments show that a typical convergence of C_{eff} can be reached within 3 to 5 iterations.

3. PROPAGATION NOISE RULE CALCULATION

We propose to simulate a simplfied nonlinear model of the driver with a load capacitor (Fig. 1(b)) to obtain the noisy output waveform, from which noise properties (rules) are directly extracted without any loss of accuracy. The

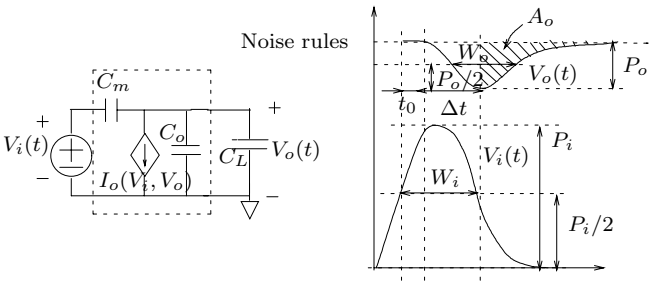

Figure 1: A noisy waveform versus a switching waveform.

simplifed driver model, originally proposed in [2, 4, 6, 10], consists of a DC voltage-dependent output current source $I_o(V_i, V_o)$, a DC voltage transfer function $V_o(V_i)$, an input capacitor C_i, a miller capacitor C_m and an output capacitor C_o. The nodal equation of the circuit shown in Fig. 1 is

$$(C_m + C_o + C_L)\frac{dV_o}{dt} = C_m\frac{dV_i}{dt} - I_o(V_i, V_o), \qquad (1)$$

which is a single-variable (V_o) nonlinear ODE that can be efficiently solved using any known numerical techniques.

The 2-D DC load table $I_o(V_i, V_o)$ and the 1-D DC voltage transfer table $V_o(V_i)$ can be precharacterized by DC simulations sweeping input and output voltages for each channel-connected-component (CCC) of the driver. As far as propagation noise is concerned, only cells with one or two stages of CCCs need to be characterized since glitches at the primary input can typically be suppressed by drivers with more CCCs. While parasitic capacitances can be obtained by measuring charge [4], load capacitance is dominant in real circuits. Hence as long as the dependent load current model drives a reasonable load capacitor, dropping the parasitic capacitances does not impact the accuracy of the output waveform too much.

The advantage of using the simple nonlinear model to calculate noise rules is as follows. First, this model is independent of input waveforms and output loads. Therefore, this method can remove potential errors introduced by characterizing different wave shapes and interpolation errors that are typically seen in timing analysis. Second, the noise rule circuit is either a single-node or a double-node nonlinear system and the convergence to the steady-state DC solution can be fastly achieved assuming that propagation noise through gates of more than two stages can be ignored. Last, the characterization table is restricted to one 2D load current table, and one 1D voltage transfer table, so the table size can be more reasonable compared to the four 3D or 4D tables in existing cell libraries [9].

Once the accurate output noise waveform is available, noise characteristics can be obtained from the waveform. In our work, we extract the following noise characteristics for the computation of the driver linear Thevenin model in our Ceff procedure. Noise rules defined in Table 1 have some redundancy in representing the output noise waveform. A smaller set of properties necessary for the computation can include only output noise peak (P_o), output noise width (W_o) and output rising transition time to peak (Δt). If necessary, some tradeoff in accuracy can be made, for example, by assuming $A_o = P_o * (2 * W_o - \Delta t)/2$ can save the effort of finding the post-peak area from the output waveform.

T_0	gate intrinsic noise delay
Δt	noise transition time to peak
P_o	noise peak
W_o	noise pulse width
A_o	noise post-peak area

Table 1: Noise rule definitions.

4. THEVENIN MODEL COMPUTATION

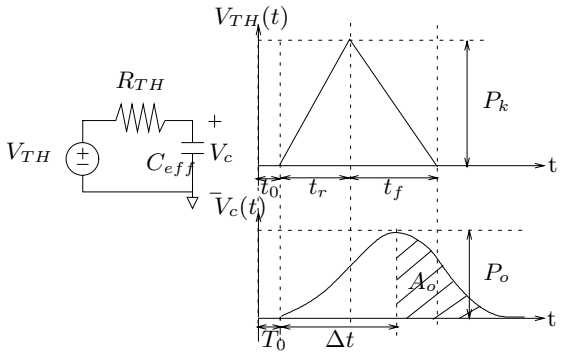

Figure 2: The Thevenin model with an effective capacitance.

Our Thevenin voltage source is modeled using a time-varying triangular waveform, with delay t_0, rising transition time to peak t_r, falling transition time from peak t_f and peak P_k. Given the noise pulse width W_i and peak P_i at the victim input and a specific load capacitance C_L, and given a specific Thevenin resistance R_{TH}, the gate Thevenin voltage source parameters are chosen to match the output waveform $V_c(t)$ (shown in Fig. 2) whose key characteristics are represented by the propagation noise rules shown in Table 1.

We assume the delay t_0 of the Thevenin voltage source is the same as the gate intrinsic noise delay T_0, i.e. $t_0 = T_0$. We choose the three parameters $t_r > 0$, $t_f > 0$ and $P_k > 0$ to match the output noise rules as follows:

$$V_c(\Delta t) = P_o \tag{2}$$

$$V_c'(\Delta t) = 0 \tag{3}$$

$$A_o = \int_{\Delta t}^{\infty} V_c(t)dt \tag{4}$$

where Eqn (2) matches the output noise peak, Eqn (3) matches the output noise rising transition time to peak and Eqn (4) matches the post peak noise area.

Through some mathematical derivation, we obtain three equations representing the relationship between the Thevenin voltage source parameters t_r, t_f and P_k and the noise rules, as well as the Thevenin resistance R and load capacitance C.

The first equation shows the relationship between the peak of the Thevenin voltage and the peak of the output noise waveform:

$$P_o = P_k \frac{t_r + t_f - \Delta t}{t_f}, \tag{5}$$

and the second equation reveals the fact that the sum of t_r and t_f is constant, given a fixed noise rule of A_o, P_o and Δt, and values of R and C:

$$t_r + t_f = \frac{2A_o}{P_o} + \Delta t - 2RC = T_c \tag{6}$$

The third equation is a nonlinear equation of t_r:

$$f(t_r) = (1 - e^{\frac{\Delta t}{RC}})t_r + T_c e^{\frac{t_r}{RC}} - T_c = 0 \tag{7}$$

where $0 < t_r < T_c$. This equation can be efficiently solved using Newton-Raphson within a couple of iterations. Once t_r is computed, t_f and P_k can be obtained from Eqn. (5) and Eqn. (6).

Taking the partial derivative of Eqn. (6) with respect to C, we can get

$$R = 0.5\frac{\partial(2A_o/P_o + \Delta t)}{\partial C} \approx \frac{\partial W_o}{\partial C}, \tag{8}$$

which shows that the driver Thevenin resistance can be approximated by the sensitivity of the output noise pulse width with respect to the output capacitance. Typically, the resistance value in the presence of an input noise pulse is higher than the quiet one. The coupling noise anlysis using such a higher driver resistance can often capture the amplifying effect of the gate. Additionally, even though the actual gate driving resistance changes with time, R_{TH} is on an average a good linear approximation.

The sensitivity-based driver resistance in Eqn. (8) assumes non-negligible output noise pulse with a finite pulse width. There are often cases when the nonzero input noise pulse is not strong enough to cause a non-negligible output noise pulse. In such cases, the driver resistance can be found from the DC load current table $I_o(V_i, V_o)$ and the DC voltage transfer table $V_o(V_i)$ by assuming an average input voltage level V_i [10].

5. CONVERGENCE DISCUSSION

The convergence of our effective capacitance procedure falls into the following three scenarios:

- Regular triangular Thevenin voltage source with $t_r > 0$, $t_f > 0$ and $P_k > 0$ and regular effective capacitance C_{eff} where $0 < C_{eff} < C_{total}$.
- Effective capacitance $C_{eff} = 0$ when $\overline{I_{actual}}$ is close to zero. In this case propagation noise is negligible and therefore we set $P_k = 0$.
- Thevenin voltage source has very sharp rising transition with t_r close to or equal to zero, which corresponds to the case when Eqn. (7) has no nonzero solution for t_r. In this case we specially choose the two parameters $t_f > 0$ and $P_k > 0$ to match the output noise rules as follows:

$$V_c(\Delta t) = P_o \tag{9}$$

$$\int_0^{\infty} V_c(t)dt = A_{total} \approx P_o \Delta t/2 + A_o \tag{10}$$

where Eqn (9) is to match the output noise peak and Eqn (10) is to match the total output noise area.

6. EXPERIMENTAL RESULTS

The noise-driven effective capacitance algorithm with embedded noise rule calculation has been implemented in C++.

We have tested our method using two global netlists extracted from a high performance microprocessor corresponding to the $0.13\mu m$ technology and the supply voltage of 1.2V. In a typical microprocessor design, around $10\% \approx 20\%$ on-chip global interconnects are inductively coupled and they are usually critical wires. Therefore, we choose one netlist which has inverters driving two $1mm$-long capacitively coupled lines, and the other which has inverters driving two $5mm$-long lines with both capacitive and inductive coupling. One line is the aggressor and the other is the victim. All the experiments are run on an AIX machine with 1GB memory.

	Input noise		Sink noise (SPICE)		Sink noise (C_{eff})			
	P_i	W_i	P_s	A_s	P_s	Err%	A_s	Err%
rc	0.86	0.100	0.845	0.0697	0.819	-3.1%	0.0657	-5.8%
	0.86	0.200	1.016	0.1501	0.992	-2.4%	0.1408	-6.2%
	0.63	0.100	0.353	0.0242	0.367	+3.9%	0.0252	+4.3%
	0.63	0.200	0.479	0.0549	0.490	+2.3%	0.0575	+4.8%
	0.48	0.100	0.133	0.0090	0.139	+4.7%	0.0093	+3.0%
	0.48	0.200	0.160	0.0187	0.171	+6.7%	0.0201	+7.7%
	0.35	0.100	0.053	0.0035	0.056	+5.1%	0.0037	5.7%
	0.35	0.200	0.061	0.0070	0.065	+6.0%	0.0078	+10.8%
rlc	0.86	0.100	0.619	0.0626	0.673	+8.7%	0.0697	+11.3%
	0.86	0.200	0.925	0.1441	0.916	-1.0%	0.1431	-0.7%
	0.63	0.100	0.260	0.0228	0.273	+5.1%	0.0273	+19.8%
	0.63	0.200	0.386	0.0506	0.414	+7.2%	0.0577	+13.9%
	0.48	0.100	0.096	0.0088	0.099	+3.7%	0.0098	+11.6%
	0.48	0.200	0.133	0.0181	0.145	+8.9%	0.0203	+12.2%
	0.35	0.100	0.038	0.0034	0.040	+6.1%	0.0038	+10.8%
	0.35	0.200	0.051	0.0069	0.057	+10.9%	0.0078	+12.7%

Table 2: Sink propagation (without coupling) noise comparison between our C_{eff} method and SPICE.

	Input noise		Sink noise (SPICE)		Sink noise (C_{eff})			
	P_i	W_i	P_s	A_s	P_s	Err%	A_s	Err%
rc	0.86	0.100	1.055	0.0834	0.974	-7.7%	0.0723	-13.3%
	0.86	0.200	1.202	0.1623	1.147	-4.6%	0.1474	-9.2%
	0.63	0.100	0.592	0.0375	0.541	-8.7%	0.0334	-10.9%
	0.63	0.200	0.719	0.0711	0.664	-7.7%	0.0658	-7.4%
	0.48	0.100	0.332	0.0180	0.317	-4.5%	0.0179	-0.5%
	0.48	0.200	0.370	0.0292	0.348	-5.9%	0.0286	-2.1%
	0.35	0.100	0.216	0.0104	0.211	-2.5%	0.0103	-0.8%
	0.35	0.200	0.227	0.0142	0.220	-2.9%	0.0143	+0.8%
	0.12	0.200	0.153	0.0066	0.167	+9.4%	0.0077	+17.4%
rlc	0.86	0.100	0.972	0.0833	0.988	+1.6%	0.0860	+3.2%
	0.86	0.200	1.272	0.1687	1.231	-3.3%	0.1595	-5.5%
	0.63	0.100	0.582	0.0405	0.596	+2.3%	0.0460	+13.7%
	0.63	0.200	0.737	0.0727	0.737	0.0%	0.0763	+5.0%
	0.48	0.100	0.413	0.0256	0.423	+2.4%	0.0289	+12.8%
	0.48	0.200	0.458	0.0360	0.469	+2.4%	0.0393	+9.3%
	0.35	0.100	0.354	0.0200	0.351	-0.7%	0.0192	-3.9%
	0.35	0.200	0.369	0.0237	0.368	-0.4%	0.0232	-2.4%
	0.12	0.200	0.317	0.0168	0.317	0.0%	0.0167	-0.6%

Table 3: Sink total coupling and propagation noise comparison between our C_{eff} method and SPICE.

Table 2 lists the sink propagation noise results at the far end sink of the line for different input noise peaks and widths. Similarly Table 3 lists the combined propagation and coupling noise results. We compare the noise results obtained from our C_{eff} procedure to SPICE results by showing the percentage error of the noise peak and the total noise area. Our method shows good accuracy compared to SPICE for both the RC and the RLC case at various input noise pulse widths and heights. The combined noise results in SPICE are obtained by iterative peak alignment assuming infinite timing windows of the victim input noise arrival and the aggressor switching time, which typically takes hours for each case.

Table 4 shows the total wiring capacitance versus the effective capacitance "seen" by the driving gate at different input noise widths and heights. As expected, all the effective capacitance is within the range between zero and the total wiring capacitance. Convergence can be seen to be within 7 iterations in our experiments. The last column lists the CPU time for each testcase. including the time of model order reduction.

	Input peak (V)	Input width (ns)	Total cap (pF)	Effective cap (pF)	Num itr	CPU time (s)
rc	0.86	0.100	0.20	0.17	3	0.24
	0.86	0.200	0.20	0.18	3	0.27
	0.63	0.100	0.20	0.17	4	0.23
	0.63	0.200	0.20	0.18	3	0.23
	0.48	0.100	0.20	0.17	4	0.25
	0.48	0.200	0.20	0.18	3	0.25
	0.12	0.200	0.20	0.19	3	0.18
rlc	0.86	0.100	0.89	0.49	7	0.36
	0.86	0.200	0.89	0.71	5	0.39
	0.63	0.100	0.89	0.48	6	0.32
	0.63	0.200	0.89	0.68	5	0.36
	0.48	0.100	0.89	0.49	5	0.29
	0.48	0.200	0.89	0.69	4	0.31
	0.12	0.200	0.89	0.80	3	0.23

Table 4: Effective capacitance, convergence and the CPU time.

7. CONCLUSION

We have presented an algorithm to address efficient propagation and coupling noise computation in traditional static noise analysis. The method is based on effective capacitance, a concept originally introduced in timing analysis. The proposed procedure captures both the nonlinearity of the victim driver and the resistive shielding effect in the interconnect. Embedded propagation noise rule calculation is performed through fast simulation of a simplifed nonlinear model of the driver. Experiments show that the proposed method can provide both efficient and accurate results compared to SPICE.

8. REFERENCES

[1] R. Arunachalam, F. Dartu, and L. Pileggi. CMOS Gate Delay Models for General RLC Loading. In *Proc. ICCAD*, pages 224–229, October 1997.

[2] J. F. Croix and D. F. Wong. Blade and Razor: Cell and Interconnect Delay Analysis Using Current-Based Model. In *Proc. DAC*, pages 386–389, June 2003.

[3] F. Dartu, N. Menezes, and L. Pileggi. Performance Computation for Precharacterized CMOS Gates with RC Loads. *IEEE TCAD*, pages 1526–1535, May 1996.

[4] R. N. Kanj, T. Lehner, B. Agrawal, and E. Rosenbaum. Noise Characterization of Static CMOS Gates. In *Proc. DAC*, pages 888–893, June 2004.

[5] C. V. Kashyap and B. L. Krauter. A Realizable Driving Point Model for On-Chip Interconnect with Inductance. In *Proc. DAC*, pages 190–195, June 2000.

[6] I. Keller, K. Tseng, and N. Verghese. A Robust Cell-Level Crosstalk Delay Change Analysis. In *Proc. ICCAD*, pages 147–154, November 2004.

[7] A. Odabasioglu, M. Celik, and L. T. Pilleggi. PRIMA: Passive Reduced-order Interconnect Macromodeling Algorithm. *IEEE TCAD*, pages 645–654, Aug 1998.

[8] L. T. Pileggi and R. Rohrer. Asymptotic Waveform Evaluation for Timing Analysis. *IEEE TCAD*, pages 352–366, April 1990.

[9] Synopsys Corp. *Library Compiler: Modeling Timing and Power*, 2004.

[10] V. Zolotov, D. Blaauw, S. Sirichotiyakul, M. Becer, C. Oh, R. Panda, A. Grinshpon, and R. Levy. Noise Propagation and Failure Criteria for VLSI Designs. In *Proc. ICCAD*, pages 587–594, November 2002.