

The Real-Time Systems Research Group is now one of the largest academic research groups in the world focusing on the engineering of real-time systems.

*Aim of the Group: To undertake fundamental research, and to bring into engineering practice modern techniques, methods and tools.*

*By what means can a system utilise free resources at run-time, to increase system utility, but still be guaranteed to meet its fundamental timing constraints?*

*Can a computational model for real-time systems be defined that is effective in terms of schedulability analysis, but can also be formally specified and implemented?*

*How can we implement, in combinations of software and hardware, complex real-time systems to meet timing and resource constraints?*

*To what extent can real-time systems be made architecture neutral?*

## **What is Real-Time?**

A system is defined as being *real-time* if it is required to respond to input stimuli within a finite and specified time interval. The stimuli being either an event at the interface to the system or some internal clock tick that is, at least notionally, coordinated with the passage of time in the system's environment. Real-time systems are found in a wide range of applications areas, from simple domestic appliances to multi-media systems, large scale process control and safety critical avionics. In some systems the required response times are measured in milliseconds, in others it is seconds or even minutes. Nevertheless they all have deadlines that must be satisfied. In the production of real-time systems, it is insufficient to use testing of the final system to ensure compliance with the timing requirements. A comprehensive and systematic approach to specification, design, implementation and analysis is required.

## **Areas of Activity**

The overall goal of the group is to facilitate the design, construction, analysis and maintenance of potentially complex systems which have real-time constraints. The work of the group spans a wide range of topics associated with timing analysis, system design, programming languages, operating system kernels, and reconfigurable hardware.

## **Projects and Funding**

Areas of application of our work include space and avionic systems, engine controllers, automobile control and multi-media systems. Work has been funded by the EPSRC and DTI, BAE SYSTEMS, European Union, European Space Agency (ESA), NASA, QinetiQ, Rolls Royce Aeroengines, DTI, the Health and Safety Executive (HSE), Sun Microsystems, Philips Research, Microsoft.

## **Further Information**

Further information and research papers can be accessed on the World Wide Web at URL <http://www.cs.york.ac.uk/rts>. To discuss educational and research opportunities contact Alan Burns (Email: [Alan.Burns@cs.york.ac.uk](mailto:Alan.Burns@cs.york.ac.uk), phone: +44 1904 432779) or Andy Wellings (Email: [Andy.Wellings@cs.york.ac.uk](mailto:Andy.Wellings@cs.york.ac.uk), phone: +44 1904 432742) at The Department of Computer Science, University of York, Heslington, York YO10 5DD, United Kingdom.

DESIGN SYNTHESIS	<b>Neil Audsley:</b> Design, analysis and implementation of embedded real-time systems; hardware/software co-design, FPGAs, kernels and toolsets. Senior Lecturer.
STATIC CODE ANALYSIS	<i>Mohammed Al Rahmawy:</i> Mobile real-time systems: Research Student
WORST-CASE EXECUTION TIME (WCET) ANALYSIS	<b>Iain Bate:</b> WCET, platform optimisation, co-design issues (HW/SW and control/scheduling), industrial applications: Lecturer.
	<i>Adam Betts:</i> WCET Analysis: Research Student.
SEARCH-BASED ENGINEERING	<b>Guillem Bernat:</b> Scheduling theory, worst-case execution time analysis, probabilistic techniques for timing analysis: Lecturer.
DISTRIBUTED & PARALLEL ARCHITECTURES	<b>Alan Burns:</b> Scheduling theory, languages, architectures including kernels and communication protocols, dependability: Professor.
	<b>Rob Davis:</b> Flexible real-time scheduling: Senior Research Fellow
	<i>Paul Emberson:</i> Automating architecture trade-off using scenarios: Research Assistant
	<i>Ian Gray:</i> High-Level hardware synthesis: Research Student
CONCURRENT OBJECT-ORIENTED LANGUAGES	<i>Min Seong Kim:</i> Real-time event handling, RTSJ: Research Student
	<i>Nick Lay:</i> Reliability of real-time embedded systems: Research Student
DESIGN METHODS	<i>Addul Haseeb Malik:</i> Real-time memory management, NUMA architectures: Research Student
	<i>Amine Marref:</i> Hardware sensitive WCET calculation: Research Student
PROBABILISTIC THEORIES OF TIME	<i>Osmar Marchi dos Santos:</i> Real-time fault tolerance, RTSJ: Research Student
	<i>Ameet Patil:</i> Application-specific real-time resource management: Research Student
COMMUNICATIONS	<i>Tom Richardson:</i> Real-time component engineering: Research students
	<i>Zheng Shi:</i> Networks on chip: Research Student
SENSOR NETWORKS	<i>Ioanna Symeous:</i> Sensor nets, logic: Research Student
	<i>Jonathan Tate:</i> sensor nets, resource-aware system management: Research Student
REAL-TIME JAVA	<i>Alex Wood:</i> WCET and machine learning: Research Student
FAULT TOLERANCE	<i>Paul Usher:</i> Distributed real-time operating systems. Research Student.
	<i>Michael Ward:</i> Compilation of Ada to reconfigurable hardware. Research Fellow.
TECHNOLOGY TRANSFER	<b>Andy Wellings:</b> Languages, Real-time Java, Ada, kernels, safety kernels, architecture-neutral systems, distributed programming. Professor.
	<i>Jack Whitham:</i> Reconfigurable architectures for embedded systems: Research Student
KERNELS	<i>Rob White:</i> Optimisation, architectures. Part-time Research Student.
	<i>Ke Yu:</i> System-level real-time operating system simulation: Research Student
EMBEDDED SYSTEMS	<i>Kun Wei:</i> Time bands for real-time systems: Research Assistant
	<i>Attila Zabos:</i> Mode-change protocols, flexible scheduling: Research Assistant
RECONFIGURABLE HARDWARE	<i>Alexandros Zerzelidis:</i> Architecture-neutral real-time systems, .Net. Research Student.
	<i>Fengxiang Zhang:</i> Real-time scheduling: Research Student
PORTABLE CODE	<i>Muhammad Zubair:</i> Reconfigurable and evolvable hardware: Research Student
	<i>Areej Zuhily:</i> Worst-case response time analysis: Research Student