The Design and Analysis of Non-Uniform Down-Sized Differential Distributed Amplifiers

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Abstract

In this paper the design and analysis of a novel non-uniform fully differential distributed amplifier is presented. The gain-bandwidth product of the proposed amplifier designed in a 0.18μm standard CMOS process reaches a record level of 34.76 GHz. Proved by both the analytical models and the HSPICE simulations, down-sizing the device and inductor sizes of each stage with respect to the preceding stage in a distributed amplifier will result in a better gain-bandwidth product. A comprehensive analytical study is carried out to predict the behavior of the amplifier. HSPICE simulations verify the superior performance of the proposed non-uniform distributed amplifier compared to its conventional counterpart in terms of a better gain-bandwidth product and a flat frequency response.

1. Introduction

The increasing trend in wireless/wire-line communication market for high data-rate applications, particularly the analog/RF front-end, is pushing the integrated circuits to operate in multi-gigahertz bandwidth. The distributed amplifier is known to be a good candidate for ultra broadband amplifier design. A distributed amplifier trades delay with bandwidth and, is therefore capable of achieving much higher bandwidth than lumped architectures [1]. The distributed amplifier concept was first proposed by Percival [2] as an attempt to resolve the usual gain-bandwidth constraint in resonant amplifier. Ginzton [1] in 1948 exploited this idea with thermionic devices and introduced the term, distributed amplifier. Since then, there have been tremendous efforts to incorporate the distributed concept in various technologies to achieve wide bandwidths.

Distributed amplifiers employ a topology in which inductors or transmission lines (T-lines) separate the gain stages, yet the output currents from individual stages combine in additive fashion. From another perspective, the

parasitic capacitances of the gain stages become a part of the electrical parameters of actual (or artificial) transmission lines, which results in higher bandwidth [3]-[7].

One of primary sources of performance degradation in any distributed amplifier is the existence of non-zero inductive loss and output resistance of the gain stages that in turn decrease gain and bandwidth. The inductive loss increases with frequency due to the skin effect phenomenon [3], which exacerbates the gain attenuation in high frequencies. As a consequence, the series loss of the inductors and output resistance of transistors dictate the bandwidth of distributed amplifiers.

In this paper a non-uniform down-sized fully differential distributed amplifier has been introduced. It is shown that down-sizing both the transistor size of each constituent stage and the inductor size of each artificial line toward the load results in a better gain-bandwidth product[1] compared to a conventional uniform CMOS differential distributed amplifier. The key advantage of using the differential topology is its immunity to common-mode environmental noise (e.g., power/ground noise and substrate noise) due to the on-chip interconnects, bond wires, and package parasitics. The superior noise performance of the proposed differential architecture compared to the single-ended circuit [8] is achieved at the expense of more power dissipation and larger chip area.

This paper is organized as follows: Section 2 discusses the conventional fully differential distributed amplifier. It also encompasses a detailed analysis of the gain of the conventional circuit as well as key parameters in the bandwidth calculation of the conventional circuit. Section 3 discusses the proposed non-uniform fully differential distributed amplifier. Section 4 includes the simulation results for both the conventional and proposed differential distributed amplifiers. The simulations have been carried in a 0.18μm CMOS process provided by the Jazz Semiconductor, Inc. The simulation results are based on the Jazz device model for the inductor, capacitor, and resistor. Finally, the conclusion is provided in Section 5.

2. Conventional Distributed Amplifier

The circuit schematic of a conventional CMOS differential distributed amplifier is shown in Fig. 1. (a) [6]

[1] . In this paper the gain-bandwidth product refers to both the voltage-gain as well as the power-gain.

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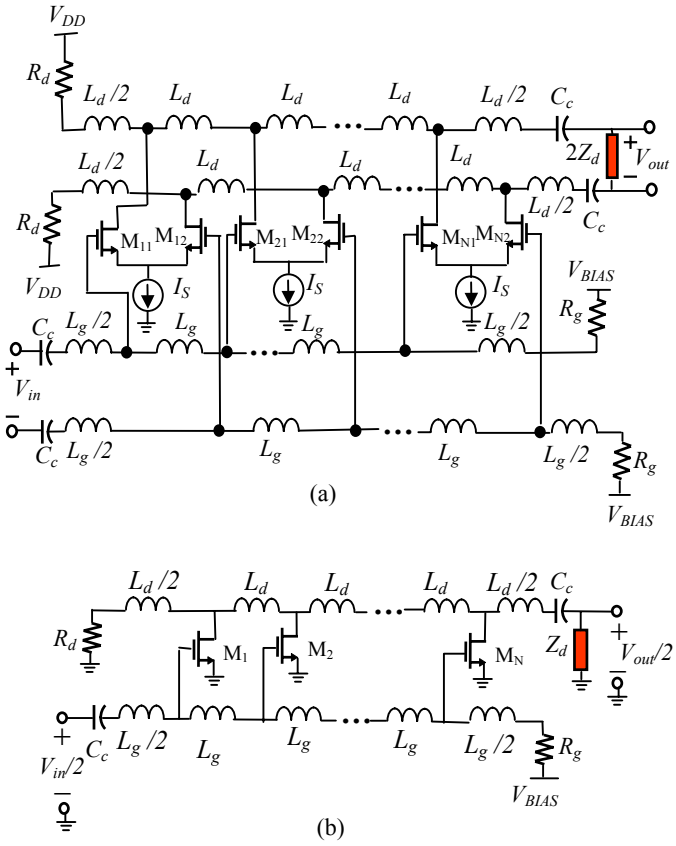


Fig. 1. (a) Conventional CMOS differential distributed amplifier (b) equivalent half circuit of the (a)

The gate-source and drain-bulk parasitic capacitances along with the inter-stage inductors form uniform LC circuits. The LC circuits virtually behave as transmission lines [4], [6], [9]. The input signal differentially applies to the gate lines, as depicted in Fig. 1 (a). Since the gate lines are identical, signals arriving at the gates of each differential pair have a 180-degree phase difference. Similarly, knowing the fact that drain lines are also identical, the signals in the drain lines have a 180-degree phase difference. Having identically matched differential pairs allows us to employ the half circuit technique [10]. The equivalent half circuit is shown in Fig. 1 (b). The differential voltage traveling along the gate lines excites each individual differential gain stage (*c.f.* Fig. 1 (a)). The signal at the input of each differential stage is amplified by that cell. The amplified signal at the differential output of each gain stage then propagates toward the load. The differential input signal traveling along the gate lines will be attenuated due to the non-zero inductor losses. Consequently, gain stages located at the far-end of the circuit will receive the signal with smaller voltage amplitudes. The equivalent small-signal model of the gate and drain lines of equivalent half circuit are shown in Fig. 2. For the drain lines, drain-source resistances of transistors as well as series resistances of inductors are the dominant contributors to the loss. As for the gate lines, the inductor series resistance is the only contributor to the loss.

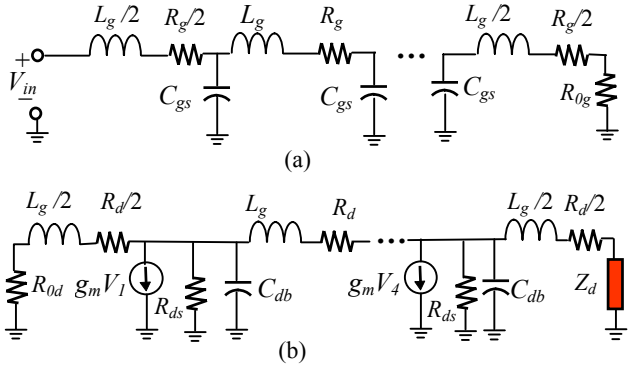


Fig. 2. The circuit models for (a) Gate line, and (b) drain line

Each LC line is terminated by its characteristic impedance (defined as *sqrt*(*L*/*C*)). From Fig. 2 (b), the current delivered to the load is [3]:

$$I_O = \frac{1}{2} g_m e^{-\frac{1}{2}\theta_d} \left(\sum_{k=1}^{N} V_k e^{-(N-k)\theta_d} \right) \quad (1)$$

where, V_k is the voltage across C_{gs} of the k^{th} transistor and N is the total number of stages. θ_d is defined as: $\theta_d = A_d + j\phi_d$ where A_d and ϕ_d are the attenuation and phase-shift of each inter-stage LC circuit in the drain line, respectively. V_k is expressed in terms of the input voltage and gate line propagation constant as follows [3]:

$$V_k = \frac{0.5 V_{in} e^{-(2k-1)\frac{1}{2}\theta_g}}{1 - (\frac{\omega}{\omega_c})^2} \quad (2)$$

where, similar to the drain line, $\theta_g = A_g + j\phi_g$. ω_c is the cutoff frequency of the gate line. The input power, the power delivered to the load, and voltage gain for the circuit of Fig. 1, under a matched termination, are derived as follows:

$$P_{in} = \frac{|0.5 V_{in}|^2}{2|Z_{0g}|^2} \mathrm{Re}\{Z_{0g}\} \quad (3)$$

$$P_{out} = \frac{1}{2} |I_O|^2 \mathrm{Re}\{Z_{out}\} \quad (4)$$

$$|A_v| = \sqrt{\frac{P_{out}}{P_{in}}} = \frac{g_m (R_{0d} R_{0g})^{\frac{1}{2}} \sinh[0.5N(A_d - A_g)] e^{-N(A_d + A_g)/2}}{2[1 - (\frac{\omega}{\omega_c})]^{1/2} \sinh[0.5(A_d - A_g)]} \quad (5)$$

where, $R_{0d,g} = \mathrm{Re}\{Z_{0d,g}\}$. From Eq. (5), it is observed that the bandwidth is defined by gate and drain line attenuations and the number of stages. The gate and drain attenuations, A_g and A_d, are frequency dependent. *This frequency dependence affects the flatness of the magnitude response of the gain.* The gate and drain attenuation per section are:

$$A_d = \mathrm{Re}\left\{ \sqrt{(j\omega L_d + R_d)(G_{ds} + jC_{db}\omega)} \right\} \quad (6)$$

$$A_g = \mathrm{Re}\left\{\sqrt{(j\omega L_g + R_g)\, jC_{gs}\omega}\right\} \tag{7}$$

To study the variations of the gate and drain attenuations with frequency, (6) and (7) are rewritten as follows:

$$A_d = \mathrm{Re}\left\{\sqrt{\left[-4(\frac{\omega}{\omega_c})^2 + L_d\omega\frac{G_{ds}}{Q}\right] + j\left[\frac{4}{Q}(\frac{\omega}{\omega_c})^2 + L_d\omega G_{ds}\right]}\right\} \tag{8}$$

$$A_g = \mathrm{Re}\left\{\sqrt{-4(\frac{\omega}{\omega_c})^2 + j\frac{4}{Q}(\frac{\omega}{\omega_c})^2}\right\} \tag{9}$$

where Q is the quality factor of each inter-stage inductor and $\omega_c=2/sqrt(LC)$ is the cutoff frequency of the line. Indicated in Fig. 3 is the gate and drain attenuations versus frequency for different cutoff frequencies and constant $L_d.G_{ds}$.

As an important observation, which is also seen from Fig. 3, the frequency dependence of the both the gate and the drain line attenuations is reduced as the cutoff frequency of the line increases.

To increase the gain-bandwidth product of the conventional distributed amplifier, we should first study the mechanisms that affect the gain and bandwidth of the conventional circuit.

For the uniform distributed amplifiers in which all gain stages are identical, the contribution of each gain stage to the overall output gain is the same. More precisely, the voltage waveform at the load termination is the superposition of the voltage waveforms propagating through different stages. This implies that for the special case of identical gate and drain lines, the voltage gain associated with each signal path, including gain stage, from the input to the output terminal of the amplifier is the same. On the other hand, the gain of each stage is linearly proportional to the transconductance (g_m) of each stage. For the fixed biasing point, the transconductance of each stage is linearly proportional to the sizing of the transistors of that stage. Consequently, for the fixed bias point sizing of the transistors in linearly affects the over gain. The bandwidth of the distributed amplifier is set by the frequency variation of the line's attenuation. From Eq. (5), the attenuation of the line exponentially increases the slope of the frequency roll-off of the magnitude response, which approximately causes an exponential decrease in the bandwidth. Furthermore, the frequency dependency of the gate and drain line attenuations is diminished by increasing the line cut-off frequency. The cut-off frequency of each line depends on the size of the inductors and capacitors of that line. The parasitic capacitances of the transistors in the distributed amplifier of Fig. 1 (a) are dominant components of the line's capacitances. Therefore, changing the transistor sizes of constituent stages will vary the gain and bandwidth of the amplifier.

The above observation provides the main idea behind the proposed non-uniform distributed amplifier to achieve a better gain-bandwidth product.

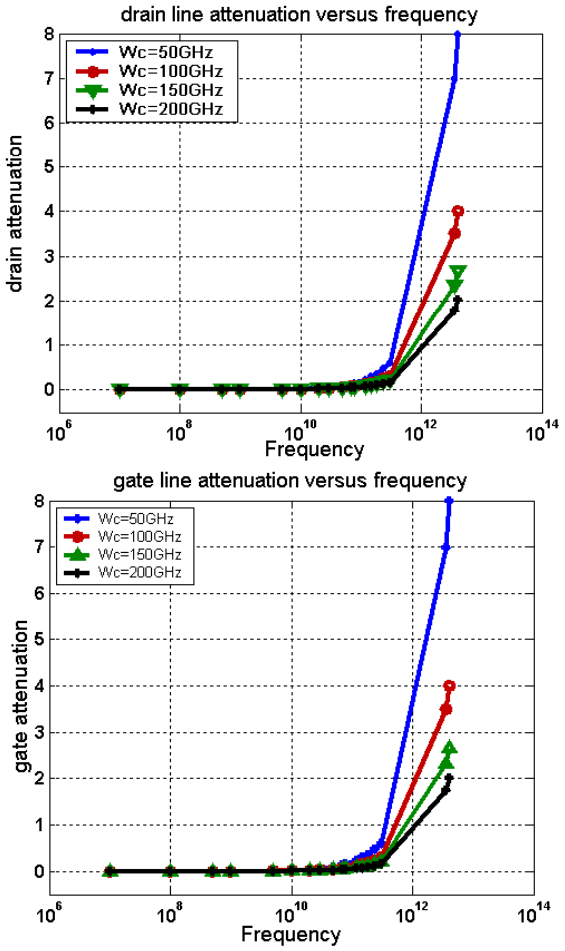
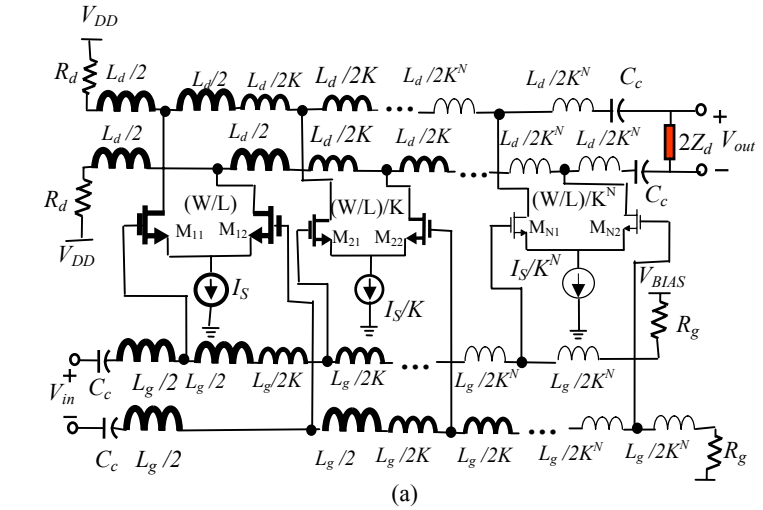


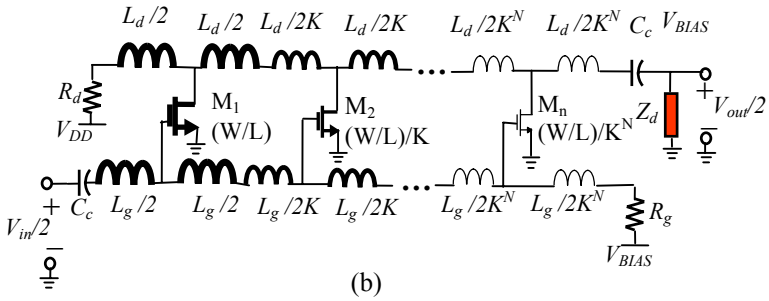
Fig. 3. The gate and drain attenuation versus frequency for the L_d=0.24nH and G_{ds}=270μmho

3. Proposed Non-Uniform Fully Differential Distributed Amplifier

The proposed non-uniform differential distributed amplifier is depicted in Fig. 4 (a). As was discussed in the previous section, the attenuation of the drain and gate lines exponentially effects the bandwidth of the circuit. In the proposed schematic, each stage toward load termination is progressively down-sized with a scaling factor of K. This obviously causes g_m, C_{db}, C_{gs}, and G_{ds} of each transistor to become $1/K^{th}$ of those of the transistor that belongs to the previous stage. The inter-stage inductor of each stage is also scaled down to be $1/K^{th}$ of the previous stage. Similar to the conventional circuit, signals in the gate lines have a 180-degree phase difference. Similarly, signals in the drain lines also have a 180-degree phase difference. Once again, identically matched differential pairs in each stage allow us to employ the half circuit technique [10].



(a)



(b)

Fig. 4. (a) The circuit schematic of the proposed N-stage non-uniform down-sized differential distributed amplifier with a scaling factor of *K*, and (b) the equivalent half circuit model of (a)

Fig. 4 (b) shows the equivalent half circuit model of proposed non-uniform differential distributed amplifier. Fig. 5 shows the small-signal models of the gate and drain lines for the equivalent half circuit model of the non-uniform distributed amplifier. Starting from Eq. (1) while accounting for the non-uniform characteristics of the proposed circuit, the output current for the scaling factor K=2 is calculated as follows:

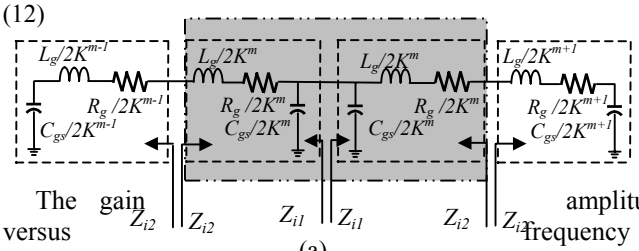
$$I_{out} = \frac{g_m}{2} e^{\frac{1}{2}\theta_d} \sum_{n=1}^{N} \frac{V_n}{K^{(n-1)}} e^{-\left(\frac{\theta_d}{K^n} + \sum_{i=n}^{N-1} \frac{\theta_d}{K^i}\right)} \tag{10}$$

Similarly, starting from Eq. (2), V_k for the proposed circuit of Fig. 4 (b) is obtained as follows:

$$V_n = \frac{V_{IN}}{(1-(\omega/\omega_c)^2)} e^{-\frac{\theta_g}{K^n} - \sum_{i=1}^{n-1} \frac{\theta_g}{K^{(i-1)}}} \tag{11}$$

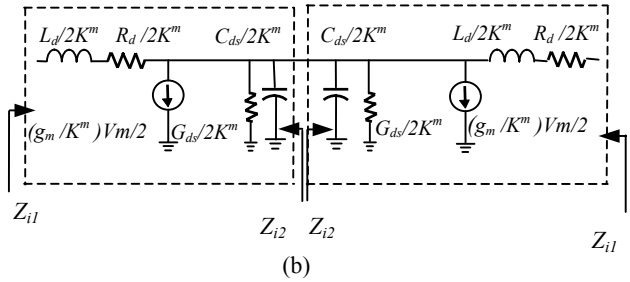
where, θ_g and θ_d is propagation constant of the first T-section of the gate line and drain lines, respectively. N is the number of stages and ω_c is the cutoff frequency of the first T-section of the gate line. We assume that T-sections of the gate and drain lines associated with the same stage have identical cutoff frequencies. The cut-off frequencies of the T-sections along the lines are doubled, as the signal travels toward the load. Substituting Eq. (11) in (10) and using equations (3) and (4), we have:

$$|A| = \frac{\sqrt{(1-(\frac{\omega}{K^N\omega_c})^2}}{1-(\frac{\omega}{\omega_c})^2} 0.5(R_{0d}R_{0g})^{\frac{1}{2}} \sum_{n=1}^{N} \frac{g_m}{K^{(n-1)}} e^{-\left(\frac{\theta_d+\theta_g}{K^n} + \sum_{i=1}^{n-1}\frac{\theta_g}{K^{(i-1)}} + \sum_{i=n}^{N-1}\frac{\theta_d}{K^i}\right)} \tag{12}$$



(a)

The gain versus amplitude frequency for the conventional distributed amplifier and proposed non-uniform distributed amplifier are shown in Figs. 6 (a) and (b), respectively.



(b)

Fig. 5. (a) Small signal model of the gate line for the proposed non-uniform distributed amplifier (b) Small signal model of the drain line for the proposed non-uniform distributed amplifier

This simulation is carried out under the assumption that the cutoff frequencies of the drain and gate lines for conventional distributed amplifier are identical. This cutoff frequency is set equal to the cutoff frequency of the first T-sections of the gate and drain lines in the proposed non-uniform distributed amplifier. In our experiment, the W/L-ratio of transistors in the conventional circuit is equal to W/L-ratio of the first transistor M_{11} and M_{12} in Fig. 4. M_{11} and M_{12} have the largest W/L-ratio in the non-uniform distributed amplifier. Therefore, the transconductance, g_m, of transistors in the conventional circuit is identical to the transconductance of the first transistor in non-uniform counterpart. Clearly, the proposed circuit has a superior gain-bandwidth product compared to the conventional one. Although the gain is halved, but the bandwidth becomes at least 10 times larger. The overshoot in the frequency response is readily explained using Eq. (5) and (12). As mentioned above, the cutoff frequency of each T-section is K times smaller than the previous section. Therefore, as the signals travels down the lines toward the

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load terminal, the cutoff frequency becomes K times larger and attenuation becomes K times smaller from each stage to the next stage. These phenomena result in an approximately exponential improvement in bandwidth for the proposed circuit compared to the conventional distributed amplifier using same number of stages. However, the gain of each stage is decreasing almost linearly from each stage to the next. As a result, the gain-bandwidth product for the proposed non-uniform distributed amplifier compared to the conventional distributed amplifier is largely enhanced. The HSPICE simulations given in the next section confirm these observations.

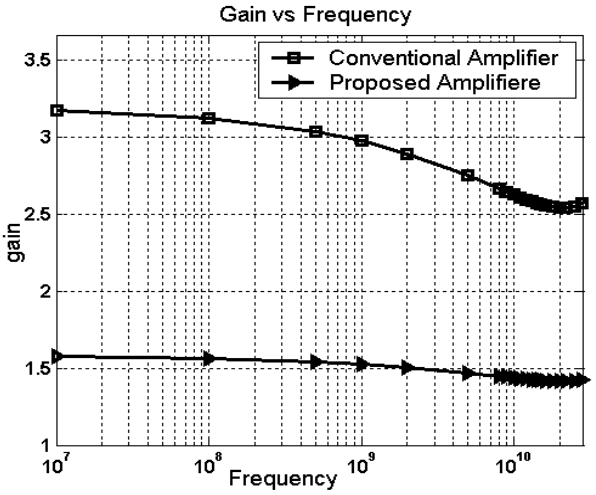

Fig. 6. Gain vs. frequency for the conventional and proposed distributed amplifier. The g_m= 33 *mmho* and ω_c=303 GHz

4. Simulation Results

The HSPICE simulation is carried out on the circuits designed in a 0.18μm standard CMOS process, which is provided by Jazz semiconductor Inc. Fig. 7 shows a comparison between the voltage gains of two 3-stage conventional amplifiers and the proposed 3-stage amplifier versus frequency. The scaling factor K is chosen to be 2. This scaling factor is taken as an example to show that the proposed amplifier achieves better gain-bandwidth product compared to the conventional amplifier. K=2 is not, however, the optimum scaling factor. Both conventional and proposed amplifiers have the same characteristic impedance of 50Ω. The load is assumed to be 100Ω. The cutoff frequency of the conventional amplifiers is the same as the first stage of the proposed amplifier. The conventional amplifier which is comprised of transistors with the W/L-ratio and tail current (I_S) equal to those of the first stage of the proposed amplifier has the largest gain and smallest bandwidth.

Similarly, the conventional amplifier consisting of transistors with W/L-ratio and tail current (I_S) equal to those of the last stage exhibits the smallest gain and the largest bandwidth.

Fig . 7 shows the voltage frequency response of the two conventional amplifier and the proposed non-uniform distributed amplifier. The proposed amplifier has the scaling factor of 2 with the first stage having (W/L)=200μm/0.18μm and tail current of 8mA. One conventional differential distributed amplifier has (W/L)=200μm/0.18μm tail current of 8mA. The other one has (W/L)=50μm/0.18μm and tail current of 2mA

As observed in Fig. 7, the gain of the proposed amplifier exhibits a flat frequency response with a much smaller overshoot than the conventional amplifiers. The voltage-gain-bandwidth product for the conventional amplifier with (W/L)=200 μm/0.18 μm and the tail current of 8mA is 20.45 GHz. The voltage-gain-bandwidth product for the conventional amplifier with (W/L)=50 μm/0.18 μm and the tail current of 2mA is 11.45 GHz. However, the voltage-gain-bandwidth product for the proposed amplifier is 34.76 GHz. Fig. 8 depicts the power gain versus frequency for the same amplifier as in the Fig. 7. The bandwidth-power-gain-product is increased, and for the same reason mentioned above, the power gain of the non-uniform differential distributed amplifier is more flat in the pass-band and the frequency overshoot is reduced.

5. Conclusion

In this paper the design of a new non-uniform differential distributed amplifier was presented. The effect of progressive down-sizing of the device and inductor sizes on the gain-bandwidth product of the distributed amplifier was studied. The circuit was design and simulated in a 0.18μm CMOS process. HSPICE simulations on both the proposed non-uniform distributed amplifier and the conventional circuit verified a considerable enhancement in the gain-bandwidth product.

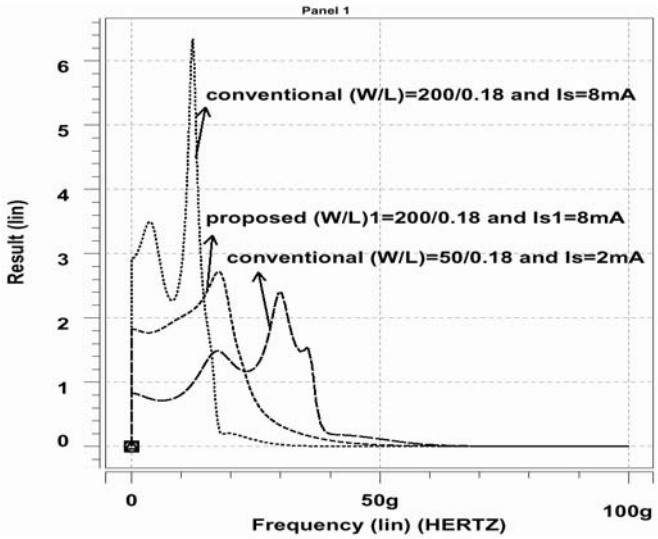

Fig. 7. The voltage gain vs. frequency for the proposed amplifier and two conventional amplifiers.

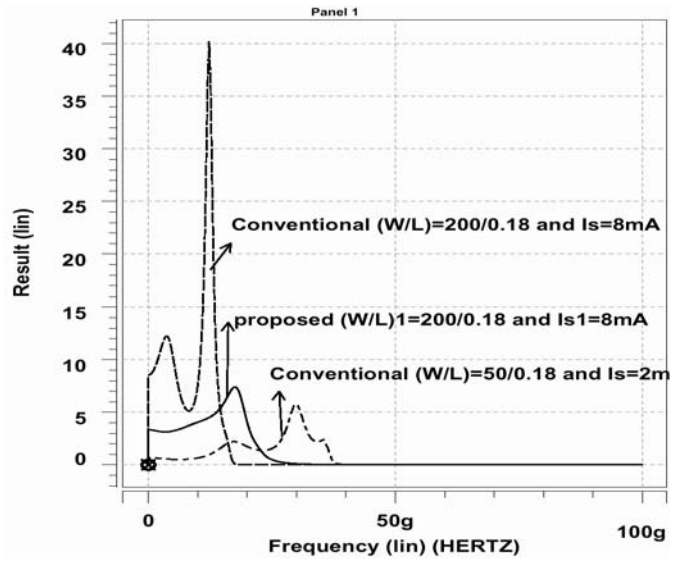

Fig. 8 Power gain vs. frequency of proposed amplifier and two conventional amplifiers.

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